A Novel Current-Scaling a-Si:H TFTs Pixel Electrode Circuit for AM-OLEDs

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***Abstract*—Hydrogenated amorphous silicon thin-film transistor (a-Si:H TFT) pixel electrode circuit with a function of current scaling is proposed for active-matrix organic light-emitting displays (AM-OLEDs). In contrast to the conventional current mirror pixel electrode circuit, in this circuit a high data-to-organic light-emitting device (OLED) current ratio can be achieved, without increasing the a-Si:H TFT size, by using a cascade structure of storage capacitors. Moreover, the proposed circuit can compensate for the variations of TFT threshold voltage. Simulation results, based on a-Si:H TFT and OLED experimental data, showed that a data-to-OLED current ratio larger than 10 and a fast pixel programming time can be accomplished with the proposed circuit.**

***Index Terms*—Active-matrix, active-matrix organic light-emitting displays (AM-OLEDs), current driving, current scaling, light-emitting diode (LED), organic light-emitting displays (OLED), polymer light-emitting device (PLED), thin-film transistor.**

I. Introduction

SINCE the first observations of the light emission in small molecules based organic light-emitting diodes (OLEDs) [1], there have been increasing interest in their applications to a large area flat panel displays due to their adequate opto-electric properties, versatility of colors, large viewing angle and potentially a low fabrication cost [2]–[4]. At the same time, for a number of years hydrogenated amorphous silicon thin-film transistor (a-Si:H TFT) and a low-temperature polysilicon (LTPS) TFT active-matrix (AM) array have been developed for liquid-crystal displays (LCDs). Recently it was also demonstrated that a combination of the OLEDs with the TFT active-matrix arrays can be used for a high resolution active-matrix OLEDs [5]–[10]. Since the AM-OLED luminance is directly proportional to the driving current passing through it, the pixel electrode circuits must deliver continuous current to OLED during the whole frame period [11].

To modulate the OLED current, two approaches have been often used. In the first approach, a voltage signal is used to directly control the driving current of two-TFT pixel electrode circuit. Unfortunately, in this pixel configuration, nonnegligible TFT characteristic variations (threshold voltage and field-effect mobility shifts) due to the manufacturing process variation and to the device aging can result in nonuniform luminance over the display area [6], [7], [10]. Current driving schemes with four-TFT pixel electrode circuits have been proposed as other approach to drive AM-OLED, whereby the current signal provided by external driver modulates directly the pixel electrode circuits [9], [10]. The four-TFT circuits can not only provide a continuous excitation to OLED, but at the same time it can also compensate for the TFT threshold voltage variation.

Although the current driving scheme improves the display luminance uniformity, a large timing delay can be observed at a low data current that is due to combination of a high OLED efficiency and charging of a large interconnect parasitic capacitances. For example, a current of 70 nA is sufficient to achieve luminance of 100 $\mathrm{cd/m^2}$ when an OLED with efficiency of 20 cd/A or higher is used. However, for such small current an interconnect parasitic capacitance of about 10 pF needs more than 150 μs to build up a sufficient voltage level. This charging time is much larger than 30 μs, that is needed for a display with VGA $(640 \times \mathrm{RGB} \times 480)$ resolution operated at 60 Hz. To reduce the programming time delay, the pixel electrode circuits based on an adjustable TFTs geometric ratio with the current scaling function have been proposed [12], [13]. One example of such circuit is current mirror type pixel electrode circuit, Fig. 1(a). In this circuit a high data-to-OLED-current ratio can only be achieved for a large geometric ratio of T4 to T3. This can significantly limit the pixel electrode aperture ratio. A possible solution to this problem is top emission OLED structure in which a nearly entire pixel area could be used as light-emitting region [14]. In general, the pixel aperture ratio should not be influenced by the size of TFT and the complexity of pixel electrode circuit. This is especially true for high resolution displays. For example, the pixel size of display with resolution higher than 200 ppi is around 125×125 $\mu\mathrm{m}^2$ [15], so that the T4/T3 ratio is limited to 2.5/1 when T3 width is of 50 μm. Consequently, the current scaling ratio of current mirror type pixel electrode circuit cannot be effectively used when the display resolution increases.

In this paper, we present an improved current driver pixel circuit based on a-Si:H TFT technology with a novel current scaling function. A cascade structure of storage capacitors is proposed here to achieve a high data-to-OLED-current ratio without increasing TFTs size in comparison to a conventional current mirror pixel circuit, shown in Fig. 1(a). The proposed pixel electrode circuit can also compensate for a-Si:H TFT threshold voltage variation so that uniform display luminance

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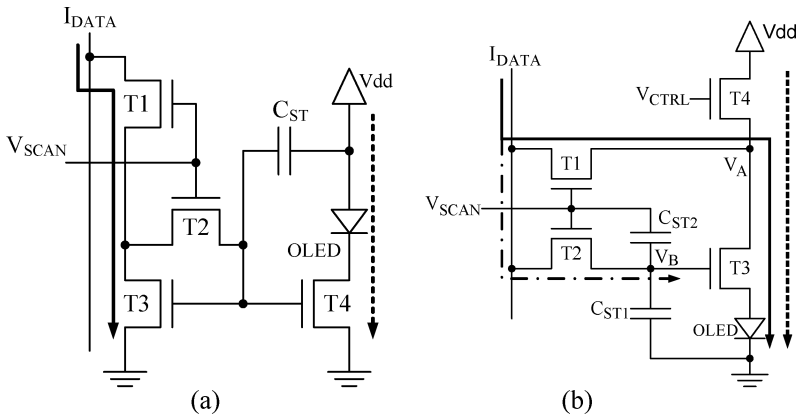


Fig. 1. Schematic diagrams of current driven pixel circuits with (a) conventional current mirror and (b) cascade structure of storage capacitors.

is expected. First, we describe the structure and discuss the operation principles of pixel electrode circuit. The parameters used for circuit simulation are discussed in Section III. The simulation results and circuit performance are discussed in Section IV, with conclusion presented in Section V.

II. Proposed Pixel Electrode Circuit

The proposed current driven pixel electrode circuit consists of three switching TFTs (T1, T2, T4), one driving TFT (T3) and two storage capacitors ($C_{\rm ST1}$, $C_{\rm ST2}$) connected between a scan line and ground with a cascade structure, as shown in Fig. 1(b). The operation of the circuit is controlled by four external terminals: $V_{\rm SCAN}$, $V_{\rm CTRL}$, $I_{\rm DATA}$, $V_{\rm dd}$, and ground. The signals of $V_{\rm SCAN}$, $V_{\rm CTRL}$, and $I_{\rm DATA}$ are supplied by external drivers while the cathode of OLED is grounded. It should be noticed that to simplify the circuit analysis, one node of $C_{\rm ST1}$ connected to the ground is adopted. In practice, the ground electrode of $C_{\rm ST1}$ needs additional routing and contact via to connect with the OLED grounded cathode. Therefore the $C_{\rm ST1}$ can be connected to the $V_{\rm dd}$ line instead of the ground in order to reduce the layout area. The $V_{\rm dd}$ electrode is connected to the external power supply to provide a constant voltage signal to the proposed pixel circuit. The operation of this pixel electrode circuit can be described as follows.

During the ON-state, the scan line signal $V_{\rm SCAN}$ turns on the switching transistors T1 and T2. During this time, a data current signal $I_{\rm DATA}$ passes through T1 and T3 to OLED, shown as the solid line in Fig. 1(b), and sets the voltage at the T3 drain electrode (nodes A). At the same time the voltage at the T3 gate electrode (node B) is set by $I_{\rm DATA}$ passing through T2 (dash line). The control signal $V_{\rm CTRL}$ turns T4 off to ensure that no current flows through T4. Consequently, in an ideal case the OLED current in ON-state, $I_{\rm OLED-ON}$, should be equivalent to $I_{\rm DATA}$. Since the T3 drain and gate electrodes are at the same potential, T3 will operate in the deep saturation region, e.g., $V_{\rm DS} > V_{\rm GS} - V_{\rm TH}$ (threshold voltage) and the V_A and V_B voltages at both nodes are determined automatically according to (1):

$$I_{\rm DATA} = \frac{1}{2} \cdot \mu_{\rm FE} \cdot C_{\rm OX} \cdot \frac{W_3}{L_3} \cdot (V_{\rm GS} - V_{\rm TH})^2 \qquad (1)$$

where $\mu_{\rm FE}$, $C_{\rm OX}$, $\rm W_3$ and $\rm L_3$ are field-effect mobility, gate oxide capacitance, width and length of TFT(T3), respectively. If T3 threshold voltage changes and if this change is not higher than $V_{\rm SCAN}$ amplitude, the T3 gate voltage, $V_{\rm B-ON}$, will be adjusted accordingly to ensure the identical $I_{\rm DATA}$ in the ON-state. Therefore, $V_{\rm B-ON}$ is always adjusted to keep $I_{\rm DATA}$ at about the same value regardless of a-Si:H TFT threshold voltage. The $V_{\rm B-ON}$ will be stored in both $C_{\rm ST1}$ and $C_{\rm ST2}$ and the voltage across $C_{\rm ST2}$ is $V_{\rm SCAN} - V_{\rm B-ON}$.

When the pixel changes from the ON- to the OFF-state, $V_{\rm SCAN}$ turns off T1 and T2, and $V_{\rm CTRL}$ simultaneously turns on T4. Because $C_{\rm ST2}$ is connected between the scan line and the node B to form a cascade structure with $C_{\rm ST1}$, $V_{\rm SCAN}$ change from high to ground state will reduce $V_{\rm B-ON}$ to $V_{\rm B-OFF}$ due to the feed-through effect of the capacitors. $V_{\rm B-OFF}$ can be derived from the charge conservation theory, and is given by (2), in which $\Delta V_{\rm SCAN}$ and $C_{\rm OV-T2}$ are an amplitude of $V_{\rm SCAN}(= V_{\rm SCAN-ON} - V_{\rm SCAN-OFF})$ and the gate-to-source/drain overlap capacitance of T2, respectively

$$V_{B-\rm OFF}=V_{B-\rm ON}-\Delta V_{\rm SCAN} \cdot \frac{C_{ST2}||C_{OV-T2}}{C_{ST1}+C_{ST2}||C_{OV-T2}}. \qquad (2)$$

A reduced T3 gate voltage, $V_{\rm B-OFF}$, will be hold in $C_{\rm ST1}$ and $C_{\rm ST2}$ and it will continuously turn on T3 during this time period. Since the overdrive voltage of T4 $(= V_{\rm CTRL} - V_A - V_{\rm TH})$ is lower than $V_{\rm dd} - V_A$, the T4 is working in saturation region. In order to ensure that the V_A is similar to $V_{\rm dd}$ and the T3 is operating in the deep saturation region, the width of T4 should be large enough to reduce the turn-on resistance of T4. A current smaller than $I_{\rm DATA}$, shown as the dash line in Fig. 1(b), will be generated by $V_{\rm B-OFF}$ and will pass through T4 and T3 to OLED. Consequently, the OLED current in OFF-state, $I_{\rm OLED-OFF}$, will be smaller than $I_{\rm DATA}$.

Since the T3 gate voltage decreases from $V_{\rm B-ON}$ to $V_{\rm B-OFF}$, the OLED driving current is scale-down from ON- to OFF-state by the storage capacitor cascade structure. The quantity of voltage drop, shown as $\Delta V_{\rm SCAN} \cdot C_{\rm ST2}||C_{\rm OV-T2}/(C_{\rm ST1} + C_{\rm ST2}||C_{\rm OV-T2})$ in (2), will increase with increasing $\Delta V_{\rm SCAN}$, $C_{\rm OV-T2}$ and $C_{\rm ST2}$ values and will lead to a smaller $I_{\rm OLED-OFF}$. In other words, the scale-down ratio, $R_{\rm SCALE} = I_{\rm OLED-ON}/I_{\rm OLED-OFF}$, is related to the size of $C_{\rm ST2}$, $C_{\rm OV-T2}$ and $\Delta V_{\rm SCAN}$. Since

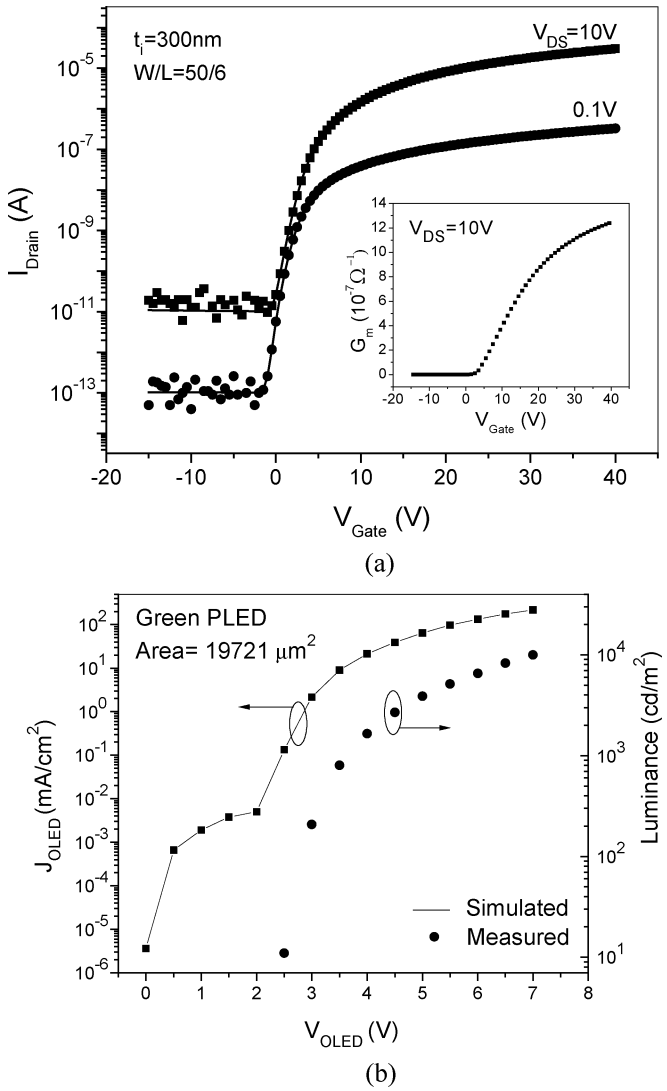


Fig. 2. (a) Transfer characteristics of a-Si:H TFT. The transconductance versus gate voltage is shown in insert. (b) An example of measured PLED current density and brightness variation with supplied voltages.

the small geometric size is adequate for switching TFT T2, the small $C_{\mathrm{OV-T2}}$ which is parallelly connected to the C_{ST2} can be regarded as a portion of C_{ST2}. Therefore it is expected that a larger C_{ST2} will result in larger R_{SCALE}. Consequently, when a very large data current I_{DATA} is used to charge the pixel electrode and to shorten the pixel programming time, at the same time a smaller driving current $I_{\mathrm{OLED-OFF}}$ can be achieved for lower gray scales.

III. Parameter Extraction and Pixel Electrode Circuit Design

Synopsis H-SPICE simulation tool with the Rensselaer Polytechnic Institute (RPI) Troy, NY, a-Si:H TFT model [16], [17] was used to evaluate the proposed pixel electrode circuit. The a-Si:H TFT parameters developed within our group were used in this simulation [18], [19]. The transfer characteristics ($I_D - V_{\mathrm{GS}}$, drain current versus gate-to-source voltage) of a-Si:H TFT are shown in Fig. 2(a) and in the insert its transconductance is given. To simulate the behavior of OLED the conventional semiconductor diode model, with the parameters extracted for organic polymer light-emitting device (PLED) fabricated in our laboratory, was used. The opto-electrical properties of PLED are shown in Fig. 2(b) and were described elsewhere [20]. In the pixel design, a C_{ST1} with the fixed size of 2.5 pF was used and C_{ST2} size was varied from 210 to 625 fF to achieve different $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$ ratios. Since T2 works as a switch in this circuit, its size can be smaller in comparison with other TFTs. Based on our own experience we believe that a high-performance a-Si:H TFT with μ_{FE} higher than 1.5 $\mathrm{cm^2V/s}$ is essential for future a-Si:H TFT pixel electrode circuit. The a-Si:H TFT with lower μ_{FE} will need a higher driving voltage and larger geometric size to achieve an adequate OLED driving current level. Then, increased display power consumption and reduced pixel aperture ratio, when light is emitted through the substrate, are expected. In addition, it is expected that a higher performance TFT will have better electrical stability over the time. The a-Si:H TFTs and OLED parameters used for this pixel electrode circuit simulation are given in Table I.

TABLE I
Parameters Used in Pixel Circuit Simulation

Device parameters for TFT	
W/L (T_1, T_3, T_4) (μm)	150/6
W/L (T_2) (μm)	50/6
V_{TH} (V)	2
μ_{FE} (cm^2/V-sec)	1.9
C_{OV} (nF/m)	0.2
I_{OFF} (pA)	0.1
C_{ST1} (pF)	2.5
C_{ST2} (fF)	210~625
Device parameters for OLED	
n	31
R_S (Ω)	20
I_S (A)	8 x 10^{-5}
C_{OLED} (pF)	3
Supplied signals	
V_{SCAN} (V)	0~35
V_{CTRL} (V)	0~35
Vdd (V)	35
I_{DATA} (μA)	0~5
Times (mSec)	
t_{ON}	0.33
t_{OFF}	33

IV. Simulation Results and Discussion

A. Current-Scaling Ratio

The proposed current-scaling pixel electrode circuit was evaluated using H-SPICE and an example of the waveforms is shown in Fig. 3. In this specific case, in ON-state, the voltages at node A and B are set to appropriate levels to allow I_{DATA} of 4 μA to pass through T3. It should be noticed that in ideal

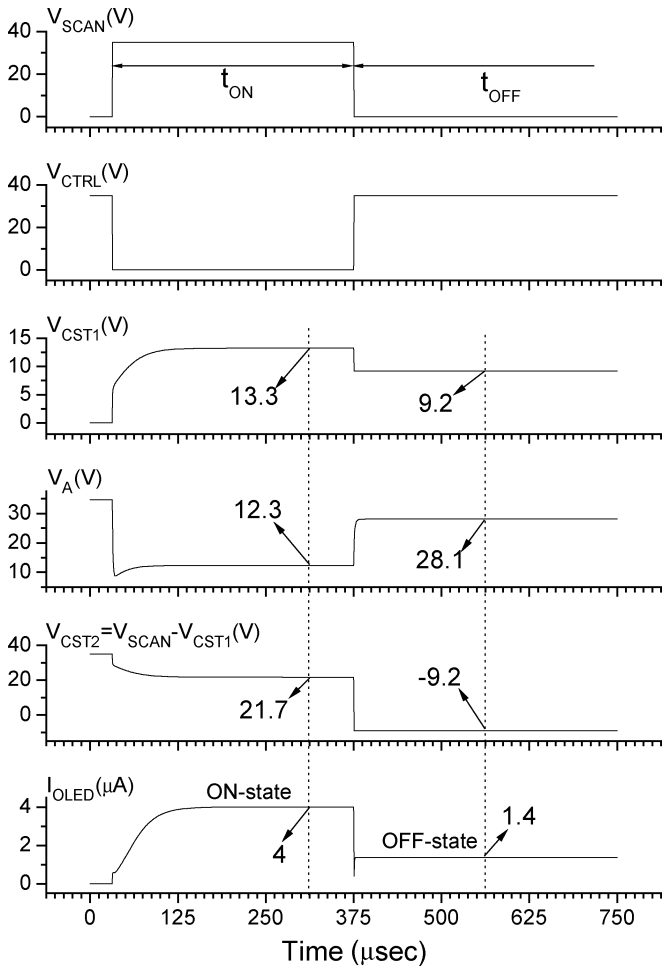


Fig. 3. Example of pixel operation waveforms simulated by H-SPICE for $V_{\rm dd} = 35$ V.

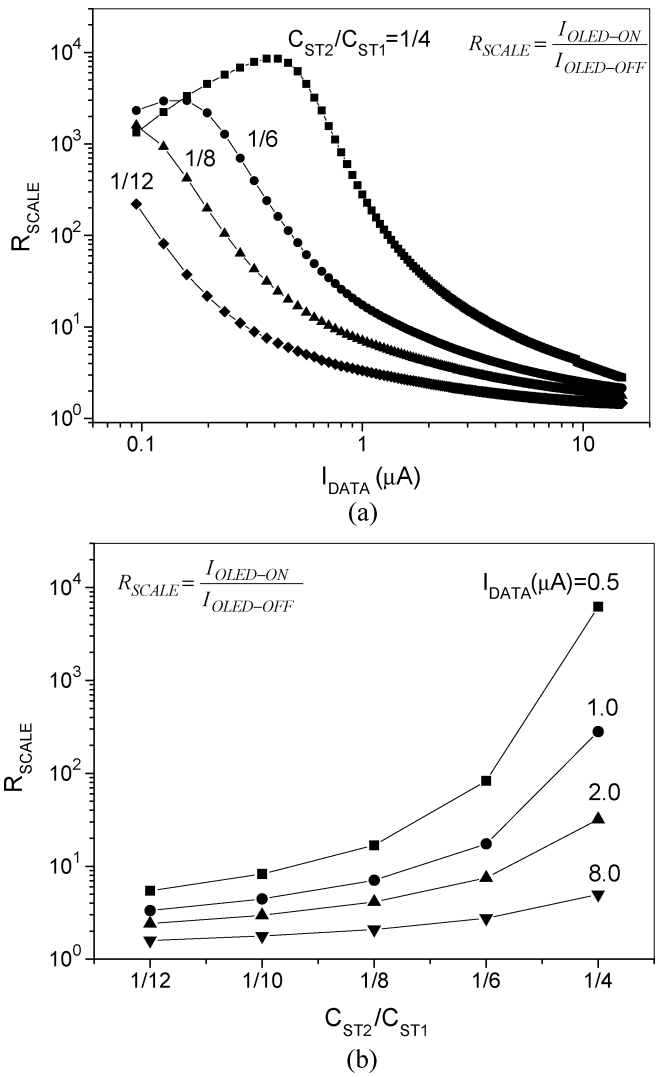


Fig. 4. Variation of the scale-down ratio versus (a) data current and (b) ratio of storage capacitances.

case the voltages at A and B nodes are identical. However, in practice, there will be a difference between A and B voltages because $I_{\rm DATA}$ passing through T1 causes a voltage drop between drain and source electrodes of T1. In OFF-state, in this special case the T3 gate voltage decreases from 13.3 ($V_{\rm B-ON}$) to 9.2 V ($V_{\rm B-OFF}$) and V_A changes from 12.3 to 28.1 V. V_A higher than V_B keeps T3 operating in deep saturation region and the drop of V_B results in reduction of $I_{\rm OLED}$ from 4 ($= I_{\rm OLED-ON}$) to 1.4 μA ($= I_{\rm ONED-OFF}$). This figure clearly shows that $I_{\rm OLED-ON}$ is different from $I_{\rm OLED-OFF}$ and the $I_{\rm OLED-ON}/I_{\rm OLED-OFF} = R_{\rm SCALE}$ $(4/1.4 = 2.86)$ is obtained.

Since $I_{\rm OLED-ON}(= I_{\rm DATA})$ is larger than $I_{\rm OLED-OFF}$ by a factor of $R_{\rm SCALE}$, the average OLED current $(I_{\rm AVG})$ for the pixel electrode circuit must be properly defined

$$I_{\rm AVG} = \frac{I_{\rm OLED-ON} \cdot t_{\rm ON} + I_{\rm OLED-OFF} \cdot t_{\rm OFF}}{t_{\rm ON} + t_{\rm OFF}} \qquad (3)$$

where $t_{\rm ON}$ and $t_{\rm OFF}$ denote the select and deselect periods during the frame time, respectively.

Since the $I_{\rm OLED-ON} = I_{\rm OLED-OFF} \cdot R_{\rm SCALE}$, (3) can be written as

$$I_{\rm AVG} = I_{\rm OLED-OFF} \cdot \left[\frac{R_{\rm SCALE} \cdot t_{\rm ON} + t_{\rm OFF}}{t_{\rm ON} + t_{\rm OFF}}\right]. \qquad (4)$$

From this equation an accurate $I_{\rm AVG}$ can be calculated for various combinations of $I_{\rm OLED-OFF}$ and $R_{\rm SCALE}$ to satisfy the display requirements for different gray scales. As it will be shown below to be able to display low gray scales, not only a low $I_{\rm OLED-OFF}$ but also a high $I_{\rm OLED-ON}$ are needed, at the same time, to control both a low display luminance and a fast programming time. Combination of a low $I_{\rm OLED-OFF}$ and a large $R_{\rm SCALE}$ can be used to satisfy such display requirement. For higher gray scales, a high $I_{\rm OLED-ON}$ is not needed since a high $I_{\rm OLED-OFF}$ can be achieved. Therefore, a combination of a large $I_{\rm OLED-OFF}$ and a low $R_{\rm SCALE}$ is appropriate to display high gray scales.

Since the scaledown ratio ($R_{\rm SCALE} = I_{\rm OLED-ON}/I_{\rm OLED-OFF}$), will affect the performance of the proposed pixel electrode circuit, it is important to evaluate its evolution with the $I_{\rm DATA}(= I_{\rm OLED-ON})$ and $C_{\rm ST2}/C_{\rm ST1}$. The variation of $R_{\rm SCALE}$ as a function of $I_{\rm DATA}$ is shown in Fig. 4(a). From this figure we can conclude that when $C_{\rm ST2}/C_{\rm ST1} = 1/12$, $R_{\rm SCALE}$ decreases from 210 to 1.5 as $I_{\rm DATA}$ increases from 0.1 to 10 μA. In this specific case since $V_{\rm B-ON}$ at a high gray scale is larger than that at a low gray scale, it is expected that

a large I_{DATA} will pass through T3. And a fixed voltage drop induced by $\Delta V_{\mathrm{SCAN}} \cdot C_{\mathrm{ST2}}/(C_{\mathrm{ST1}} + C_{\mathrm{ST2}})$ is relatively small in comparison to $V_{\mathrm{B-ON}}$, hence data current drop is expected to be small. In the other words, a fixed voltage drop can dramatically affect $V_{\mathrm{B-ON}}$ at low gray scales where $V_{\mathrm{B-ON}}$ is small. Therefore, desirable a high R_{SCALE} at low gray scales and a low R_{SCALE} at high gray scales can be achieved by proposed pixel electrode circuit. The variation of R_{SCALE} with the $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$ is as shown in Fig. 4(b). This figure was calculated from Fig. 4(a). It should be mentioned that, (2), a large $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$ ratio can induce a large V_B offset between pixel ON- and OFFOFF-state. Consequently, V_B decrease will result in the scale-down of the data current and in a high R_{SCALE}. The simulation results showed that when I_{DATA} is fixed, R_{SCALE} increases when C_{ST2} increases from 210 to 625 fF, corresponding to an increase of $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$ from 1/12 to 1/4. Fig. 4(b) also demonstrates that when a smaller I_{DATA} is used, a higher R_{SCALE} can be achieved with the constant $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$.

The current-scaling function is performed so that the large programming current can be reduced to an appropriate value when the pixel operates from the ON- to the OFF-state. In ON-state, the $I_{\mathrm{OLED-ON}}(= I_{\mathrm{DATA}})$ are identical in not only the conventional but also the proposed pixel electrode circuits because the external driver directly controls the current, Fig. 5(a). When pixels work in OFF-state, the proposed pixel circuit reveals superior current-scaling ability in comparison with the conventional current-driven pixel electrode circuit [9], [10] which just ideally keeps the $I_{\mathrm{OLED-OFF}}$ equivalent to $I_{\mathrm{OLED-ON}}$ [Fig. 5(b)]. It should be noticed that the $I_{\mathrm{OLED-OFF}}$ versus I_{DATA} of the conventional pixel circuit changes from linear to curved behavior due to the charge injection phenomenon. This charge injection can occur when the gate voltage is removed, and when the charge carriers in the T2 channel are released and redistributed into the drain and source electrodes. The carrier redistribution will alter the voltages at both nodes. Therefore, the charge injection from T2 causes the $I_{\mathrm{OLED-OFF}}$ slightly deviate from $I_{\mathrm{OLED-ON}}$. From Fig. 5(b), it is obvious that the large $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$ results in significant decrease of the $I_{\mathrm{OLED-OFF}}$. Moreover, since the OFF-state period is much longer than ON-state, the small $I_{\mathrm{OLED-OFF}}$ in OFF-state can further reduce the I_{AVG} even if the $I_{\mathrm{OLED-ON}}$ is large. Using (3), the plots of I_{AVG} versus $I_{\mathrm{DATA}}(= I_{\mathrm{OLED-ON}})$ in one frame period $(t_{\mathrm{ON}} + t_{\mathrm{OFF}})$ with $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$ ratios as a parameter are shown in Fig. 5(c). For example, the proposed pixel electrode circuit can generate I_{AVG} ranging from 1 nA to 5 μA with I_{DATA} ranging from 0.1 to 10 μA. By contrast, the I_{AVG} of conventional pixel electrode circuit is almost equal to I_{DATA}. In other words, a very small I_{AVG} can only be achieved by the I_{DATA} having a similar magnitude. From these figures, it is evident that I_{DATA} larger than I_{AVG} can be used to program the proposed pixel circuit in ON-state without increasing the a-Si:H TFTs geometric size. Hence, using an additional C_{ST2} to form a cascade capacitors structure, a large R_{SCALE} can be achieved and a high I_{DATA} can be used to accelerate the pixel circuit programming in ON-state.

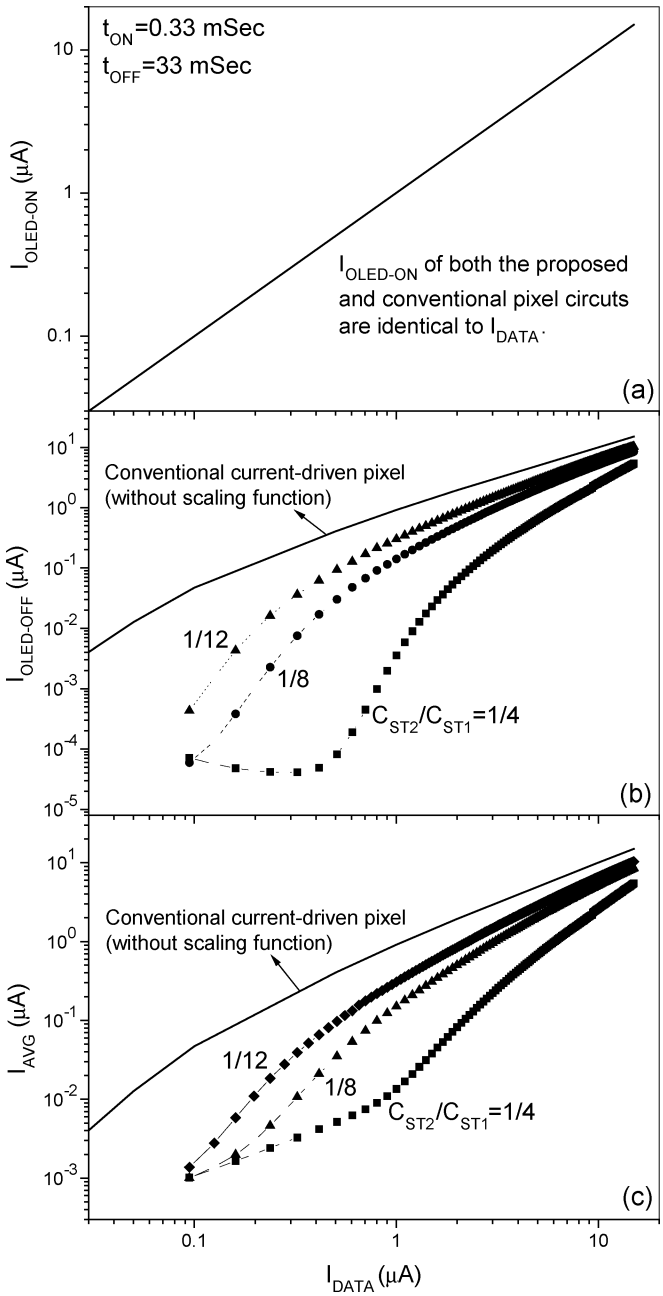


Fig. 5. Variation of the $I_{\mathrm{OLED-ON}}$, $I_{\mathrm{OLED-OFF}}$ and I_{AVG} during one frame period versus $I_{\mathrm{DATA}}(= I_{\mathrm{OLED-ON}})$ at various $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$ ratio.

To demonstrate the proposed pixel electrode circuit outstanding current scaling function in comparison with both the conventional current-driven and current-mirror pixels, one simulated I_{AVG} as a function of I_{DATA} for each pixel electrode circuit is shown in Fig. 6. Although the current-mirror pixel is able to scale down I_{DATA}, the scale-down ratio R_{SCALE} is constant in the whole range of I_{DATA}. In current-mirror pixel, a large I_{DATA} for high gray scales will result in a high power consumption due to the fixed scale-down ratio. In addition, to achieve the current scaling function, a larger driving TFT T4 needed in the current-mirror pixel will substantially reduce the pixel electrode aperture ratio. From Fig. 6, we can conclude that with the I_{DATA} ranging from 0.1 to 10 μA, our proposed pixel circuit can achieve I_{AVG} ranging from 1 nA to 5 μA,

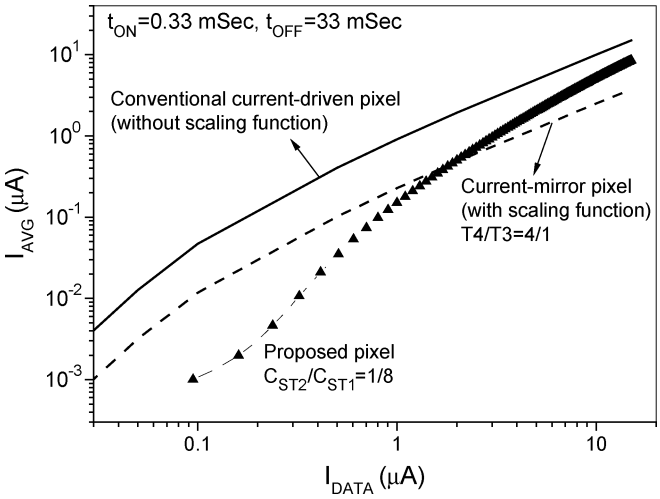


Fig. 6. Comparison of $I_{\rm AVG}$ as a function of $I_{\rm DATA}$ among conventional current-driven, current-mirror, and proposed pixels.

which represents a much wider range in comparison with the conventional current-driven pixel (0.05 to 10 μA) and the current-mirror pixel (0.01 to 2.5 μA). Therefore, the proposed pixel circuit can yield not only a high $I_{\rm DATA}$ and a high $R_{\rm SCALE}$ for the low gray scales, but also reasonable $I_{\rm DATA}$ for a high gray scale to avoid large display power consumption.

B. Influence of Threshold-Voltage Variation

To investigate the influence of $V_{\rm TH}$ variations of T3 and T4 on pixel circuit performance, various threshold voltage deviations ($\Delta V_{\rm TH} = V_{\rm TH}$(after stress)$-V_{\rm TH}$(initial)), based on the experimental results reported in [19], have been used in pixel circuit simulation. Since the $I_{\rm OLED-ON}(= I_{\rm DATA})$ is not affected by $\Delta V_{\rm TH}$ and the $I_{\rm OLED-OFF}$ is related to $I_{\rm AVG}$ through (4), the variation of $I_{\rm OLED-OFF}$ with the TFT threshold voltage is used to estimate the influence of $\Delta V_{\rm TH}$ on pixel circuit operation. For $C_{\rm ST2}/C_{\rm ST1} = 1/8$, the variation of the $I_{\rm OLED-OFF}$, defined by (5), with $\Delta V_{\rm TH}$ can be calculated

$$\Delta I_{\rm OLED-OFF} = \frac{I_{\rm OLED-OFF}(\Delta V_{\rm TH}) - I_{\rm OLED-OFF}(\Delta V_{\rm TH}=0)}{I_{\rm OLED-OFF}(\Delta V_{\rm TH}=0)}. \quad (5)$$

The variation of $\Delta I_{\rm OLED-OFF}$ as a function of $\Delta V_{\rm TH}$ is shown in Fig. 7(a). Following the increase of $\Delta V_{\rm TH}$, $\Delta I_{\rm OLED-OFF}$ gradually increases from around 1 to 6% when $I_{\rm OLED-OFF}$ is higher than 1.0 μA. The $\Delta I_{\rm OLED-OFF}$ up to 6% at $\Delta V_{\rm TH}$ of 4 V can be reached. This is due to turn-on resistance of T4 and channel length modulation of T3. In ideal case, $I_{\rm OLED-OFF}$ of T3 operating in saturation mode is independent of drain voltage V_A. However, in practice the TFTs are impacted by the channel length modulation and the drain voltage variation can only slightly affect $I_{\rm OLED-OFF}$. Since the turn-on resistance of T4 changes with the $\Delta V_{\rm TH}$ increase, the T3 can suffer a serious drain voltage offset ΔV_A between ON- and OFF-state so that the $I_{\rm OLED-OFF}$ can be changed. In other words, an increase of $I_{\rm OLED-OFF}$ with a high T4 turn-on resistance can lead to a decrease of V_A and consequently can result in a large $\Delta I_{\rm OLED-OFF}$, Fig. 7(b). In order to suppress the effect of T4 $\Delta V_{\rm TH}$, a higher $V_{\rm CTRL}$ or T4 with a larger width can be used

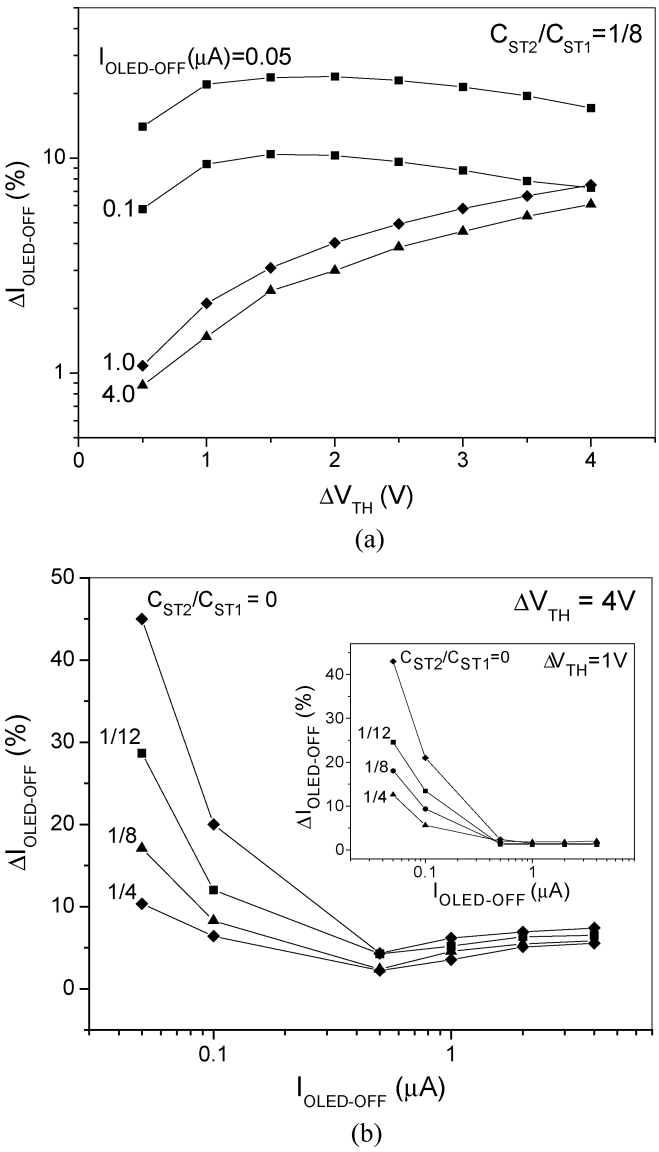


Fig. 7. (a) Variation of $\Delta I_{\rm OLED-OFF}$ as function of TFT threshold voltage shift. (b) $\Delta I_{\rm OLED-OFF}$ versus OLED current during display operation OFF-state for different $C_{\rm ST2}/C_{\rm ST1}$ and $\Delta V_{\rm TH} = 4$V. The data for $\Delta V_{\rm TH} = 1$ V is shown in insert.

to reduce the turn-on resistance of T4. However, an additional voltage signal can increase the complexity of peripheral drivers and a larger T4 can slightly decrease the pixel aperture ratio for bottom light-emission OLED structure.

Substantial increase of $\Delta I_{\rm OLED-OFF}$ when $I_{\rm OLED-OFF}$ is lower than 100 nA is due to the influence of charge injection of switching T2 on $V_{\rm B-ON}$. Since a small $V_{\rm B-ON}$ will result from a low driving current $I_{\rm OLED-ON}$ at low gray scales, the charge carrier released from T2, when T2 is turn-off, can reduce the $V_{\rm B-ON}$. Therefore, $V_{\rm B-ON}$ can be modified by not only a voltage drop induced by cascade structure of $C_{\rm ST1}$ and $C_{\rm ST2}$ but also by a charge injection from T2. In addition, the $V_{\rm TH}$ shift of all TFTs can lead to a higher sensitivity of $V_{\rm B-ON}$ to the charge injection from T2. Therefore, large storage capacitor is needed to eliminate the effect of T2 charge injection. As shown in Fig. 7(b), when large $C_{\rm ST2}/C_{\rm ST1}$ is used, a significant reduction of $\Delta I_{\rm OLED-OFF}$ at low gray scales is observed

in comparison to $C_{\mathrm{ST2}}/C_{\mathrm{ST1}} = 0$. From our data shown in Figs. 4(b) and 7(b), we can conclude that a large $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$ can achieve a high R_{SCALE} as well as a small $\Delta I_{\mathrm{OLED-OFF}}$.

C. Effects of Device Spatial Mismatch and Temperature

Mismatch of TFT geometric size and its operating temperature can affect the stability of scale-down ratio R_{SCALE}. The TFT size mismatch usually can result from device fabrication processes such as over-etching and alignment errors. The heat generated by nonemissive recombination of electron and hole in OLED can also increase substrate temperature thus alter the electrical performance of TFTs. According to (1) and (2), the OLED current in OFF-state can be given as

$$I_{\mathrm{OLED-OFF}} = \beta(V_{\mathrm{GS}} - V_{\mathrm{TH}} - V_{offset})^2 = \beta\left(\sqrt{\frac{I_{\mathrm{OLED-ON}}}{\beta}} - V_{\mathrm{offset}}\right)^2 \quad (6)$$

where $\beta = (1/2)\mu_{\mathrm{FE}} C_{\mathrm{OX}}(W_3/L_3)$, $V_{\mathrm{offset}} = \Delta V_{\mathrm{SCAN}}(C_{\mathrm{ST2}} \| C_{\mathrm{OV-T2}}/(C_{\mathrm{ST1}} + C_{\mathrm{ST2}} \| C_{\mathrm{OV-T2}}))$.

Equation (6) can be rewritten as

$$I_{\mathrm{OLED-OFF}} = I_{\mathrm{OLED-ON}} - 2\sqrt{\beta \cdot I_{\mathrm{OLED-ON}}} \cdot V_{\mathrm{offset}} + \beta \cdot V_{\mathrm{offset}}^2. \quad (7)$$

It should be noted that β in the second and third terms of (7) is temperature and mismatch sensitive, hence the $I_{\mathrm{OLED-OFF}}$ will be influenced by temperature, resulting in variation of R_{SCALE}. Fig. 8(a) shows the variation of R_{SCALE} with T3 size (W_3/L_3) mismatch. The R_{SCALE} changes by $\pm 1.2\%$ as the T3 width varies from 147 to 153 μm, corresponding to $\pm 2\%$ deviation. Also, according to (7), a higher offset voltage V_{offset} value, associated with a large $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$ ratio, will introduce greater scale-down ratio deviation $\Delta R_{\mathrm{SCALE}}$, Fig. 8(a). Finally, the $\Delta R_{\mathrm{SCALE}}$ in a high gray scale is not as large as that in a low gray scale because a high driving current can reduce its sensitivity to the geometric size mismatch.

Since the field-effect mobility μ_{FE} can be affected by device temperature, it is expected that β in (6) will also have temperature dependence [21], [22]. The temperature increasing from 20 to 70 °C will result in a higher field-effect mobility thus giving a rise in $\Delta R_{\mathrm{SCALE}}$ [Fig. 8(b)]. Also, a higher V_{offset} due to a larger $C_{\mathrm{ST2}}/C_{\mathrm{ST1}}$ ratio can cause an increase of $\Delta R_{\mathrm{SCALE}}$ not only in a high gray scale ($I_{\mathrm{OLED-ON}} = 8\ \mu$A) but also in a low gray scale ($I_{\mathrm{OLED-ON}} = 0.5\ \mu$A) regions. It should be mentioned that as the driving current increases, $\Delta R_{\mathrm{SCALE}}$ becomes smaller as a result of low temperature sensitivity achieved by a larger $I_{\mathrm{OLED-ON}}$.

D. Scan Line Delay in High-Resolution Display

The key factor to realize a large size and a high resolution display is to overcome the long resistance-capacitance (*RC*) time constant of the bus lines of which the resistance and capacitance are proportional to the size and the resolution of display panel. A large *RC* time constant can cause cross-talk and flicker effects due to the insufficient pixel charging across the large display area. Since the bus line resistance is due to intrinsic resistance

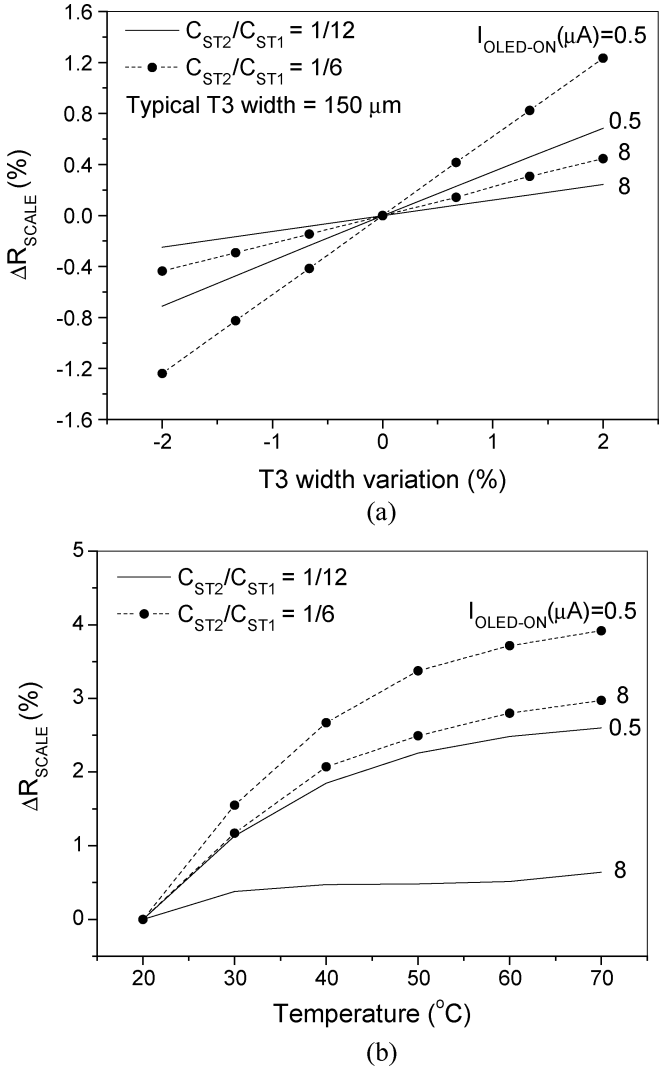
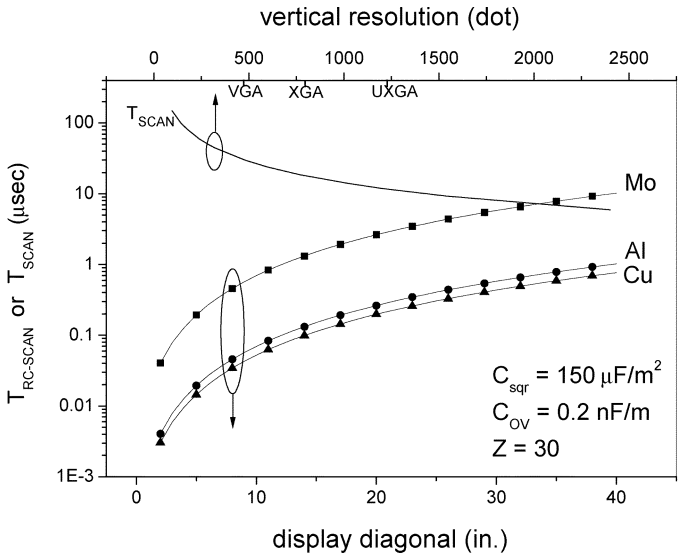


Fig. 8. (a) Variation of R_{SCALE} as a function of T3 width variation. (b) Influence of operation temperature upon R_{SCALE}.

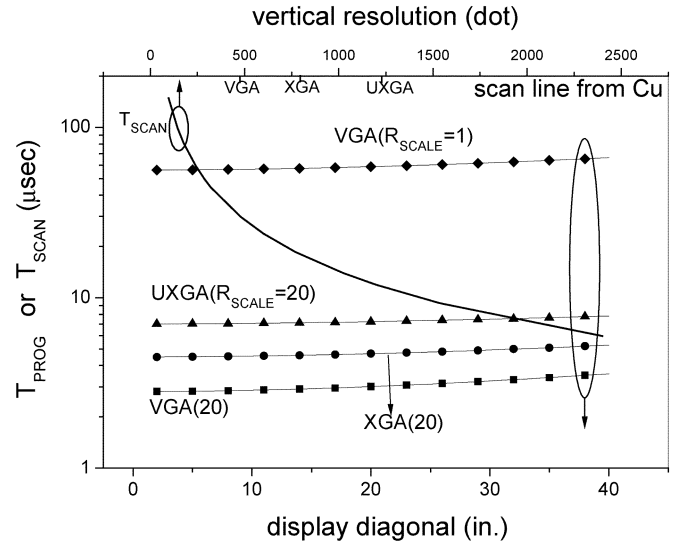
of bus lines materials and capacitance is associated with overlap capacitance of intersections and TFTs, the *RC* time constant of scan line $T_{\mathrm{RC-SCAN}}$ can approximately estimated by the following equation:

$$\begin{aligned} T_{;\mathrm{RC-SCAN}} &= (N_H \cdot R_{\mathrm{PIXEL}}) \cdot (N_H \cdot C_{\mathrm{PIXEL}}) \\ &= [N_H \cdot R_{\square} \cdot Z] \cdot \left[N_H \cdot C_{\square}\left(\frac{H}{N_H \cdot Z}\right)^2 + N_H \cdot C_{\mathrm{OV}} \cdot \frac{H}{N_H \cdot Z}\right] \\ &= \frac{R_{\square} \cdot C_{\square} \cdot H^2}{Z} + N_H \cdot C_{\mathrm{OV}} \cdot R_{\square} \cdot H \end{aligned} \quad (8)$$

where H, N_H, $C_{\square}$, $R_{\square}$, Z, and C_{OV} are display width, horizontal resolution, capacitance per meter square, sheet resistance, pixel pitch to bus line width ratio and TFT gate-to-drain/source overlap capacitance. According to (8), it is expected that a larger panel size and a higher display resolution will cause a longer $T_{\mathrm{RC-SCAN}}$ which can affect the data programming precision. For $C_{\square} = 150\ \mu\mathrm{F/m^2}$, $C_{\mathrm{OV}} = 0.2\ \mathrm{nF/m}$, and $Z = 30$,



(a)



(b)

Fig. 9. (a) Dependence of scan line *RC* time constant ($T_{\mathrm{RC-SCAN}}$) on display diagonal and the relationship between scan pulsewidth (T_{SCAN}) and resolution. (b) Data programming time (T_{PROG}) as a function of panel resolution with a scan line made from Cu.

the $T_{\mathrm{RC-SCAN}}$ as a function of display diagonal was calculated for UXGA resolution and for different metallurgy, e.g., copper ($R_{\square} = 0.075\ \Omega/\square$), aluminum ($0.1\ \Omega/\square$) and molybdenum ($1.0\ \Omega/\square$), Fig. 9(a). The scan pulsewidth T_{SCAN} shown as the solid line in Fig. 9(a) is also evaluated for 60-Hz frame rate and for different vertical resolutions. In general, the T_{SCAN} should be ten times larger than $T_{\mathrm{RC-SCAN}}$ to prevent the data programming error. Therefore, based on this simple calculation a high-resistance material such as molybdenum will limit the display size to about 12 in with UXGA resolution. A low-resistance material such as aluminum or copper is capable to reduce $T_{\mathrm{RC-SCAN}}$ in large size display up to 35 in or higher to acceptable value.

For AM-OLED, not only the $T_{\mathrm{RC-SCAN}}$ but also the data programming time (T_{DATA}) is important. The T_{DATA} is directly related to the data line capacitance C_{DATA}, storage capacitance C_{ST} and the programming current I_{DATA} and can be approximated by the following equation:

$$T_{\mathrm{DATA}} = \frac{V_{\mathrm{DATA}} \cdot (C_{\mathrm{DATA}} + C_{\mathrm{ST}})}{I_{\mathrm{DATA}}} \cong \frac{V_{\mathrm{DATA}} \cdot N_V \cdot C_{\square}}{R_{\mathrm{SCALE}} \cdot J_{\mathrm{OLED}}} \quad (9)$$

where $J_{\mathrm{OLED}} = (C_n \cdot C_E \cdot \pi \cdot L)/(C_V \cdot \eta)$.

Since the C_{ST} is much smaller than C_{DATA}, it can be neglected to simplify the calculation. In (9), V_{DATA} denotes the voltage at C_{ST} generated by the I_{DATA}, and N_V is the vertical resolution which can be obtained from N_H and aspect ratio of display. The constants C_n, C_{E}, and C_V depend on the refractive index and the emission spectrum of the OLED material [23]. Besides, L is the OLED luminance and η is device quantum efficiency [23]. It should be noted that the T_{DATA} in (9) is independent of the display size, and I_{DATA} is increased when the pixel area is increased to compensate for large C_{DATA} resulting from the increase of display size. In order to compare the proposed pixel electrode circuit with the conventional pixel circuit and to evaluate its performance, T_{PROG} is defined as $T_{\mathrm{RC-SCAN}} + T_{\mathrm{DATA}}$ to describe the total time requirement for accurate data programming. Fig. 9(b) shows T_{PROG} of proposed pixel as a function of display size for $V_{\mathrm{DATA}} = 5$ V, $C_n = 1.1$, $C_E = 0.44\ \mathrm{V}^{-1}$, $C_V = 427$ lm/W, $L = 100\ \mathrm{cd/m^2}$, $\eta = 5\%$, $C_{\square} = 150\ \mu\mathrm{F/m^2}$ and $R_{\mathrm{SCALE}} = 20$, along with the T_{PROG} of conventional pixel for $R_{\mathrm{SCALE}} = 1$. Without current scaling function ($R_{\mathrm{SCALE}} = 1$), a VGA display requires T_{PROG} of $60 \sim 70\ \mu$s to charge up the conventional pixel electrode circuit which is two times higher than a specific T_{SCAN} of display with VGA resolution. Therefore conventional pixel circuit is not applicable for a large size and a high resolution display device. By contrast, the proposed pixel circuit with the current scaling function can reduce the T_{PROG} significantly when a large I_{DATA} is used. Furthermore, as display resolution increases, the T_{PROG} for UXGA resolution (1600×1200) is of $8 \sim 9\ \mu$s which is lower than a specific T_{SCAN} of $10\ \mu$s even for display diagonal of 40 in. In summary, the proposed pixel electrode circuit with cascade storage capacitance has built-in current scaling capability that could allow to achieve a high resolution and a large size current-driven AM-OLED.

V. Conclusion

We proposed a pixel electrode circuit based on a-Si:H TFT technology and current driving scheme for speeding up the data programming time. We have shown that this circuit can achieve a high current scale-down ratio by a cascade structure of storage capacitors instead of increasing the size of TFT. In the proposed circuit, the ON-state data current of a factor of 10 larger than OLED current in OFF-state can be achieved. In contrast to the conventional current-driven and the current-mirror pixel electrode circuits, our pixel circuit can achieve the widest range of I_{AVG} for I_{DATA} ranging from 0.1 to 10 μA, hence both the current scaling function and the reasonable power consumption can be easily accomplished without substantially sacrificing the pixel aperture ratio. Furthermore, the threshold voltage variation of all TFT can also be compensated by the proposed circuit. The effects of device geometric size mismatch and temperature increase on pixel electrode circuit were analyzed, and it has been

concluded that they are within acceptable range of operation. The calculation of scan line delay and the required programming time indicated that the proposed pixel shows admirable capability to improve the data programming time. Even though the higher resolution limits the pixel pitch, the proposed pixel can be easily integrated with the top emission OLED without any aperture ratio restriction. Consequently, this new pixel electrode circuit has great potential for applications in a large size, a high resolution a-Si:H TFT AM-OLEDs.

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