Mechanism for Slow Switching Effect in Advanced Low-Voltage, High-Speed $Pb(Zr_{1-x}Ti_x)O_3$ Ferroelectric Memory

Ching-Wei Tsai, *Member, IEEE*, Sheng-Chih Lai, *Student Member, IEEE*, C. T. Yen, Hao-Ming Lien, Hsiang-Lan Lung, *Member, IEEE*, Tai-Bor Wu, Tahui Wang, *Senior Member, IEEE*, Rich Liu, *Senior Member, IEEE*, and Chih-Yuan Lu, *Fellow, IEEE*

***Abstract*—Slow-switching effect in PZT ferroelectric memory under low-voltage and high-speed operation is observed. The slow-switching effect becomes worse at lower operation voltage and elevated temperature. This effect significantly reduces the sensing margin and causes severe reliability issue for advanced ferroelectric memory, particularly for low-voltage and high-speed applications. This slow-switching effect is believed to be attributed to slowing down of polarization switching caused by band bending from Schottky built-in potential at the electrode/ferroelectric interface. The proposed mechanism is supported by the polarity dependence in an asymmetric LNO/PZT/Pt sample.**

***Index Terms*—Ferroelectric memory, Schottky built-in potential, slow-switching effect.**

I. Introduction

FERROELECTRIC random access memory (FeRAM) has attracted much attention due to its nonvolatility, high read/write speed, low operation voltage, low power consumption and high endurance [1]–[4]. Additionally, FeRAM can be more easily embedded as part of a larger integrated circuit to provide system-on-a-chip solutions to various applications than EEPROM and Flash memories because the ferroelectric capacitor can be stacked over the transistors at the backend processes [5], [6]. However, several reliability issues seriously limit the applications of FeRAM, such as fatigue [7], imprint [8] and decrease of switching charges [9]–[11] etc. Fatigue is a gradual degradation of switching polarization after repeated cycles, because of the electro-migration of oxygen vacancies to form extended defects capable of pinging domains, or formation of interfacial layers between metal electrode and ferroelectric [7]. Imprint is the inability to switch a capacitor to the opposite state after being for some time/temperature stress programmed in one state, resulting in a write error of the memory cell. In general, two mechanisms are proposed to explain the imprint effect of ferroelectric capacitor, which are the alignment of defect dipoles and the charge trapping near electrode/ferroelectric interface [8].

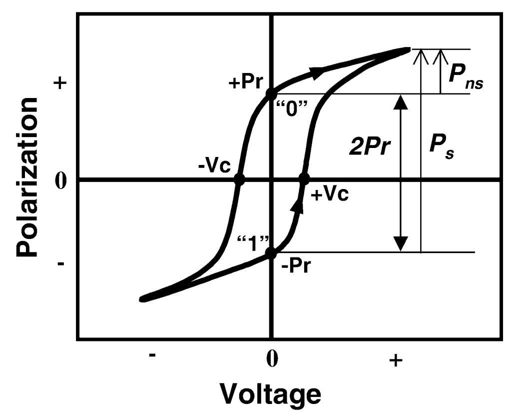


Fig. 1. Schematic hysteresis loop of a ferroelectric capacitor. Two remanent polarization states (+Pr and −Pr) exist in a ferroelectric capacitor after the applied voltage is removed. P_s and $P_{\rm ns}$ denote the switching polarization and nonswitching polarization, respectively, and the difference between P_s and $P_{\rm ns}$ is denoted by 2Pr.

In a ferroelectric capacitor, there are two remanent polarization states, i.e., +Pr for "0" state and −Pr for "1" state as illustrated in Fig. 1, which can be switched alternatively by the applied electric field. When the voltage across the ferroelectric capacitor is 0 V, the capacitor supposes to be at one of the two stable states: "1" or "0". Therefore, a ferroelectric capacitor along with a transistor for isolation can be a memory cell of FeRAM (Fig. 2). In a conventional bit-line driven read-operation, the bit line (BL) is pre-charged to a certain level; the bit line bar (/BL) is set to the reference voltage ($V_{\rm ref}$); plate line (PL) is grounded. Subsequently, the word line (WL) is turned on. If the ferroelectric capacitor is at the "0" state, the polarization will be switched from +Pr to −Pr, thus reducing BL voltage. On the contrary, when the ferroelectric capacitor is at "1" state, the polarization is not switched and fewer charges are changed from PL. The sensed BL voltage of "1" state is therefore higher than that of "0" state. After choosing appropriate $V_{\rm ref}$, the data in a ferroelectric capacitor can be read-out by the sense amplifier.

Therefore, the sensing window of FeRAM is attributed to the switching polarization from domain reversal, and a larger remanent polarization (Pr) usually offers a larger sensing window for

Manuscript received September 3, 2004; revised January 31, 2005.
C. W. Tsai and T. Wang are with the Macronix International Company Ltd., Hsinchu 300, Taiwan, R.O.C., and are also with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, R.O.C.
S. C. Lai is with the Macronix International Company Ltd., Hsinchu 300, Taiwan, R.O.C., and is also with the Department of Materials Science and Engineering, National Tsing-Hua University, Hsinchu, Taiwan, R.O.C. (e-mail: sclai@mxic.com.tw).
C. T. Yen, H. M. Lien, S. L. Lung, R. Liu, and C.-Y. Lu are with the Macronix International Company Ltd., Hsinchu 300, Taiwan, R.O.C.
T. B. Wu is with the Department of Materials Science and Engineering, National Tsing-Hua University, Hsinchu, Taiwan, R.O.C.
Digital Object Identifier 10.1109/TDMR.2005.846977

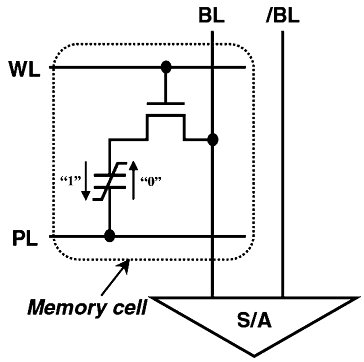


Fig. 2. Schematic diagram of a 1T/1C FeRAM cell.

FeRAM. The difference between switching polarization (P_s) and nonswitching polarization $(P_{\rm ns})$, i.e., 2Pr as illustratively denoted in Fig. 1, is thus an important index to represent the sensing window of FeRAM. The required charge for 1T/1C FeRAM operation is $\sim$85 fC/cell ($\Delta V_{\rm BL} \sim 200$ mV) [2], which can be obtained either by increasing the effective surface area of the capacitor electrodes or by raising the switching polarization. However, the switching polarization was reported to decrease with shortened operation pulse width or lower operation voltage [9]–[11]. This effect severely degrades the operation speed and limits the scaling ability for high-density applications. It is significant to improve this issue because low-voltage and high-speed operation is imperative in future generation memories, especially for low power systems such as contactless smart card, radio-frequency tag (RF tag) and 3 G cellular phone applications. With regard to the decrease of switching charges during low-voltage and high-speed operation, some solutions to this effect were suggested, such as lanthanum doped $Pb(Zr_{1-x}\,Ti_x)O_3$ (PZT) [9] and modified Zr/Ti ratio in PZT film [10], but the mechanism remains ambiguous.

In this work, the decrease of switching charges in PZT ferroelectric capacitor at low-voltage and high-speed operation is comprehensively studied. Symmetric Pt/PZT/Pt and asymmetric LNO/PZT/Pt structure are compared and a mechanism to explain this phenomenon is also proposed.

II. Experimental

The PZT films were deposited by the sol-gel and the sputtering methods on Pt (150 nm)/Ti (50 nm)/SiO_2(150 nm)/Si substrates with thickness of 220 nm and 170 nm, respectively. The compositions of the sol-gel and the sputtered PZT films are both $Pb(Zr_{0.4}, Ti_{0.6})O_3$. Platinum top electrodes of 60 nm in thickness and 1.76×10^{-4} cm^2 in area were sputtered and patterned by the lift-off process to have a symmetric Pt/PZT/Pt structure. The $LaNiO_3$ (LNO) top electrodes of the same dimensions were also sputtered at $\sim$350°C and patterned by wet etching processes to produce an asymmetric LNO/PZT/Pt structure. Before electrical measurement, a pre-polarization pulse with 1 sec. pulse duration generated by Agilent 8110 A pulse generator was applied to assure the initial polarization state of PZT ferroelectric capacitor was fully programmed and was opposite to the programming state. The switching polarization was measured by an aixACCT TF Analyzer 2000, where the duration

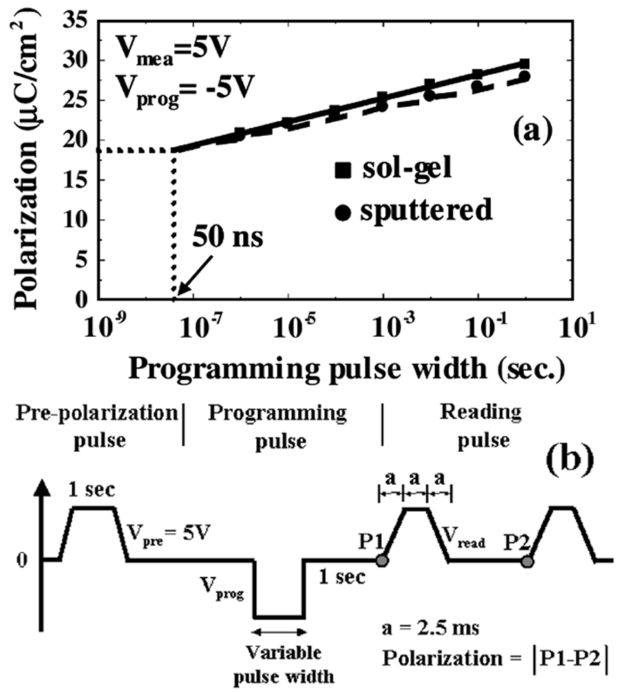


Fig. 3 (a) Effect of programming pulsewidth on switching polarization for Pt/PZT(sol-gel)/Pt and Pt/PZT(sputtered) /Pt ferroelectric capacitors. (b) Applied pulse sequence for switching polarization measurement. The driving pulses are applied on the top electrode.

of measurement pulses was artificially set at 2.5 ms to ensure the quality of observation. The transient polarization current is measured by Agilent 4156 C. The driving pulses were applied on the top electrode.

III. Results and Discussion

Fig. 3(a) shows a typical result of degradation in switching polarization with shortening the programming pulse width. Both of the sol-gel and the sputtered PZT films exhibit the same characteristic. The applied pulse sequence for the measurement of switching polarization is depicted in Fig. 3(b). The switching polarization in Fig. 3(a) was derived from the difference between P1 and P2 states in Fig. 3(b). At a programming pulsewidth of 50 ns in 5 V operation, the achievable polarization in both samples is estimated at $\sim$18 μC/cm^2, which is sufficient for high-speed FeRAM applications. However, the polarization-charge loss becomes much more serious when the programming voltage $(V_{\rm prog})$ is reduced, as shown in Fig. 4. The switching polarization is deteriorated to 2.8 μC/cm^2, i.e., $\sim$90% degradation, at $V_{\rm prog} = 2$ V with the programming pulsewidth of 1 μs. Therefore, this polarization-charge loss significantly impedes FeRAM for low-voltage and high-speed applications.

Since the polarization switching strongly depends on the programming pulse width, it would be interesting to clarify the switching behavior from the aspect of transient current in programming. The transient current at each program voltage in a PZT ferroelectric capacitor is shown in Fig. 5. Because this I-t curve is measured after the pre-polarization, the programming pulsewidth represents the entire program transient behavior. To our knowledge, polarization should be switched

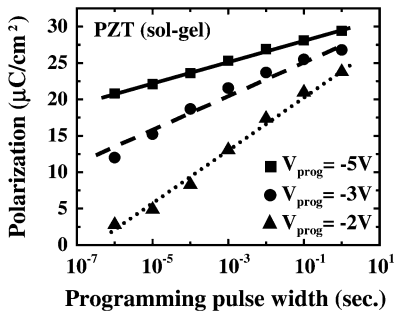


Fig. 4. Switching polarization as a function of programming pulsewidth with various program pulse voltages, where the measurement voltage $V_{\rm mea} = 5$ V.

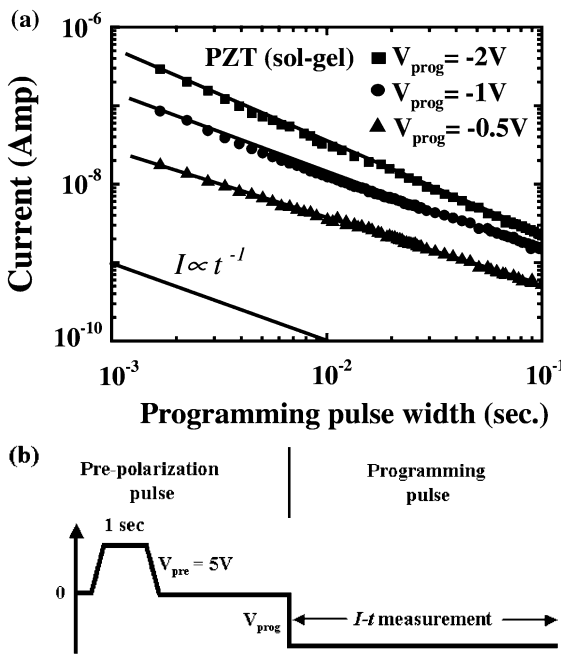


Fig. 5. (a) Plot of transient current versus programming pulsewidth at various programming voltages. (b) Pulse sequence for the measurement of transient current.

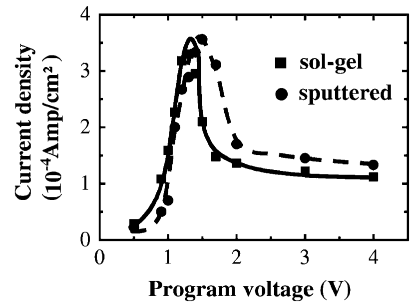


Fig. 6. J-V curves derived from Fig. 5 for the sol-gel and the sputtered PZT samples. The current value chosen is that at $t = 10$ ms.

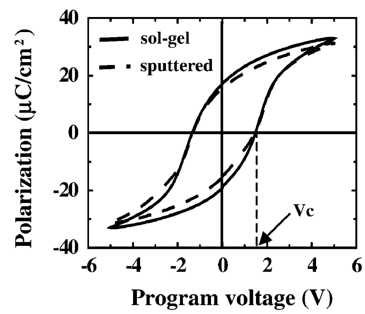


Fig. 7. Hysteresis loops for Pt/PZT(sol-gel)/Pt and Pt/PZT (sputtered)/Pt ferroelectric capacitors.

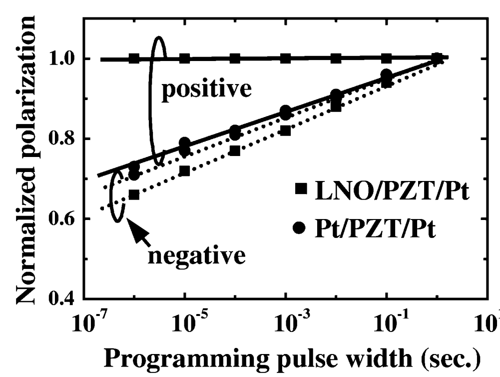


Fig. 8. Polarity dependence of normalized switching polarization on the programming pulse width. The polarization switching charges are normalized to the polarization charges of 1 sec programming. Positive and negative polarity refers to the programming voltages ($V_{\rm prog}$) of ± 5 V on the top electrode.

completely within nanoseconds [3], [4]. However, in this figure, transient current at each program voltage is observed and follows a power law standing for polarization switching, i.e., Curie–von Schweidler behavior $(I \propto t^{-n})$ with n close to unity [12], [13]. Current transferred charges, integrated from this I-t curve, increase and exhibit a logarithmic function with programming pulsewidth $(Q \propto \log t)$. These features on I-t curve strongly correlate with the polarization-charge loss in Fig. 4. That is, the larger the programming pulse width, the more transferred charges on I-t and the less polarization loss it achieves. Besides, the power law dependence suggests the polarization switching in the ferroelectric capacitor is slow and even slower than 1 ms.

To confirm the polarization charge loss is due to a portion of polarization slow-switching, the programming voltage dependence of transient current is obtained (Fig. 6). In this figure, the current derived from $t = 10$ ms reveals a turn-around feature. The programming voltage at the maximum switching current is around 1.5 V and is close to the coercive voltage (V_c) of both films (Fig. 7). At $|V_{\rm prog}| \gg V_c$, a large portion of polarization switching is finished within 100 ns, but a small part remains at the time over 1 ms. The slow-switching part thus contributes to a transient current between 1 ms and 100 ms (Fig. 5). As the program voltage is reduced and approaching V_c, slow-switching part becomes to play a significant role, and the transient current (derived from $t = 10$ ms) therefore has its maximum at around $|V_{\rm prog}| \sim V_c$. Once when $|V_{\rm prog}| < V_c$, the overall switching charges are substantially decreased and the slow-switching component within is reduced correspondingly. The turn-around feature for the transient current (Fig. 6) cannot be simply explained by carrier trapping and de-trapping from interfaces [15] since such mechanism should be a monotonic function of the programming voltage.

Additionally, we also studied the slow-switching effect in an asymmetric LNO/PZT/Pt sample [16], compared with a

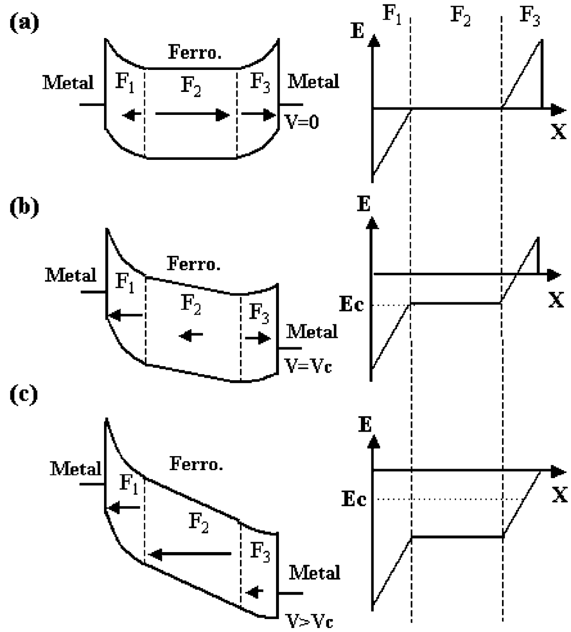


Fig. 9. Schematic band diagram and the corresponding electric field distribution in a ferroelectric capacitor. The ferroelectric film is pre-polarized at $V < -V_c$. (a) At $V = 0$, remanent polarization is contributed by F2 and F3; (b) at $V = V_c$, the electric field in F2 is around E_c (coercive electric field). (c) At $V > V_c$, F1 and F2 regions are switched while the electric field in a large portion of F3 is still below E_c.

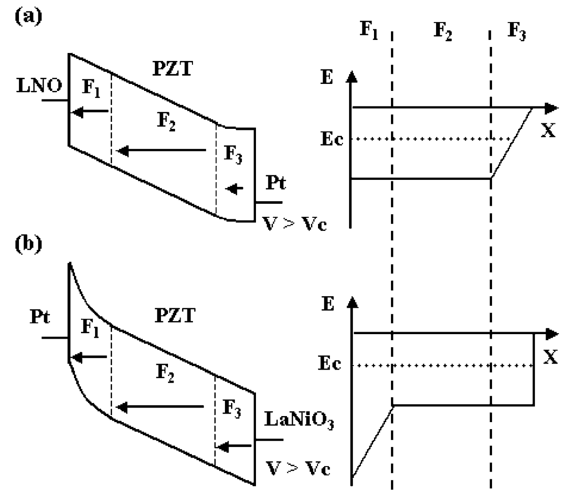


Fig. 10. Schematic band diagram and the corresponding electric field distribution at $V > V_c$ in an asymmetric LNO/PZT/Pt ferroelectric capacitor. (a) The LNO electrode is driven negatively (or platinum electrode is driven positively) and the electric field in a large portion of F3 is still below E_c. (b) The LNO electrode is driven positively and no region is below E_c.

symmetric Pt/PZT/Pt structure. As shown in Fig. 8, there is no polarity dependence of the applied bias on the switching polarization, and both polarities of the applied bias reveal the slow-switching effect in the case of symmetric Pt/PZT/Pt structure. However, in the case of asymmetric LNO/PZT/Pt structure, when the LNO-electrode is driven positively, the polarization reversal is independent of the programming pulse width. In general, conducting oxide electrodes and ferroelectric films possess smaller work function difference [14] because the work function of Pt is very high. The formation of interfacial layer with low dielectric constant at a LNO/ferroelectric interface [22] also reduces the width of depletion region through the formula [21]. These possibly lead to insignificant Schottky effect (smaller slow-switching region) for LNO/PZT compared to the Pt/PZT interface.

Based on this understanding, we propose that the slow-switching effect is mainly caused by band bending from the Schottky built-in potential at the electrode/ferroelectric interface. In a ferroelectric capacitor, the ferroelectric is not an ideal insulator but displays some semiconductor properties of n-type resulting from the electron donors of oxygen vacancies. As a result, a Schottky barrier, resulting from the migration of electrons from the ferroelectric film to the electrode due to the work function difference, exists at the metal electrode/ferroelectric interface [15], [17]–[20]. Since the speed of domain reversal decreases at low electric field [12], the local electric field formed by Schottky built-in potential should increase the polarization switching time. The energy band structure and the corresponding electric field distribution within the PZT film are illustrated in Fig. 9. The PZT film is divided into three regions designated as F_1, F_2, and F_3 and is pre-polarized toward the right direction. At $V = 0$ [Fig. 9(a)], the F_1 part suffers a built-in electric field against its original direction, and therefore the polarization in F_1 is slightly reversed. When the applied voltage (V) increases to the coercive voltage (V_c) [Fig. 9(b)], the electric field in most of the PZT film including F_2 and F_3 is low. Therefore, the speed of domain reversal slows down, and the switching current at the coercive voltage at $t = 10$ ms is at its maximum [Fig. 6]. When the applied voltage further increases to $V > V_c$ [Fig. 9(c)], the switching speed in F_2 region is fast hereafter, and the component for slow-switching is contributed only by part of F_3. The switching current therefore decreases with voltage from 1.5 V to 4 V as observed in Fig. 6.

Note that the LNO electrode has no impact at negative program voltage [Fig. 8], since in this case the Schottky barrier at Pt/PZT interface still makes F_3 region slow-switching [Fig. 10(a)]. However, the slow-switching region is smaller or eliminated as the LNO electrode is driven positively [Fig. 10(b)]. Actually, any other factors responsible for slow-switching at the electrode/ferroelectric interface are possible. Among them, we believe that the formation of Schottky potential plays a major role for the slow-switching due to the significant improvement by LNO electrode. Here, since the Schottky potential builds up a depletion region following the formula [21], several hundred angstroms in F_1 and F_3 can be roughly estimated by parameters of a typical PZT film. Accordingly, the depletion width can be reduced through three ways: 1) small dielectric constant of a ferroelectric capacitor; 2) high doping concentration in a ferroelectric capacitor; and 3) low Schottky potential barrier at interface. It is our next work to provide quantitative calculations by incorporating slow-switching components in a PZT ferroelectric capacitor and then considering the effect of electric field distribution on the switching behavior.

The switching behavior at different temperature is also investigated. Fig. 11 shows the slow-switching effect becomes more serious at higher temperatures, and Fig. 12 also shows that the

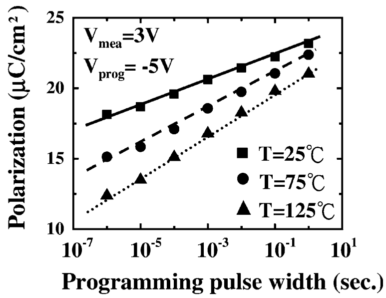


Fig. 11. Effect of programming pulsewidth on switching polarization at different operation temperatures.

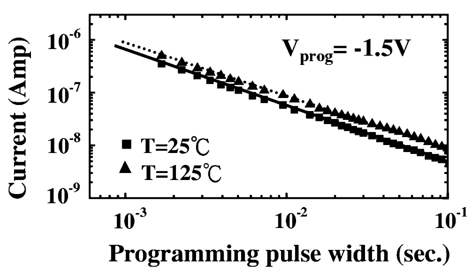


Fig. 12. Impact of operation temperature on the transient polarization switching current.

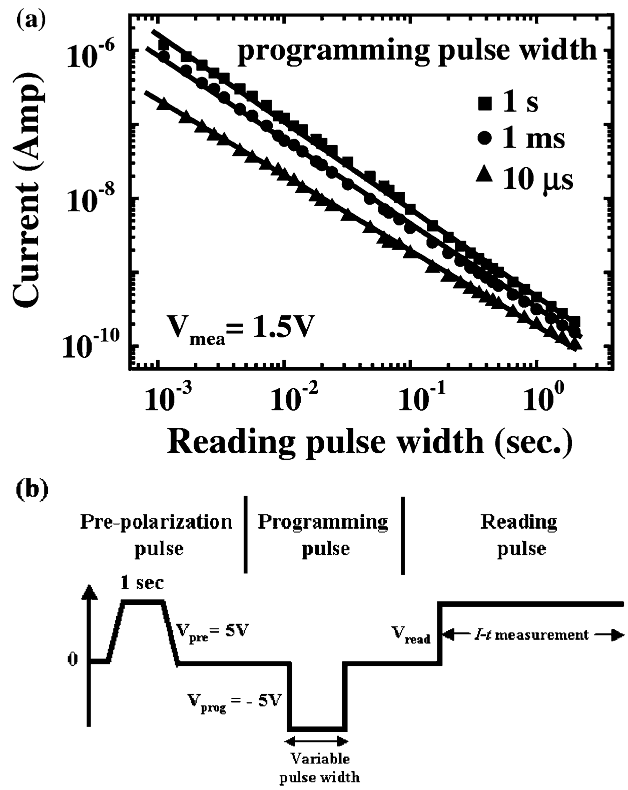


Fig. 13. (a) Plot of transient switching current versus reading pulsewidth with various programming pulse width. (b) Pulse sequence for the measurement of transient switching current.

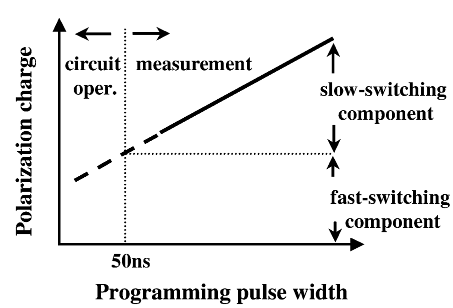


Fig. 14. Schematic diagram of the programming pulsewidth dependence on the switching polarization charge. Slow-switching and fast-switching components are identified. The time range for circuit operation is also noted.

transient switching current increases with higher temperature. At elevated temperature, the dielectric constant of the PZT is expected to increase [18], and the interface region (F_3 in Fig. 9) induced by the Schottky built-in potential should be enlarged accordingly [21]. The enlarged interface region at high temperature thus leads to larger transient current and worse slow-switching effect.

The slow-switching effect can also be expected when the reading pulsewidth is shortened (Fig. 13). The read transient current shows nearly identical dependence with the program transient current. This is because the sensed polarization charges (integrated from the I-t curve) also increase with longer reading pulse width. Since the read operation of 1T/1C FeRAM is destructive and is the inverse of program operation, slow-switching in the read operation may in the same way deteriorate the amount of sensed polarization charges and the resulting sensing margin. Thus the slow-switching will affect both programming and reading speed.

Fig. 14 illustrates the roles of slow-switching and fast switching components (shorter than 50 ns) through the programming time range. During high-speed writing and reading, only the polarization charges with fast switching characteristics can contribute to the sensing window of FeRAM. The reduction of Schottky built-in potential not only is beneficial to remove the slow-switching component for low-voltage and high-speed applications but also is effective in suppressing the decrease of remanent polarization and the increase of coercive electric filed caused by an aggressive thickness-scaled ferroelectric capacitor [17], [18].

IV. Conclusion

A slow-switching model induced by the Schottky built-in potential is proposed. This built-in potential reduces the local electric field and thus slows down the switching speed of domain reversal. The Schottky potential effect is evident in the polarity dependence of LNO/PZT/Pt structure and in the temperature dependence of slow-switching effect. To minimize the slow-switching effect in low-voltage and high-speed operation, electrodes with low Schottky barrier to PZT film is recommended.

Acknowledgment

The authors would like to thank Dr. C. H. Chien from National Nano Device Laboratories and Dr. C. L. Liu from Department of Materials Science and Engineering, National

Tsing-Hua University, Hsinchu, Taiwan, for their support of the sample preparation and for fruitful discussion.

REFERENCES

[1] S. Y. Lee and K. Kim, "Future 1T1C FRAM technologies for highly reliable, high density FRAM," in *IEDM Tech. Dig.*, 2002, pp. 547–550.

[2] Y. J. Song, H. J. Joo, N. W. Jang, H. H. Kim, J. H. Park, H. Y. Kang, S. Y. Lee, and K. Kim, "Highly manufacturable and reliable 32 Mb FRAM technology with novel BC and capacitor cleaning process," in *Symp. VLSI Tech. Dig.*, 2003, pp. 169–170.

[3] Y. Nagano *et al.*, "0.18 μm SBT-based embedded FeRAM operating at a low voltage of 1.1 V," in *Symp. VLSI Tech. Dig.*, 2003, pp. 171–172.

[4] S. H. Oh *et al.*, "Noble FeRAM technologies with MTP cell structure and BLT ferroelectric capacitors," in *IEDM Tech. Dig.*, 2003, pp. 34.5.1–34.5.4.

[5] R. E. Jones Jr., "Ferroelectric nonvolatile memories for embedded applications," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1998, pp. 431–438.

[6] T. Mira *et al.*, "An embedded FeRAM macro cell for a smart card microcontroller," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1998, pp. 439–442.

[7] M. Dawber and J. F. Scott, "A model for fatigue in ferroelectric perovskite thin films," *Appl. Phys. Lett.*, vol. 76, pp. 1060–1062, 2000.

[8] M. Grossmann, O. Lohse, D. Bolten, U. Boettger, R. Waser, W. Hartner, M. Kastner, and G. Schindler, "Lifetime estimation due to imprint failure in ferroelectric $SrBi_2Ta_2O_9$ thin films," *Appl. Phys. Lett.*, vol. 76, pp. 363–365, 2000.

[9] B. Yang, T. K. Song, S. Aggarwal, and R. Ramesh, "Low voltage performance of $Pb(Zr,Ti)O_3$ capacitors through donor doping," *Appl. Phys. Lett.*, vol. 71, pp. 3578–3580, 1997.

[10] K. Aoki, T. Sakoda, and Y. Fukuda, "Characterization of switching properties of lead-zirconate-titanate thin films in Ti-rich phase," *Jpn. J. Appl. Phys.*, vol. 37, pp. L522–L524, 1998.

[11] N. Tanisake, K. Itani, K. H. Kim, E. Tokumitsu, and H. Ishiwara, "Study on gradual reversal of polarization in ferroelectric PZT thin films for adaptive-learning MFSFET applications," *Integrat. Ferroelectr.*, vol. 6, pp. 69–80, 1995.

[12] O. Lohse, M. Grossmann, U. Boettger, and D. Bolten, "Relaxation mechanism of ferroelectric switching in $Pb(Zr,Ti)O_3$ thin films," *J. Appl. Phys.*, vol. 89, no. 4, pp. 2332–2336, 2001.

[13] A. K. Tagantsev, A. L. Kholkin, E. L. Colla, K. G. Brooks, and N. Setter, "Effect of ferroelectric polarization on current response of PZT thin films," *Integrat. Ferroelectr.*, vol. 10, pp. 189–204, 1995.

[14] C. S. Hwang, B. T. Lee, C. S. Kang, J. W. Kim, K. H. Lee, H. J. Cho, H. Horii, W. D. Kim, S. I. Lee, and Y. B. Roh, "A comparative study on the electrical conduction mechanisms of $(Ba_{0.5}, Sr_{0.5})TiO_3$ thin films on Pt and IrO_2 electrodes," *J. Appl. Phys.*, vol. 83, no. 7, pp. 3703–3713, 1998.

[15] Y. Fukuda, K. Numata, K. Aoki, and A. Nishimura, "Origin of dielectric relaxation observed for $Ba_{0.5}Sr_{0.5}TiO_3$ thin-film capacitor," *Jpn. J. Appl. Phys.*, vol. 35, pp. 5178–5180, 1996.

[16] S. L. Lung, C. L. Liu, S. S. Chen, S. C. Lai, C. W. Tsai, T. T. Sheng, T. Wang, S. Pan, T. B. Wu, and R. Liu, "Low temperature epitaxial growth of PZT on conductive perovskite $LaNiO_3$ electrode for embedded capacitor-over-interconnect (COI) FeRAM application," in *IEDM Tech. Dig.*, 2001, pp. 275–278.

[17] A. K. Tagantsev, C. Z. Pawlaczyk, K. Brooks, and N. Setter, "Built-in electric field assisted nucleation and coercive fields in ferroelectric thin films," *Integrat. Ferroelectr.*, vol. 4, pp. 1–12, 1994.

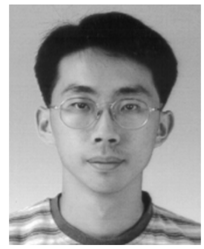
[18] C. H. Lin, P. A. Friddle, C. H. Ma, A. Daga, and H. Chen, "Effects of thickness on the electrical properties of metal-organic chemical vapor deposition $Pb(Zr,Ti)O_3$ (25–100 nm) thin films on $LaNiO_3$ buffered Si," *J. Appl. Phys.*, vol. 90, no. 3, pp. 1509–1515, 2001.

[19] S. O. Park, C. S. Huang, H. J. Cho, C. S. Kang, H. K. Kang, S. I. Lee, and M. Y. Lee, "Fabrication and electrical characterization of $Pt/(Ba,Sr)TiO_3/Pt$ capacitors for ultralarge-scale integrated dynamic random access memory applications," *Jpn. J. Appl. Phys.*, vol. 35, pp. 1548–1552, 1996.

[20] J. F. Scott, M. Azuma, C. A. P. de Araujo, L. D. McMillan, M. C. Scott, and T. Roberts, "Dielectric breakdown in high-ε films for ULSI DRAMs: II. Barium-strontium titanate ceramics," *Integrat. Ferroelectr.*, vol. 4, pp. 61–84, 1994.

[21] S. M. Sze, *Physics of Semiconductor Devices*, 2nd ed. New York: Central Book Co., 1985, p. 77.

[22] C. M. Chu and P. Lin, "Electrical properties and crystal structure of $(Ba,Sr)TiO_3$ films prepared at low temperature on a $LaNiO_3$ electrode by radio-frequency magnetron sputtering," *Appl. Phys. Lett.*, vol. 70, pp. 249–251, 1997.



Ching-Wei Tsai (S'01–M'03) was born in Tao-Yuan, Taiwan, R.O.C. He received the B.S. degree in electronics engineering from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C., in 1998. He is currently pursuing the Ph.D. degree in electronics engineering at the same university.

His research interests include ultrathin gate dielectric reliability of MOSFETs and nonvolatile memory devices such as flash memories and FeRAMs.

Sheng-Chih Lai (S'04) received the B.S. and M.S. degrees in materials science and engineering from National Tsing-Hua University, Taiwan, R.O.C., in 1999 and 2001, respectively, where he is currently pursuing the Ph.D. degree.

He is also a Senior Engineer with Emerging Central Lab, Macronix, Taiwan. His research interests include nonvolatile memory devices such as flash memories and FeRAMs.

C. T. Yen received the M.S. degree in electrophysics from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C.

Her research interests include device physics and modeling.

Hao-Ming Lien was born in Taipei, Taiwan, R.O.C. He received the M.S. degree in materials science and engineering from National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. in 1995.

His research interests include nonvolatile memory devices such as flash memories and FeRAMs.

Hsiang-Lan Lung (S'02–M'03) received the B.S. degree from Feng Chia University, Taichung, Taiwan, R.O.C., the M.S. degree from National Cheng Kung University, Tainan, Taiwan, and the Ph.D. degree from National Tsing Hua University, Hsinchu, Taiwan, in 1992, 1996, and 2003, respectively, all in materials science and engineering.

He joined Macronix International, Hsinchu, Taiwan, in 1996. Since then, he has engaged in research and advanced technology development of CMOS logic, embedded SRAM, embedded MROM, embedded Flash, NROM, FeRAM, and phase-change memory. He is currently the chief for the Nano-Device R&D department and in charge of the R&D work for advanced nonvolatile memory technology. He has published 14 technical papers and has been granted 26 international patents.

Tai-Bor Wu received the B.S. and M.S. degrees from National Tsing Hua University, Hsinchu, Taiwan, R.O.C., and the Ph.D. degree from Northwestern University, Evanston, IL, in 1973, 1975, and 1982, respectively.

In 1982, he joined the Department of Materials Science and Engineering, National Tsing Hua University, Taiwan. He is a Professor of the Department of Materials Science and Engineering, National Tsing-Hua University, and he is also the Chair of the Materials Science Center, Hsinchu, Taiwan. He is currently involved in research of ferroelectric thin films for NVRAM and microwave tunable devices application as well as high-κ gate oxide for nano-CMOS applications.

Tahui Wang (S'85–M'86–SM'94) was born in Taoyuan, Taiwan, R.O.C., on May 3, 1958. He received the B.S.E.E. degree from National Taiwan University, Taipei, in 1980 and the Ph.D. degree in electrical engineering from the University of Illinois, Urbana-Champaign, in 1985.

From 1985 to 1987, he was with Hewlett-Packard Laboratories, Palo Alto, CA, where he was engaged in the development of GaAs HEMT devices and circuits. Since 1987, he has been with the Department of Electronics Engineering, National Chiao-Tung University, Hsinchu, Taiwan, where he is currently a Professor. His research interests include hot carrier phenomena characterization and reliability physics in VLSI devices, RF CMOS devices and nonvolatile semiconductor devices.

Dr. Wang was granted the Best Teacher Award by the Ministry of Education, R.O.C. He has served as technical committee member of many international conferences, among them IEDM, IRPS, and VLSI-TSA. His name was listed in *Who's Who in the World*.

Rich Liu (M'87–SM'01) received the Ph.D. degree in materials science from the University of Illinois, Urbana-Champaign, in 1977.

He joined Bell Laboratories in 1979. His research interests covered e-beam lithography systems, electronic materials, CMOS devices and technology, interconnect technology, embedded memories and nonvolatile memories. He joined Macronix International, Taiwan, 2001.

Dr. Liu has served on program committees of many IEEE conferences, and was a past editor of IEEE ELECTRON DEVICE LETTERS.

Chih-Yuan Lu (M'78–SM'84–F'95) received the B.S. degree from National Taiwan University, Taipei, Taiwan, R.O.C., in 1972, and the M.A., M.Ph., and Ph.D. degrees from Columbia University, New York, NY, in 1974, 1975, and 1977, respectively, all in physics.

From 1978 to 1983, he was an Associate Professor and was promoted to Full Professor of National Chiao-Tung University, Hsinchu, Taiwan. In 1983, he was with North Carolina State University, Raleigh, as a Visiting Associate Professor and Adjunct Research Staff Member of the Microelectronic Center of North Carolina (MCNC), Research Triangle Park. In 1984, he joined AT&T Bell Laboratories, where he was engaged in very high voltage bipolar-CMOS-DMOS (BCDMOS) IC technology for telecommunication applications, CMOS DRAM technology, laser programmable redundancy, and submicron CMOS ULSI technology. He joined the Electronics Research and Service Organization, Industrial Technology Research Institute, Hsinchu, (ERSO/ITRI) in late 1989 as a Deputy General Director responsible for semiconductor and integrated circuit operation, especially the Grand Submicron Project. This project later successfully developed Taiwan's first 8-in CMOS submicron manufacturing technology with high-density DRAM/SRAM as technology vehicles. In late 1994, he was the cofounder of Vanguard International Semiconductor Corporation, Hsinchu, which is a spinoff memory IC Company from ITRI's Submicron Project. He was the Vice President of Operations, Vice President of Research and Development, and later President from 1994 to 1999. He brought Vanguard from a research and development laboratory to a U.S. $400 million sales company and went IPO in 1998. He is currently Chairman and CEO of Ardentec Corporation, Hsinchu, a VLSI testing service company, and also serves Macronix International Company (MXIC), Ltd., Hsinchu, as a Senior Vice President/CTO. He led MXIC's technology development team to successfully achieve the state-of-the-art nonvolatile memory technology and embedded SoC technology, now, MXIC is the top nonvolatile semiconductor company in Taiwan. He has published more than 100 technical papers and has been granted 123 international patents. He also authored more than 30 articles in science education and R&D policy in magazines and newspapers. He served as the President of *Science Monthly* from 1978 to 1983.

Dr. Lu was the Executive Secretary and Managing Director of the Board and Board Director since 1998 for the Physical Society of R.O.C. from 1981 to 1984. He has been Vice-Chairman and then Chairman of IEEE Electron Devices Society, Taipei Chapter, from 1991 to 1996, and Board Director and Supervisor of IEEE Section since 1996. He is a member of many honor societies, including Sigma Pi Sigma, Phi Tau Phi, and Phi Lambda. He is a life member of the American Physical Society, the Physical Society of R.O.C., the Chinese Institute of Engineers, and CIE-USA. He received the National Science and Technology Achievement Award from the Prime Minister of Taiwan, R.O.C., in 1994. In 1995, he was awarded the National Invention Award, and in 2002, he was awarded the most prestigious semiconductor award in Taiwan—the Pan Wen Yuan Award.