Overview of On-Chip Electrostatic Discharge Protection Design With SCR-Based Devices in CMOS Integrated Circuits

Ming-Dou Ker, *Senior Member, IEEE,* and Kuo-Chun Hsu, *Member, IEEE*

***Abstract*—An overview on the electrostatic discharge (ESD) protection circuits by using the silicon controlled rectifier (SCR)-based devices in CMOS ICs is presented. The history and evolution of SCR device used for on-chip ESD protection is introduced. Moreover, two practical problems (higher switching voltage and transient-induced latchup issue) limiting the use of SCR-based devices in on-chip ESD protection are reported. Some modified device structures and trigger-assist circuit techniques to reduce the switching voltage of SCR-based devices are discussed. The solutions to overcome latchup issue in the SCR-based devices are also discussed to safely apply the SCR-based devices for on-chip ESD protection in CMOS IC products.**

***Index Terms*—Electrostatic discharge (ESD), ESD protection circuits, latchup, silicon controlled rectifier (SCR).**

I. Introduction

ELECTROSTATIC DISCHARGE (ESD) phenomenon is originated from the transfer of electrostatic charges between two objects with different electrical potentials, which results in damage to integrated circuits (ICs) due to large energy dissipation in an extremely short time of less than 150 ns. ESD failure will become more serious reliability concern in nanoscale CMOS IC products. Common ESD failures are catastrophic, leading to immediate malfunction of IC chips caused by either thermal breakdown in silicon and/or melting metal interconnects due to high-current transient, or dielectric breakdown in gate oxide due to high-voltage overstress [1]. The ESD specifications of commercial IC products are generally higher than 2 kV in human- body-model (HBM) [2] ESD stress and 200 V in machine-model (MM) [3] ESD stress. Therefore, in order to provide the effective ESD protection for CMOS ICs against unexpected ESD damages in the internal circuits of CMOS ICs [4]–[10], the on-chip ESD protection circuits have to be designed and placed around the input, output, and power pads to clamp the overstress voltage across the internal circuits, and to provide a low impendence path to ground for discharging the ESD current of several amperes. The locations of the ESD protection circuits to achieve whole-chip ESD protection for CMOS ICs are illustrated in Fig. 1 [11].

Due to the low holding voltage ($V_{\rm hold}$, about $\sim$1.5 V in general bulk CMOS processes) of silicon controlled rectifier (SCR) device [12]–[15], the power dissipation $(\text{power} \cong I_{\rm ESD} \times Vh)$ located on the SCR device during ESD stress is significantly less than that located on other ESD protection devices, such as the diode, MOS, BJT, or field-oxide device. The SCR device can sustain a much higher ESD level within a smaller layout area in CMOS ICs, so it has been used to protect the internal circuits against ESD damage for a long time. But, the SCR device still has a higher switching voltage (i.e., trigger voltage, as much as 22 V) in the sub-quarter-micron CMOS technology, which is generally greater than the gate-oxide breakdown voltage of the input stages. Furthermore, the gate oxide thickness, its time-to-breakdown $(t_{\rm BD})$, or charge-to-breakdown $(Q_{\rm BD})$ will be also decreased with the shrinkage of CMOS technologies. Thus, it is imperative to reduce the switching voltage of SCR and to enhance the turn-on speed of SCR for efficiently protecting the ultrathin gate oxide from latent damage or rupture [16], especially against the fast charged-device-model (CDM) [17] ESD events. Therefore, to provide more effective on-chip ESD protection, the modified lateral SCR (MLSCR) [18] and the low-voltage triggering SCR (LVTSCR) [19], [20] had been invented to reduce the switching voltage of SCR device. Moreover, some advanced trigger-assist circuit techniques had been also reported to enhance the turn-on speed of SCR device, such as the gate-coupled technique [21], the hot-carrier triggered technique [22], the GGNMOS-triggered technique [23], [24], the substrate-triggered technique [25], [26], double-triggered technique [27], native-NMOS-trigger technique [28], etc. For mixed-voltage I/O buffer, the stacked-NMOS triggered SCR was invented to improve the ESD level of stacked nMOS [29], [30].

The review of SCR-based devices for on-chip ESD protection is investigated and compared in this paper. In addition, the solutions to avoid the transient-induced latchup issue [31] of SCR-based devices in CMOS IC products are also discussed. However, the static latchup issue will vanish certainly when the maximum voltage supply of IC products is smaller than the holding voltage of SCR devices. For example, a single NANSCR with holding voltage of $\sim$1.6 V can be safely used as on-chip ESD protection without static latchup danger in a 0.13-μm CMOS process with the maximum power supply voltage of 1.2 V. For some noisy circuit applications, NANSCR can be designed with series diodes to raise its holding voltage and to improve its latchup immunity, which will be discussed in Section IV.

II. Turn-on Mechanism of SCR Device

The equivalent circuit schematic of the SCR device is shown in Fig. 2(a). The SCR device consists of a lateral NPN and

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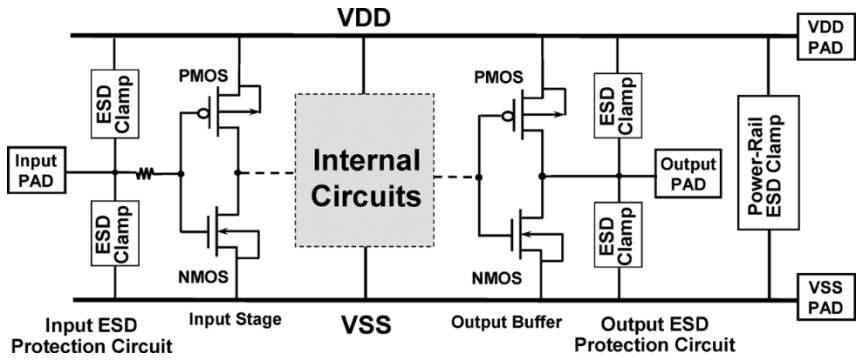

Fig. 1. Typical design of on-chip ESD protection circuits in CMOS ICs.

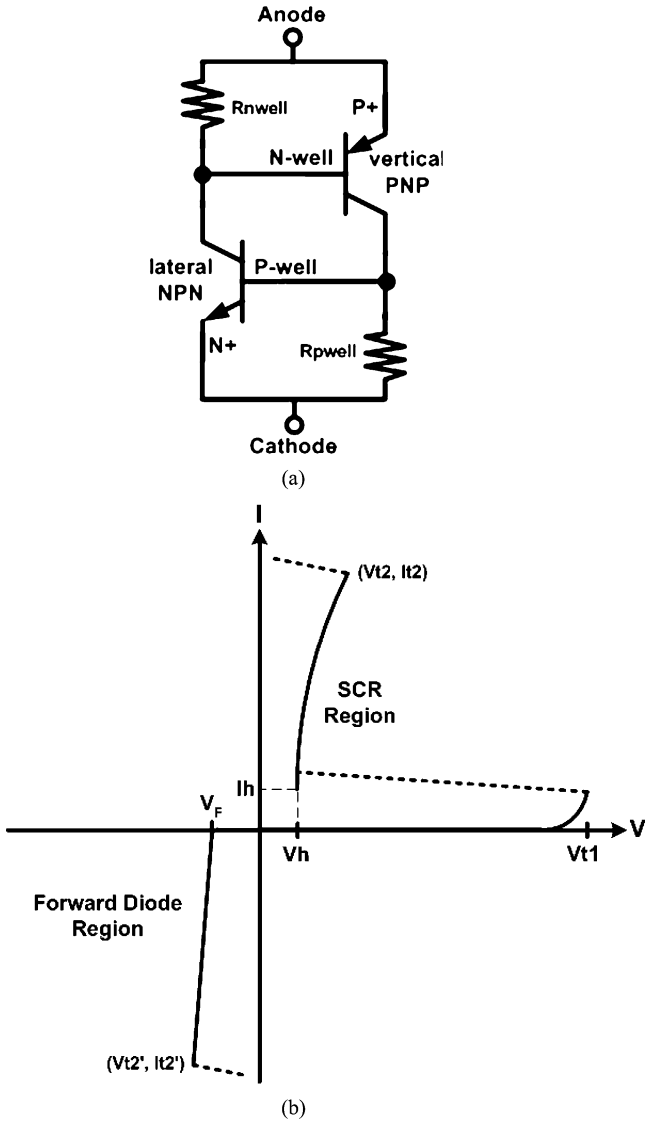

Fig. 2. (a) Equivalent circuit schematic of a SCR device. (b) *I–V* characteristics of SCR device in CMOS process under positive and negative voltage biases.

a vertical PNP bipolar transistor to form a 2-terminal/4-layer PNPN (P+/N-well/P-well/N+) structure, which is inherent in the CMOS processes. The switching voltage of the SCR device is dominated by the avalanche breakdown voltage of the N-well/P-well junction, which could be as much as 22 V in a 0.25-μm CMOS process, or $\sim$18 V in a 0.13-μm CMOS process. When the positive voltage applied to the anode of SCR is greater than the breakdown voltage and its cathode is relatively grounded, the hole and electron current will be generated through the avalanche breakdown mechanism. The hole current will flow through the P-well to P+ diffusion connected to ground, whereas the electron current will flow through the N-well to N+ diffusion connected to the anode of SCR. As long as the voltage drop across the P-well resistor (Rpwell) (N-well resistor (Rnwell)) is greater than 0.7 V, the NPN (PNP) transistor will be turned on to inject the electron (hole) current to further bias the PNP (NPN) transistor, which initiates the SCR latching action. Finally, the SCR will be successfully triggered into its latching state with the positive-feedback regenerative mechanism [32], [33].

The DC *I–V* characteristics of the SCR device is shown in Fig. 2(b). Once the SCR is triggered on, the required holding current to keep the NPN and PNP transistors on can be generated through the positive-feedback regenerative mechanism of latchup without involving the avalanche breakdown mechanism again. So, the SCR has a lower holding voltage ($V_{\rm hold}$) of $\sim$1.5 V, typically in the bulk CMOS processes. If the negative voltage is applied on the anode terminal of the SCR, the parasitic diode (N-well/P-well junction) inherent in SCR structure will be forward biased to clamp the negative voltage at a lower voltage level of $\sim$1 V (cut-in voltage of a diode). Whatever the ESD energy is, positive or negative, the SCR device can clamp ESD overstresses to a lower voltage level, so the SCR device can sustain the highest ESD robustness within a smaller layout area in CMOS ICs.

III. SCR-Based Devices for CMOS On-Chip ESD Protection

A. Lateral SCR (LSCR) [12]–[15]

The lateral SCR (LSCR) device was used as an effective input ESD protection element in CMOS ICs. The device structure of the LSCR is illustrated in Fig. 3(a), and the corresponding positive *I–V* characteristics of the LSCR in a 0.25-μm CMOS process is shown in Fig. 3(b). The negative *I–V* curve of the LSCR device is the curve of forward-biased P-well/N-well diode inherent in the LSCR, as that shown in Fig. 2(b). The forward-biased diode path used to discharge the negative-to-VSS ESD stress is often not the worst ESD path as compared with the SCR path, so this paper will be focused on only the SCR path. The application example of the LSCR

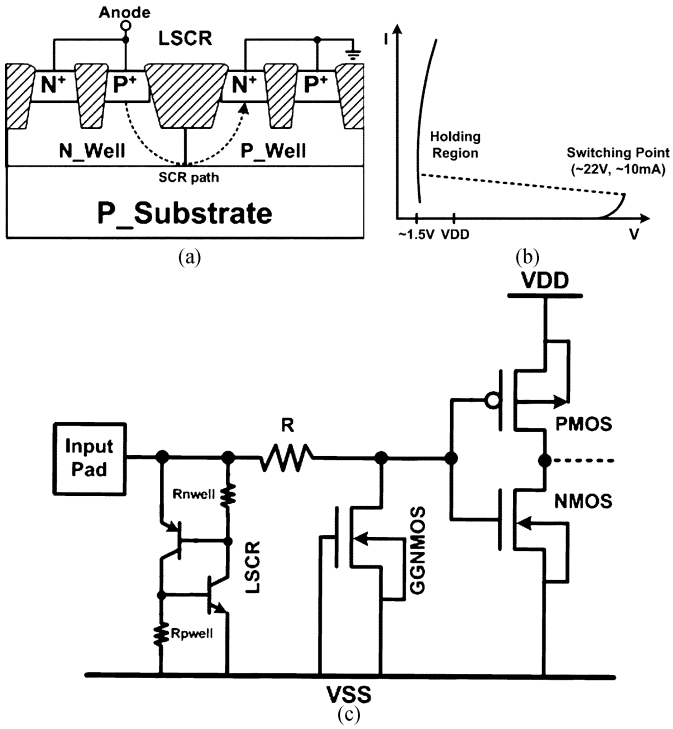

Fig. 3. (a) Device structure of the lateral SCR (LSCR) in CMOS process. (b) *I–V* characteristics of the LSCR in a 0.25-μm CMOS process. (c) Input ESD protection circuit with the LSCR device.

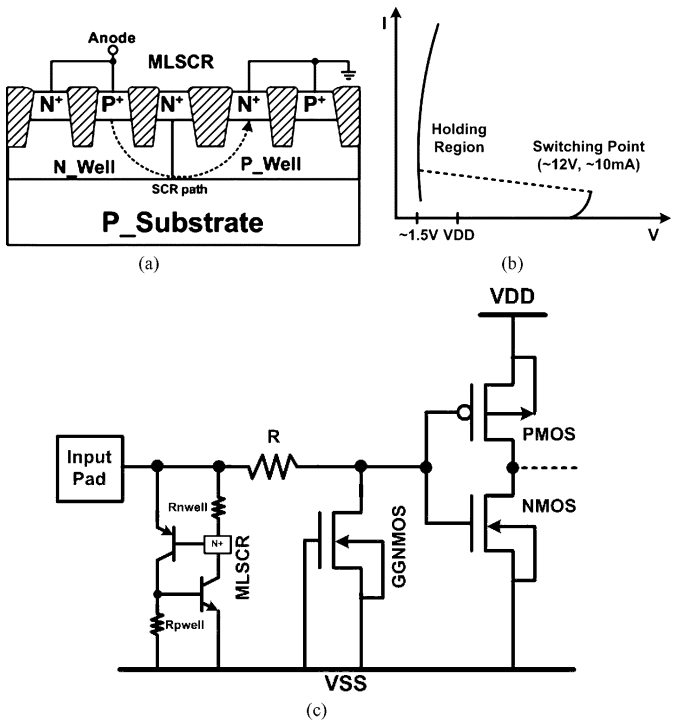

Fig. 4. (a) Device structure of the modified LSCR (MLSCR) in CMOS process. (b) *I–V* characteristics of the MLSCR in a 0.25-μm CMOS process. (c) Input ESD protection circuit with the MLSCR device.

device in the input ESD protection circuit is shown in Fig. 3(c). The LSCR has a switching voltage of $\sim$22 V in a 0.25-μm CMOS process, which is generally greater than the gate-oxide breakdown voltage of the input stages. Therefore, the SCR device needs the additional secondary protection circuit [the series resistor and the gate-grounded nMOS (GGNMOS), in Fig. 3(c)] to perform the overall ESD protection function to protect the input stages. The secondary protection circuit has to sustain ESD stress before the LSCR is triggered on to discharge ESD current on the input pad. The design equation among the LSCRs switching voltage (Vt1_SCR), series resistor (R), secondary breakdown voltage of GGNMOS (Vt2_GGNMOS), and secondary breakdown current of GGNMOS (It2_GGNMOS) can be calculated as

$$\mathrm{Vt1\_SCR} < (\mathrm{It2\_GGNMOS} \times \mathrm{R}) + \mathrm{Vt2\_GGNMOS}. \quad (1)$$

Because the LSCR is difficult to trigger on in time, the secondary ESD protection circuit was designed with larger-sized GGNMOS and series resistor to protect itself from ESD damage before the LSCR is triggered on. This secondary ESD protection circuit with large device dimensions often occupies more layout area. If the secondary protection circuit was not properly designed, it caused some fail window in the ESD test scanning from the low voltage to high voltage [34]. Such input ESD protection circuit was found to pass the ESD stress with low voltage level and high voltage level, but it failed with ESD stress with a middle voltage level [34]. So, the design of LSCR with the secondary protection circuit to achieve effective input ESD protection is somewhat critical in CMOS ICs.

B. Modified Lateral SCR (MLSCR) [18]

In order to reduce the switching voltage of LSCR device to provide more effective ESD protection for the internal circuits, the modified lateral SCR (MLSCR) was invented. The device structure of the MLSCR is illustrated in Fig. 4(a), and the corresponding *I–V* characteristics of the MLSCR in a 0.25-μm CMOS process is shown in Fig. 4(b). The application example of using the MLSCR device as the input ESD protection circuit is shown in Fig. 4(c). The MLSCR is made by adding an N+ diffusion across the N-well/P-well junction to lower the avalanche breakdown voltage of N-well/P-well junction. However, the switching voltage ($\sim$12 V) of the MLSCR could be still somewhat too high to effectively protect the thin gate oxide of input stages in the same 0.25-μm CMOS process. Therefore, the MLSCR has to be still cooperated with the secondary protection circuit to perform the overall ESD protection function for the input stages. Due to the low switching voltage ($\sim$12 V) of the MLSCR in the 0.25-μm CMOS process, the secondary protection circuit can be drawn with smaller device dimensions to save layout area. For the output stage, the two-stage ESD protection configuration in Fig. 4(c) will cause some signal delay under normal circuit operating conditions, so the LSCR and MLSCR devices were seldom used in the ESD protection circuits for output buffers.

C. Low-Voltage Triggering SCR (LVTSCR) [19], [20]

To more effectively protect the input stages and even the output stages, the low-voltage triggering SCR (LVTSCR) was invented. The device structure of the LVTSCR is illustrated in Fig. 5(a), and the corresponding *I–V* characteristics of the LVTSCR in a 0.25-μm CMOS process is shown in Fig. 5(b).

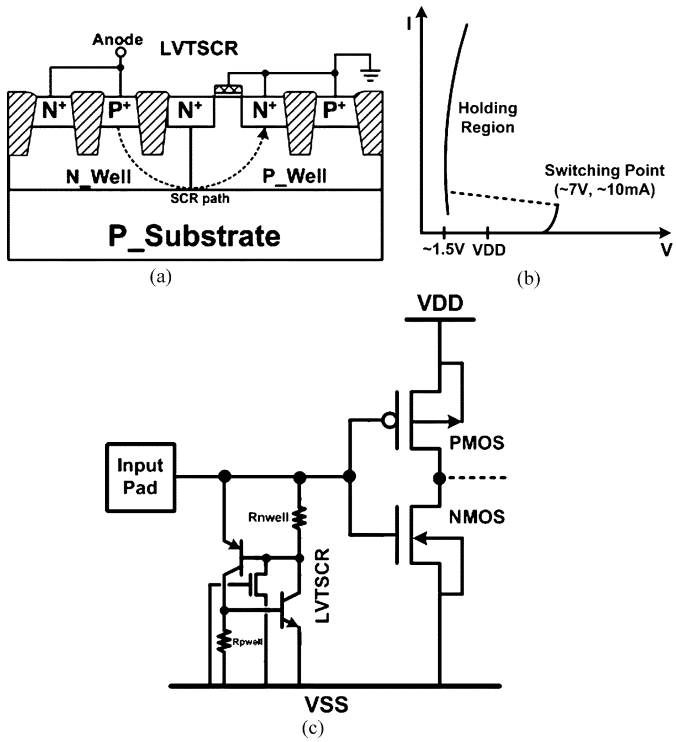

Fig. 5. (a) Device structure of the low-voltage triggering SCR (LVTSCR) in CMOS process. (b) *I–V* characteristics of the LVTSCR in a 0.25-μm CMOS process. (c) Application example of input ESD protection circuit with the LVTSCR device.

The application example of using the LVTSCR device as the input ESD protection circuit is shown in Fig. 5(c). The switching voltage of the LVTSCR ($\sim$7 V) is equivalent to the drain breakdown or punch-through voltage of the short-channel nMOS device, which is inserted into the lateral SCR structure, rather than the original switching voltage ($\sim$22 V) of LSCR device. With such a low switching voltage, the LVTSCR can provide effective ESD protection for the input stage of CMOS ICs without a secondary ESD protection circuit. Therefore, the total layout area of the ESD protection circuits with LVTSCR can be significantly saved. For output ESD protection, a small series resistor is suggested to be added between the LVTSCR and the output buffer, otherwise the LVTSCR is not effective to protect the output buffer. Furthermore, the complementary-LVTSCR structure [20] has invented to provide better ESD protection against ESD stresses from the I/O pad to VDD or VSS.

D. Gate-Coupled LVTSCR [21]

To effectively protect the ultrathin gate oxide in deep-submicron CMOS process, the gate-coupled technique was applied to further reduce the switching voltage of LVTSCR without involving avalanche breakdown mechanism. The ESD protection circuit for input or output pad with the complementary gate-coupled LVTSCR devices [NMOS-triggered LSCR (NTLSCR) and PMOS-triggered LSCR (PTLSCR)] is shown in Fig. 6(a). The N-well of NTLSCR, connected to VDD instead of the I/O pad, is used to discharge the positive-to-VDD (PD) ESD stress (with grounded VDD but floating VSS) through the forward-biased P+/N-well diode. The negative-to-VSS (NS) ESD stress (with grounded VSS but floating VDD) can be discharged through the forward-biased P-well/N+ cathode of the PTLSCR device. The device structure of the complementary gate-coupled LVTSCR is illustrated in Fig. 6(b), and the *I–V* characteristics of the gate-coupled LVTSCR in a 0.25-μm CMOS process is shown in Fig. 6(c). The dependence of the switching voltage of SCR device on the gate-bias voltage of the NTLSCR device is shown in Fig. 6(d). The capacitances (Cn and Cp) in Fig. 6(a) must be designed at some suitable value, where the coupled voltage under normal circuit operating conditions is smaller than the threshold voltage of NMOS/PMOS, but greater than the threshold voltage of NMOS/PMOS under ESD stress conditions [35]. The switching voltage of the gate-coupled NTLSCR (PTLSCR) can be adjusted by the voltage level on the gate of the short-channel nMOS (PMOS) in the SCR device structure. The higher coupled voltage on the gate of the short-channel NMOS/PMOS in the LVTSCR leads the lower switching voltage of LVTSCR. Therefore, the gate-coupled LVTSCR devices can be quickly turned on to provide more effective protection for the ultrathin gate oxide of the input or output stages against ESD stress.

E. Hot-Carrier Triggered SCR (HCTSCR) [22]

The power-rail ESD clamp circuit with hot-carrier triggered SCR (HCTSCR) is shown in Fig. 7(a). The device structures of the primary protection devices including the SCR and trigger nMOS (M1) are shown in Fig. 7(b). The triggering mechanism of the HCTSCR is initiated by the substrate hole current generated from the hot carrier effect of M1 during an ESD event. To ensure the proper operation of the HCTSCR, M1 must be active to provide sufficient substrate current to trigger on the SCR before other devices are damaged by ESD energy. The switching voltage of the HCTSCR is dependent on the substrate hole current, which is the function of gate length, gate voltage, and drain voltage of M1 [36]. The smaller gate length of M1 results in the lower switching voltage of the HCTSCR. The gate voltage coupled through the capacitor (M2) has to be carefully designed to gain the peak substrate current. The device dimensions of M2 and M3 have to be optimized to ensure that the gate voltage of M1 is greater than its threshold voltage to trigger HCTSCR on during ESD stresses. In addition, a double guardring has to be used around the perimeter of the HCTSCR to prevent the SCR from being accidentally triggered on by the current injected from the exterior. With an SCR as the power-rail ESD clamp circuit, it can effectively clamp the ESD overstress voltage to avoid ESD damage to internal circuits. However, this SCR in a power-rail ESD clamp circuit could be triggered on by transient-induced latchup [31], when the IC is under normal operating conditions. This will cause serious latchup failure on the CMOS IC, if the holding voltage of SCR device is smaller than the VDD voltage level.

F. Gate-Grounded nMOS Triggered SCR (GGSCR) [23], [24]

The gate-grounded nMOS triggered SCR (GGSCR) is another design for on-chip ESD protection circuit. An nMOS transistor, which resembles a gate-grounded configuration, is used as an external trigger device to trigger on the GGSCR. In contrast to the LVTSCR, the drain of the external trigger nMOS in

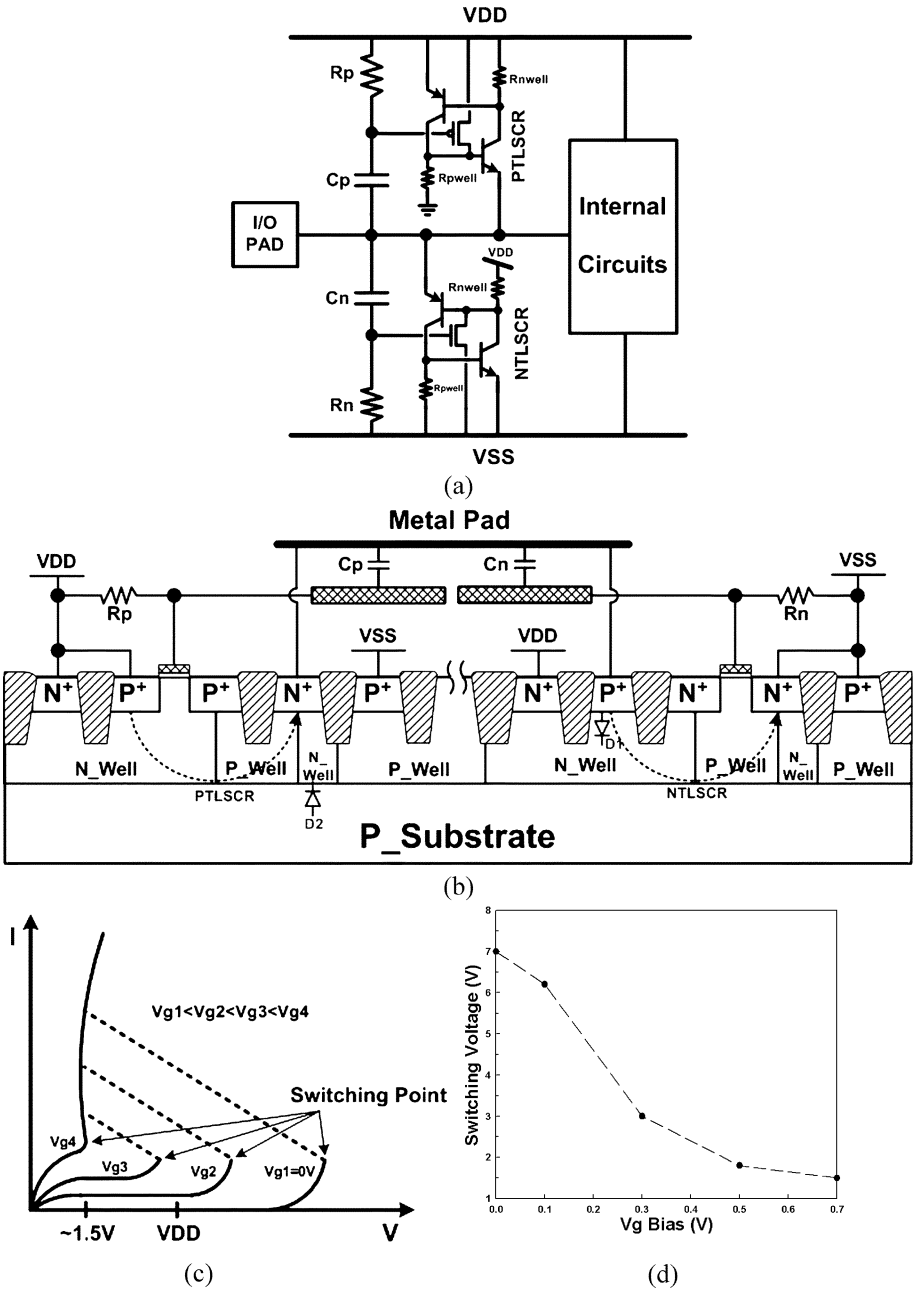

Fig. 6. (a) ESD protection circuit with the gate-coupled LVTSCR devices. (b) Device structure of the gate-coupled LVTSCR device in CMOS process. (c) *I–V* characteristics of the gate-coupled LVTSCR device in a 0.25-μm CMOS process. (d) Dependence of switching voltage of SCR device on the gate bias voltage of the NTLSCR device.

GGSCR is directly coupled to the pad and its gate and source are coupled into the P-substrate (the base of NPN). The application example of using the GGSCR device as the input ESD protection circuit is shown in Fig. 8(a). The layout top view of the GGSCR is illustrated in Fig. 8(b) [24]. When an ESD voltage is applied to the I/O pad in Fig. 8(a), the external trigger nMOS will enter avalanche breakdown first to inject the triggering current into the P-substrate. As long as the base voltage of NPN is greater than 0.7 V, the GGSCR will be triggered on. The poly resistor (Rp) in Fig. 8(b) is used to control the triggering and holding current and to prevent the false trigger of GGSCR. From the experimental results, the GGSCR, designed with a shorter anode-to-cathode spacing, has the lower holding voltage, higher *It2*, better *dV/dt* triggering ability, and faster turn-on speed than those of LVTSCR with a longer anode-to-cathode spacing.

G. Substrate-Triggered SCR (STSCR) [25], [26]

The turn-on mechanism of an SCR device is essentially a current triggering event. While a current is applied to the base or substrate of an SCR device, it can be quickly triggered on into its latching state. With the substrate-triggered technique, the p-type substrate-triggered SCR (P_STSCR) and n-type substrate-triggered SCR (N_STSCR) devices for ESD protection were reported. The device structures of the P_STSCR and N_STSCR are illustrated in Fig. 9(a) and (b), respectively. As compared with

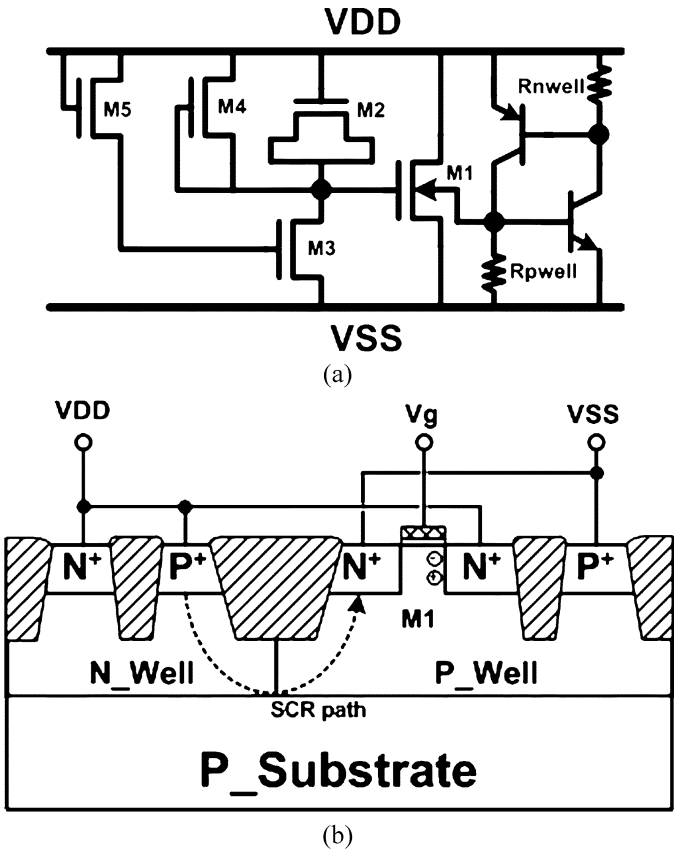

Fig. 7. (a) Power-rail ESD clamp circuit with the hot-carrier triggered SCR (HCTSCR) device. (b) Device structures of primary protection devices including SCR and nMOS M1.

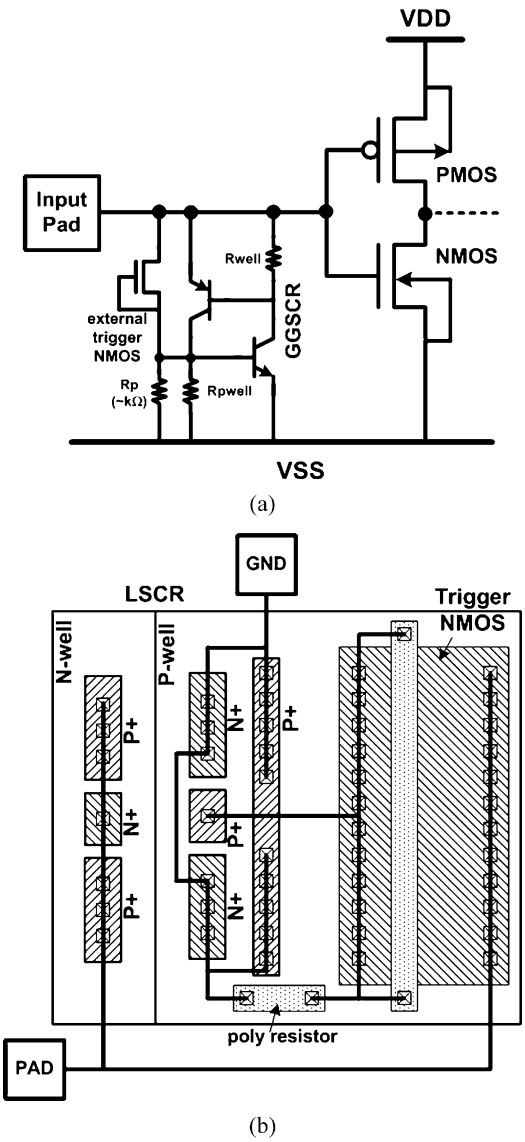

Fig. 8. (a) Input ESD protection circuit with the grounded-gate nMOS triggered SCR (GGSCR) device. (b) Layout top view of the GGSCR in a CMOS process.

the traditional lateral SCR device structure, an extra P+ diffusion is inserted into the P-well of the P_STSCR device structure and connected out as the p-trigger node of the P_STSCR device. For the N_STSCR, an extra N+ diffusion is inserted into the N-well of the N_STSCR device structure and connected out as the n-trigger node of the N_STSCR device. The *I–V* characteristics of the P_STSCR and N_STSCR are shown in Fig. 9(c) and (d), respectively. With the increase of substrate-/well-triggered current, the switching voltage of P_STSCR/N_STSCR device can be reduced to its holding voltage. The turn-on time of STSCR can be also reduced to ~10 ns under 5-V voltage pulse with 10-ns rise time in a 0.25-μm CMOS process. The turn-on time can be further reduced by increasing the substrate-/well-triggered current [25] or reducing the rise time of voltage pulse [27], [28]. With the lower switching voltage, the STSCR device can clamp the overstress ESD voltage to a lower voltage level more quickly to fully protect the ultrathin gate oxide of input stages. The ESD protection circuit for input or output pad with the P_STSCR and N_STSCR devices is shown in Fig. 9(e). In the normal circuit operating conditions with VDD and VSS power supplies, the input of inv_1 (inv_2) is biased at VDD (VSS). Therefore, the output of the inv_1 (inv_2) is biased at VSS (VDD) due to the turn on of nMOS (PMOS) in the inv_1 (inv_2), whenever the input signal is logic high or logic low. The p-trigger (n-trigger) node of the P_STSCR (N_STSCR) device is kept at VSS (VDD) by the output of the inv_1 (inv_2), so the P_STSCR and N_STSCR devices are guaranteed to be kept off in the normal circuit operating conditions. Under the positive-to-VSS (PS) ESD stress condition (with grounded VSS but floating VDD) in Fig. 9(e), the input of the inv_1 is initially floating with a zero voltage level, thereby the pMOS of the inv_1 will be turned on due to the positive ESD voltage on the pad. So, the output of the inv_1 is charged up by the ESD energy to generate the trigger current into the p-trigger node of the P_STSCR device. Therefore, the P_STSCR device is triggered on, and the ESD current is discharged from I/O pad to the grounded VSS pin through the P_STSCR device. The similar operating principle can be applied to N_STSCR under the negative-to-VDD (ND) ESD-zapping condition (with grounded VDD but floating VSS). Under NS-mode ESD stress condition, the P-well/N+ junction of N_STSCR can be forward biased to discharge ESD current. Under PD-mode ESD stress condition, the P+/N-well junction of P_STSCR can be forward biased to discharge ESD current. Furthermore, the STSCR device with dummy-gate structure had been invented [37], [38] to further reduce the switching voltage

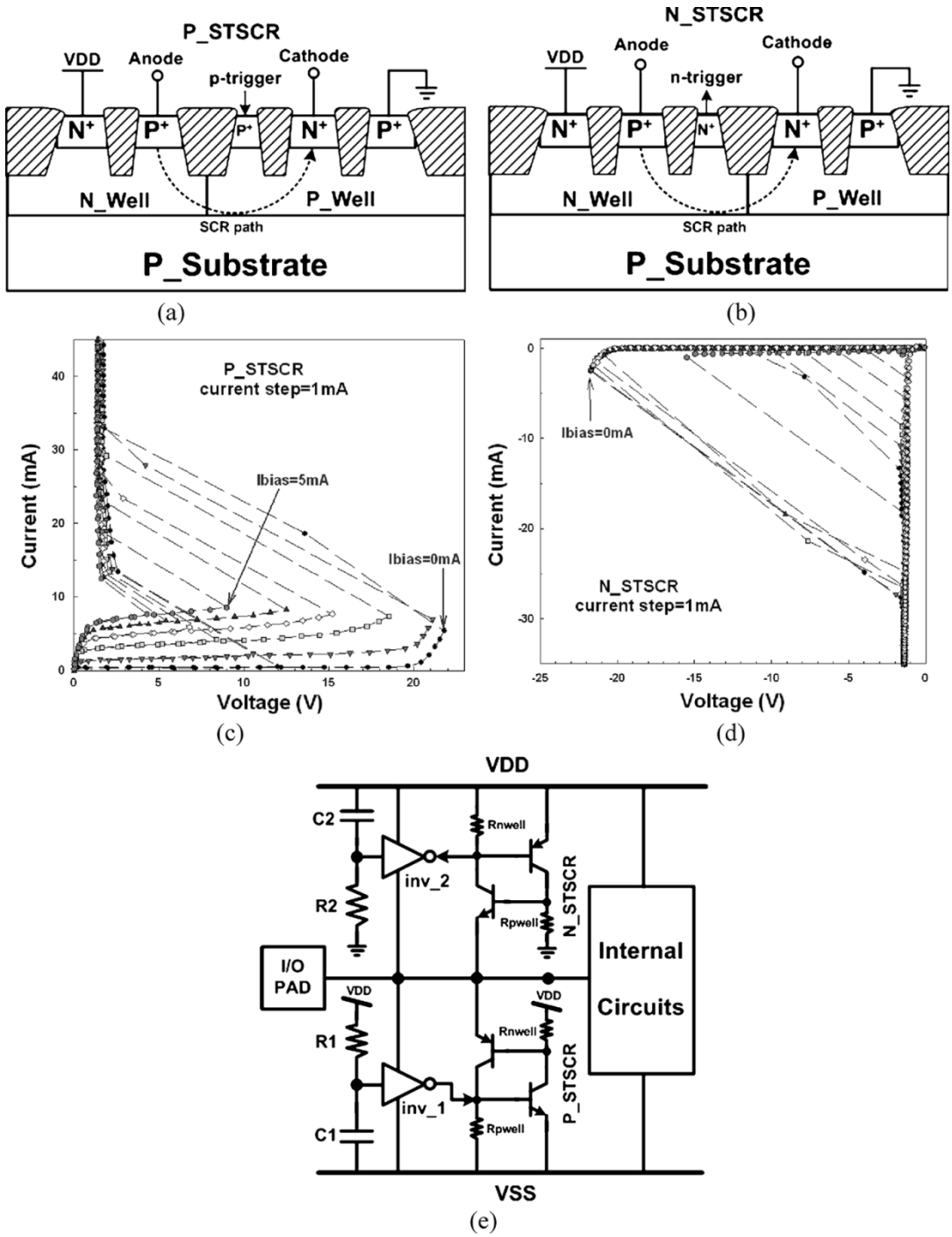

Fig. 9. Device structures of (a) the p-type substrate-triggered SCR (P_STSCR) and (b) the n-type substrate-triggered SCR (N_STSCR) devices. The *I–V* characteristics of (c) the P_STSCR and (d) the N_STSCR devices in a 0.25-μm CMOS process. (e) The ESD protection circuit with the P_STSCR and N_STSCR devices for I/O pad.

and to improve the turn-on speed of STSCR. The bipolar current gain of STSCR with dummy-gate structure is larger than that of STSCR with shallow trench isolation (STI) structure, so the triggering efficiency of STSCR with dummy-gate structure is better than that of STSCR with STI.

H. Double-Triggered SCR (DTSCR) [27]

Another method, to reduce the switching voltage of LSCR device and to further enhance the turn-on speed of LSCR device more efficiently, is the double-triggered technique. The device structure of the double-triggered SCR (DTSCR) is shown in Fig. 10(a). The extra P+ and N+ diffusions are inserted into the P-well and N-well of DTSCR device structure and connected out as the p-trigger and n-trigger nodes of the DTSCR device. The dependence of the switching voltage of the DTSCR device on the substrate-triggered current under different N-well triggered currents is summarized in Fig. 10(b). The switching voltage of the DTSCR can be reduced to a lower voltage level more efficiently if the substrate and N-well triggered currents are synchronously applied to the p-trigger and n-trigger nodes,

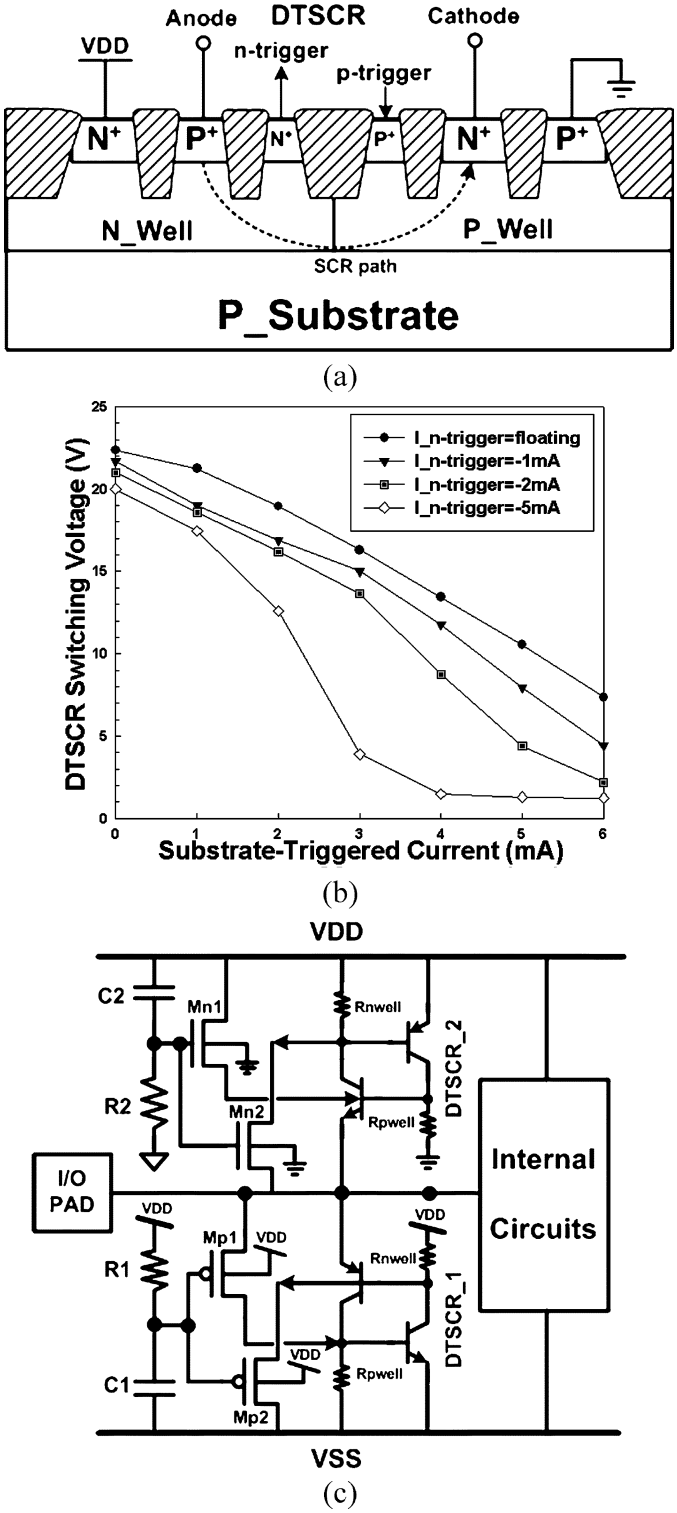

Fig. 10. (a) Device structure of the double-triggered SCR (DTSCR). (b) Dependence of the switching voltage of DTSCR device on the substrate-triggered current under different N-well triggered currents in a 0.25-μm CMOS process. (c) The ESD protection circuit with the DTSCR devices for I/O pad.

respectively. The I/O ESD protection circuit realized with DTSCR devices is shown in Fig. 10(c). Based on the *RC* delay principle, the substrate (N-well) triggered currents can be generated by the Mp1 and Mp2 (Mn1 and Mn2), respectively, under PS (ND)-mode ESD stress condition. Therefore, the DTSCR with the double-triggered currents in Fig. 10(c) can be triggered on more quickly to discharge ESD current. Under NS (PD)-mode ESD stress condition, the P-well/N+ (P+/N-well) junction of DTSCR_2 (DTSCR_1) can be forward biased to discharge ESD current. In the normal circuit operating conditions with VDD and VSS power supplies, the gates of Mp1 and Mp2 (Mn1 and Mn2) are biased at VDD (VSS) through the resistor R1 (R2). Therefore, the Mp1, Mp2, Mn1, and Mn2 are all in off state, whenever the input signal is high or low. The p-trigger (n-trigger) node of the DTSCR device are kept at VSS (VDD) through the parasitic resistor Rsub (Rwell), so the DTSCR is guaranteed to be kept off in the normal circuit operating conditions. From the experimental results in a 0.25-μm CMOS process, when a 0-to-5 V voltage pulse with rise time of 10 ns is applied to the anode of the DTSCR, the turn-on time of the DTSCR is about $\sim$37 ns under the positive voltage pulse of 1.5 V at p-trigger node of DTSCR. But the turn-on time of the DTSCR can be further reduced to $\sim$12 ns, while a negative voltage pulse of -5 V with fall time of 10 ns is synchronously applied to its n-trigger node. The turn-on time can be further reduced with increasing the voltage biases at the p-trigger and n-trigger nodes or reducing the rise time of voltage pulse [27]. The dummy-gate structure used to block the STI in the SCR device can be applied to the DTSCR structure to further reduce the switching voltage and to enhance the turn-on speed of DTSCR more efficiently.

I. Native-NMOS-Triggered SCR (NANSCR) [28]

The native nMOS is directly built in a lightly-doped p-type substrate in sub-quarter-micron CMOS process, whereas the normal nMOS (PMOS) is in a heavily-doped P-well (N-well) in a P-substrate twin-well CMOS technology. The native nMOS and lateral SCR can be merged together to be a new ESD protection device, native-NMOS-triggered SCR (NANSCR), which has the advantages of lower switching voltage and faster turn-on speed. The device structure of NANSCR is illustrated in Fig. 11(a). The gate of native nMOS is connected to a negative bias circuit (NBC) [39] to turn off the NANSCR under normal circuit operating conditions. The comparison of DC *I–V* curves between NANSCR and LVTSCR is shown in Fig. 11(b). The switching voltage ($\sim$4 V) of NANSCR with a channel length of 0.3 μm is smaller than that ($\sim$5 V) of LVTSCR with a channel length of 0.13 μm in a 0.13-μm silicided CMOS process under the same channel width. With the substrate-triggered technique, the switching voltage of NANSCR can be further reduced by the increase of the W/L ratio of native NMOS. The switching voltage of NANSCR can be further reduced to only $\sim$2.5 V if the channel width of native nMOS in NANSCR is increased from 20 to 40 μm in Fig. 11(b). The ESD protection circuit for input or output pad with the NANSCR devices is shown in Fig. 11(c). No extra series resistor needs to be added between output buffer and NANSCR, because the NANSCR can be turned on more quickly than the output buffer. In normal circuit operating conditions, the gates of native nMOS in all NANSCR devices are biased by the same NBC to turn off the NANSCR devices. So, the NANSCR devices, NANSCR_1 and NANSCR_2, will not interfere with the functions of the I/O circuits. Under the PS-mode ESD stress condition, the gate of

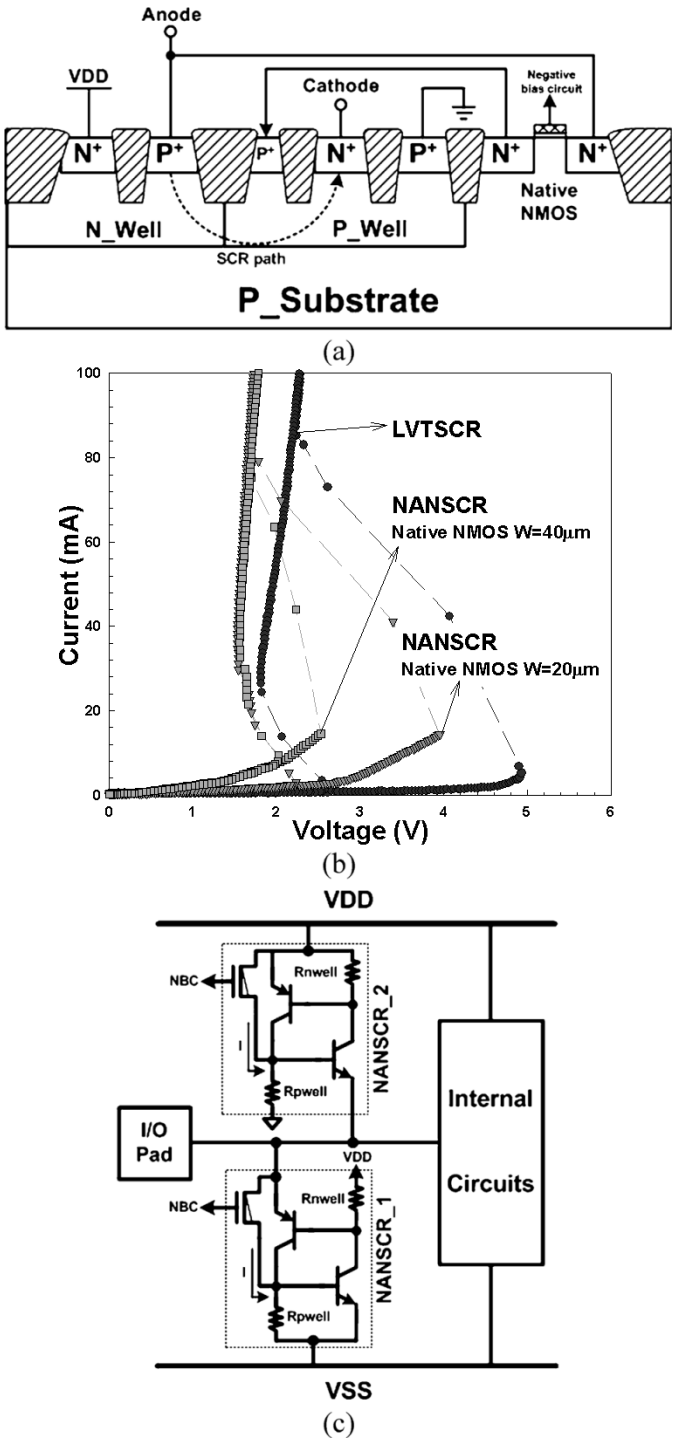

Fig. 11. (a) Device structure of the native-NMOS-triggered SCR (NANSCR). (b) Comparison of DC *I–V* curves between NANSCR and LVTSCR in a 0.13-μm CMOS process. (c) ESD protection circuit with the NANSCR device.

native nMOS in the NANSCR_1 is floating. The NANSCR_1 is triggered on quickly by the substrate-triggering current generated from the already-on native NMOS. So, the positive ESD current can be quickly discharged from the I/O pad through the NANSCR_1 to grounded VSS line. Under the ND-mode ESD stress condition, the gate of native nMOS in the NANSCR_2 is floating but with an initial voltage level of 0 V. The negative ESD voltage at the I/O pad will pull down the source voltage of native nMOS through the base-emitter junction of NPN in the NANSCR_2 device. Therefore, the native nMOS in NANSCR_2 will be turned on first, resulting in the NANSCR_2 being fully triggered on. The negative ESD current will be discharged from the I/O pad through NANSCR_2 to the grounded VDD line. For the NS (PD)-mode ESD stress condition, the P-well/N+ (P+/N-well) junction of NANSCR_2 (NANSCR_1) can be forward biased to discharge the ESD current. From the experimental results in a 0.13-μm CMOS process, the turn-on speed of NANSCR is faster than that of LVTSCR. Under the voltage pulse with shorter rise time, the turn-on time of NANSCR can be further reduced to follow the rise time of the voltage pulse [28]. Moreover, under the CDM ESD test with a monitored thin gate oxide of $\sim$20 Å, such NANSCR can sustain a higher CDM ESD level (5 V/μm^2) than that (2.33 V/μm^2) of the LVTSCR in 0.13-μm CMOS process, where the test chip has a die size of 1500×1500 μm^2 in a 40-pin DIP package. So, the design of the NANSCR is more suitable to protect the ultrathin gate oxide in nanoscale CMOS technologies.

J. Stacked-NMOS Triggered SCR (SNTSCR) for Mixed-Voltage I/O Buffer [29], [30]

To improve ESD robustness of the stacked nMOS in the conventional mixed-voltage I/O buffers, the stacked-NMOS triggered SCR (SNTSCR) had been reported without using the thick gate oxide. The ESD protection circuit combining the gate-coupled circuit with SNTSCR for mixed-voltage I/O buffer is shown in Fig. 12(a). The ESD detection circuit and the device structure of SNTSCR are shown in Fig. 12(b). Such an ESD protection circuit with only thin gate oxide is fully compatible with general CMOS process without causing the gate-oxide reliability issue. During the normal circuit operating conditions, the Mn3 in Fig. 12(b) acts as a resistor to bias the gate voltage (Vg1) of Mn1 at VDD. But, the gate of Mn2 is grounded through the resistor R2. So, all the devices in the ESD protection circuit can meet the electrical-field constraint of gate-oxide reliability in the normal circuit operation condition. Under PS-mode ESD stress condition, the Mp is turned on but Mn3 is off since the initial voltage level on the floating VDD line is zero. The capacitors C1 and C2 are designed to couple ESD transient voltage from the I/O pad to the gates of Mn1 and Mn2, respectively. The coupled voltage should be designed greater than the threshold voltage to turn on Mn1 and Mn2 for triggering on the SNTSCR device, before the devices in the mixed-voltage I/O circuit are damaged by ESD stress. With the gate-coupled circuit technique, the switching voltage of SNTSCR can be nearly reduced to its holding voltage, so the SNTSCR can be quickly triggered on to discharge ESD current. From the experimental results in 0.35-μm CMOS process, the HBM ESD level of the mixed-voltage I/O buffer with this ESD protection circuit can be greatly improved to 8 kV, as compared with that ($\sim$2 kV) of the traditional mixed-voltage I/O buffer with stacked nMOS device only.

K. Dual-Direction SCR [40]

A typical ESD protection scheme must protect each I/O pad against ESD events in all stress modes with respect to both VDD and VSS power lines (i.e., positive-to-VSS (PS),

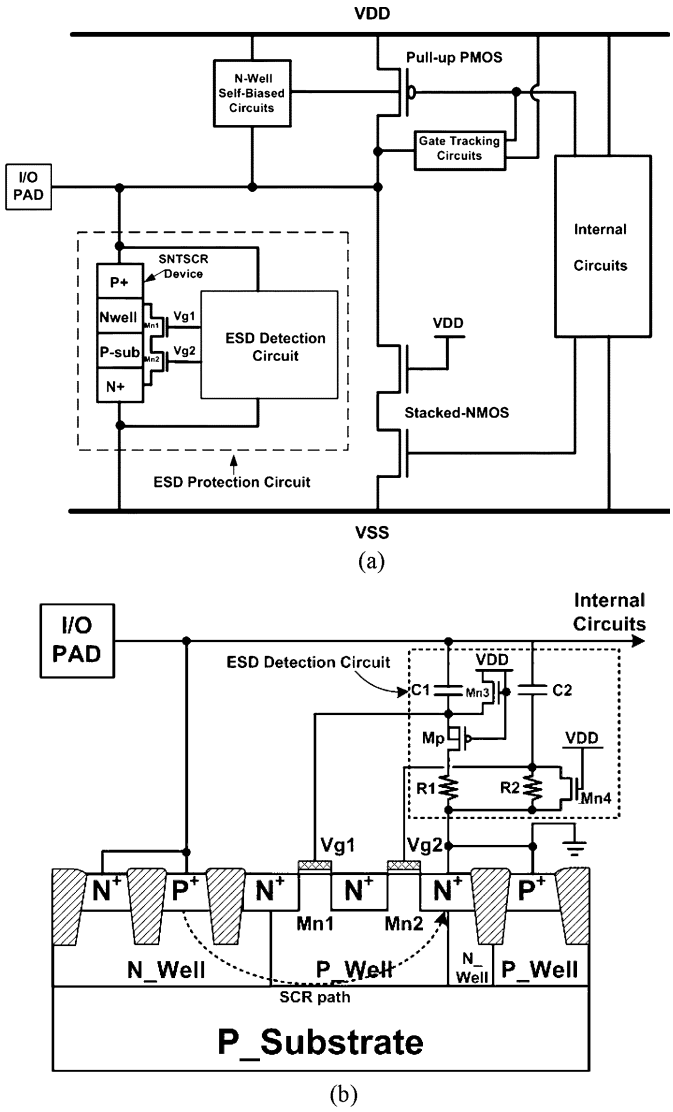

Fig. 12. (a) ESD protection circuit with stacked-NMOS triggered SCR (SNTSCR) device for mixed-voltage I/O interface. (b) ESD detection circuit and the device structure of the SNTSCR.

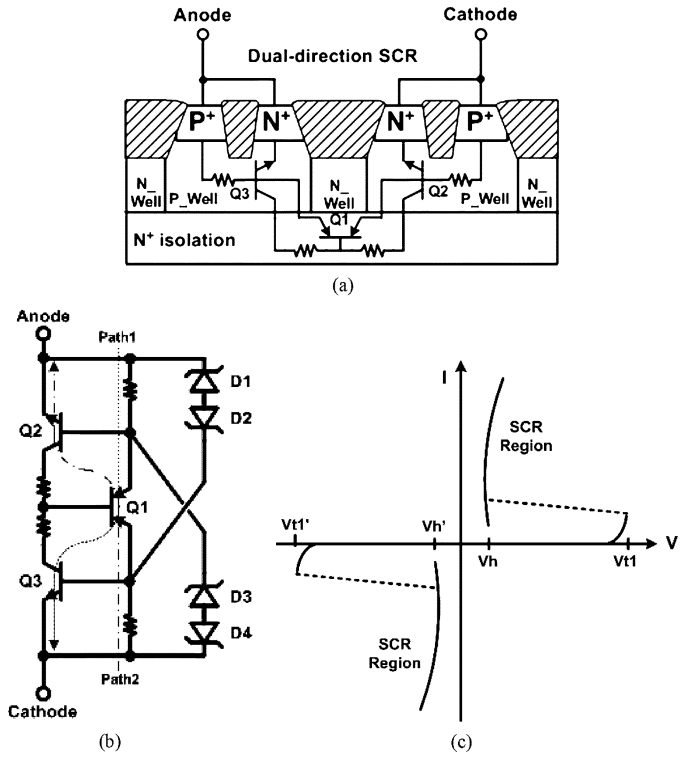

Fig. 13. (a) Device structure of the dual-direction SCR. (b) Circuit schematic of the low-trigger-voltage ESD protection circuit consists of a core dual-direction SCR and two back-to-back Zener diodes. (c) *I–V* characteristics of the dual-direction SCR device.

negative-to-VDD (ND), positive-to-VDD (PD), and negative-to-VSS (NS) ESD stress conditions). The dual-direction SCR device was invented in BiCMOS technology to provide the ESD current paths through SCR for all ESD stress modes. The device structure of a dual-direction SCR device illustrated in Fig. 13(a) is a symmetrical 5-layer NPNPN structure, which comprises one lateral PNP (Q1) and two vertical NPN (Q2 and Q3) in the BiCMOS process. The trigger-assist circuit to reduce the switching voltage of dual-direction SCR comprises two pairs of Zener diodes (D1–D4) with back-to-back connection, as shown in Fig. 13(b). When a positive ESD pulse is applied to the anode of dual-direction SCR and its cathode is relatively grounded (e.g., PS or ND-mode ESD stress condition), the Zener diode D1 will be reverse breakdown first to conduct some ESD current to trigger on the NPN bipolar Q3 and then in turn turns on the PNP bipolar Q1. The positive ESD current can be discharged through the current path1 in Fig. 13(b). Similarly, when a negative ESD pulse is applied to anode of dual-direction SCR with its cathode grounded (e.g., PD or NS-mode ESD stress condition), the negative ESD current can be discharged through the current path2 in Fig. 13(b). The *I–V* characteristics of the dual-direction SCR is shown in Fig. 13(c). Such a dual-direction SCR can provide the desired low holding voltage and low impedance path to protect the internal circuit under positive and negative ESD stresses. To realize the dual-direction SCR device in the CMOS process, an extra deep N-well mask will be added into the process flow. In the earlier literature, the full-SCR protection scheme for I/O pad with four SCR devices in CMOS IC had been reported [41].

L. SCR Devices for RF ESD Protection

In order to achieve the ESD specification of commercial IC products, the regular GGNMOS device is usually designed with hundreds of microns in channel width and drawn in multifinger structure. The parasitic capacitance of the ESD protection device (GGNMOS) can be in the order of several pF, which will seriously degrade the performance of radio-frequency (RF) circuit in giga-Hz frequency bands. Because the SCR device can sustain a high enough ESD level in a smaller layout area which in turn has a low parasitic capacitance generated from the ESD protection device to RF input pin, SCR-based devices with low parasitic capacitance have been proposed as the ESD protection devices for RF ICs such as diode-triggered SCR [42] and all-directional SCR [43]. The diode-triggered SCR can be quickly triggered on by forward biasing the diode chain [44], which was used in the input ESD protection circuit for low-noise amplifiers (LNAs) [42]. The all-directional SCR is a three-terminal device to discharge the pad-to-VDD, pad-to-VSS, and VDD-to-VSS ESD currents through the SCR paths, which was proposed to

be the ESD protection circuit for the RF and mixed-signal integrated circuits [43]. The simulated parasitic capacitance of all-directional SCR can be greatly reduced as compared with the traditional GGNMOS. In addition, the all-directional SCR has shown to only generate slight increment in the noise figure of LNA. A modified design of the SCR, called an LC-SCR, having a low-capacitance loading has been reported in [45] for RF applications. Among all the SCR devices used for ESD protection in RF applications, the high switching voltage of the SCR should be considered in the ESD protection design for RF circuits. The gate-biased circuit for the cascade nMOS amplifier in the RF LNA, or even the gate oxide of the first nMOS of LNA, could be damaged before the SCR is triggered on during ESD stress. The high-level ESD stress can be triggered on the SCR by the transient-triggering effect to protect the RF LNA. However, the SCR during the low-level ESD stress could not be triggered on in time. The RF input stage could be damaged by such low-level ESD stress.

M. SCR Devices in Other Applications

Except for standard logic CMOS process, SCR devices can be used as the ESD protection circuits in other applications, such as high-voltage process. The drain-extended nMOS (DENMOS) or lateral DMOS (LDMOS) had been used in mature high-voltage processes to tolerant the large gate-to-drain voltage. However, the DENMOS or LDMOS is very poor to sustain the required ESD specifications under the limitation of parasitic capacitance. The DENMOS merged with an SCR [46], [47], or the embedded SCR LDMOS (ESCR-LDMOS) [48], had been reported to improve ESD level of high-voltage IC products. Another ESD protection device for high-voltage applications is the mirrored lateral SCR (MILSCR) [49]. The MILSCR, which is designed with dual-direction active SCR current paths, comprises two vertical NPN transistors, one vertical PNP transistor, and one lateral PNP transistor in N-epi P-substrate high-voltage CMOS process. The MILSCR was designed for high-voltage applications [49], but its switching voltage can be also adjusted to meet the requirements of the low-voltage CMOS ICs as those of the MLSCR or the LVTSCR. Although the SCR-based devices can elevate the ESD levels of high-voltage CMOS IC products, how to avoid the transient-induced latchup issue [31] of SCR-based devices under normal circuit operating conditions in high-voltage process is another important reliability consideration [50].

IV. SCR Latchup Engineering

The SCR-based ESD protection devices were designed with low enough switching voltage for effective ESD protection, however the transient-induced latchup issue [31] must be solved. There are two solutions to avoid the SCR-based devices with low switching voltage being accidentally triggered on by noise pulses when CMOS ICs are in normal circuit operating conditions. As shown in Fig. 14(a), one is to increase the triggering current of the low-voltage-trigger SCR-based devices, but the switching voltage and the holding voltage are kept the same. With higher triggering current, the low-voltage-trigger SCR-based devices can have enough noise margins against

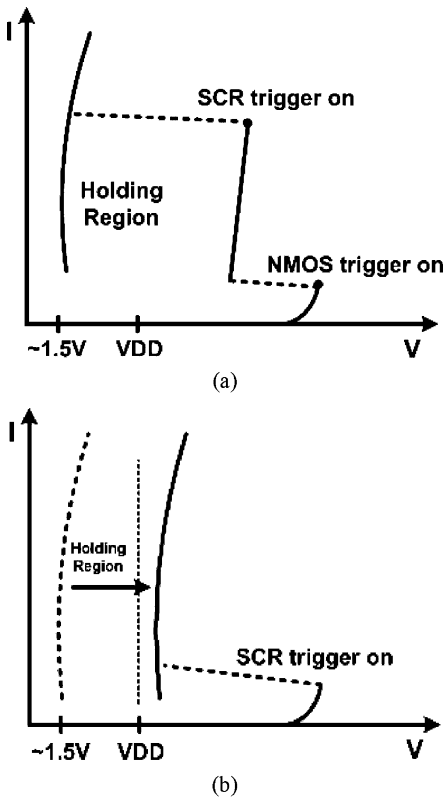

Fig. 14. Two solutions to overcome latchup issue in the ESD protection design with SCR-based device: (a) increasing the trigger current and (b) increasing holding voltage to avoid the SCR-based devices being accidentally triggered on by noise pulse.

the overshooting or undershooting noise pulses on the pads. A high-current NMOS-trigger lateral SCR (HINTSCR) device [51] has been successfully designed by adding a bypass diode into the LVTSCR structure to increase its triggering current up to 218.5 mA in a 0.6-μm CMOS process. Such HINTSCR has a noise margin greater than VDD+12 V in the 3-V application. In addition, a high holding current SCR (HHI-SCR) device [24], which is modified from the GGSCR, was reported with a holding current of $\sim$70 mA in a 0.1-μm CMOS process by adjusting the external poly resistance from $\sim$k Ω in GGSCR to only $\sim$10 Ω in HHI-SCR. The holding current of HHISCR can be also increased by adding more well ties into the P-well and N-well of HHISCR [24].

Another method immune from latchup is to increase the holding voltage of the SCR-based devices to be greater than the maximum voltage supply of VDD, as shown in Fig. 14(b). By using the epi-substrate, the holding voltage of SCR device can be increased to avoid latchup problem [52]. But, the fabrication cost of CMOS wafer will be also increased. By stacking the voltage drop elements (such as diode or the SCR devices), the SCR-based device can elevate its total holding voltage in the bulk CMOS process. The switching voltage and current can be still kept at a lower voltage level by suitable trigger-assist circuit design. A cascaded-LVTSCR structure [53] was designed to increase the holding voltage (>VDD) without degrading its ESD robustness in a 0.35-μm silicided CMOS technology. In addition, the ESD protection circuits designed with stacked STSCR devices [25], or designed with a STSCR device and

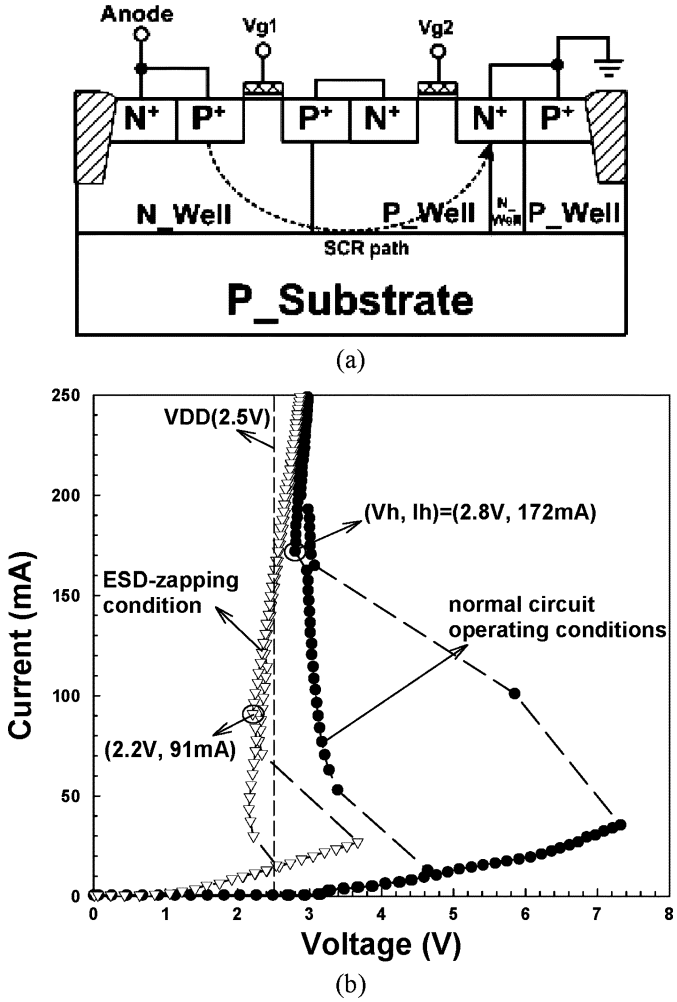

Fig. 15. (a) Device structure of dynamic holding voltage SCR (DHVSCR) in CMOS process. (b) *I–V* characteristics of the DHVSCR under normal circuit operating conditions and ESD-zapping conditions in a 0.25-μm CMOS process.

stacked diode string [26], had been reported to have 7-kV HBM ESD level and free to latchup issue in a 0.25-μm silicided CMOS technology. Recently, the holding voltage of a single SCR device can be dynamically adjusted for ESD protection (with low holding voltage) and for normal circuit operation (with higher holding voltage) [54]–[56]. A dynamic holding voltage SCR (DHVSCR) was reported to be an ESD protection device with high latchup immunity [55]. The device structure of DHVSCR is shown in Fig. 15(a). A pMOS and an nMOS are inserted into the DHVSCR device structure, as compared with the LSCR structure. The *I–V* characteristics of the DHVSCR under normal circuit operating conditions and ESD stress conditions in a 0.25-μm CMOS process are shown in Fig. 15(b). The holding voltage and holding current of DHVSCR can be adjusted by controlling the gate voltages of pMOS and NMOS, which are merged into the SCR structure [55]. Under normal circuit operating conditions, the gates (Vg1 and Vg2) of pMOS and nMOS are biased at 2.5 V (VDD), but at 0 V under ESD stress conditions. The holding voltage and holding current of DHVSCR under normal circuit operating conditions are 2.8 V and 172 mA, respectively. Thus, the DHVSCR will not be kept in the latchup state in normal circuit operating conditions with VDD of 2.5 V. However, the holding voltage and holding current of DHVSCR under ESD stress conditions are dropped to 2.2 V and 91 mA, respectively. So, the DHVSCR can clamp the overstress ESD pulse to a lower voltage level to achieve higher ESD robustness.

V. Discussion and Comparison

Moreover, with the scaled-down CMOS technologies, the power-supply voltages in CMOS ICs have been also scaled downwards to follow the constant-field scaling requirement and to reduce power consumption. For CMOS IC products realized in a 0.13-μm silicided CMOS process, the maximum supply voltage for the internal circuit has been reduced to 1.2 V, so the static latchup concern inherent in SCR-based device will vanish certainly. Therefore, SCR-based device with lower switching voltage can be a great candidate for on-chip ESD protection due to its highest ESD robustness, smallest layout area, and free to static latchup danger, as compared with other ESD protection devices. However, in a 0.13-μm CMOS process with ultrathin gate oxide of $\sim$20 Å, the turn-on speed of SCR devices should be enhanced to quickly discharge ESD overstress voltage for effectively protecting the thinner gate oxide. The NANSCR [28] and the dummy-gate structure [38], [57], [58] used to improve the turn-on speed of SCR-based device will be a better choice to protect the input stages with such ultrathin gate oxide in the nanoscale CMOS processes.

The comparison among various SCR-based devices for on-chip ESD protection has been summarized in Table I. The evaluated parameters are explained as follows:

- Switching voltage (Vt1):
  - "high": $\mathrm{Vt1} \gg \mathrm{BVox}$ (breakdown voltage of gate oxide),
  - "middle": $\mathrm{Vt1} > \mathrm{BVox}$, "low": $\mathrm{Vt1} < \mathrm{BVox}$,
  - "lower": $\mathrm{Vt1} \ll \mathrm{BVox}$, and
  - "tunable": Vt1 is adjustable.
- Turn-on speed:
  - "slow": SCR must be triggered on through breakdown mechanism and its Vt1 is greater than the BVox,
  - "middle": SCR must be triggered on through breakdown mechanism and its Vt1 is smaller than the BVox,
  - "fast": SCR can be triggered on through one active-triggered technique without involving breakdown mechanism, and
  - "faster": SCR can be triggered on through some active-triggered techniques and some layout techniques.
- V_{hold} increased required: will the standalone SCR-based devices induce the latchup issue if the supply voltage of CMOS ICs is set to 2.5 V? "Yes" or "No".
- Design complexity:
  - "high": need some well-designed auxiliary circuits and their operating range is very narrow,
  - "middle": need some well-designed auxiliary circuits and their operating range is wider, and
  - "low": the standalone SCR-based device is the ESD protection circuit without extra auxiliary circuit.
- Overall performance: based on the above parameters to evaluate the performance of the ESD protection circuits with SCR-based devices.

TABLE I
COMPARISON AMONG THE SCR-BASED DEVICES FOR ON-CHIP ESD PROTECTION

Application	SCR Category	Switching Voltage	Turn-on Speed	Latchup Issue (1)	Design Complexity	Overall Performance
Standard CMOS Process	Lateral SCR (LSCR)	high	slow	Yes	high	poor
	Modified LSCR (MLSCR)	middle	slow	Yes	high	middle
	Low-Voltage-Triggered SCR (LVTSCR)	low	middle	Yes	low	good
	Gate-Coupled LVTSCR	lower + tunable	fast	Yes	middle	better
	High-Current-Triggered LVTSCR (HINTSCR)	low	middle	No	middle	better
	High-Holding-Voltage LVTSCR	low	middle	No	high	good
	Hot-Carrier-Triggered SCR (HCTSCR)	low + tunable	slow	Yes	high	middle
	GGNMOS-Triggered SCR (GGSCR)	low	fast	Yes	low	better
	High-Holding-Current SCR (HHI-SCR) (2)	low	slow	No	middle	better
	Dual-Direction SCR	low	middle	Yes	high	good
	All-Direction SCR	low	middle	Yes	high	good
	Diode-Triggered SCR	low	fast	Yes	middle	good
	Stacked-NMOS-Triggered SCR (SNTSCR)	lower + tunable	middle	Yes	high	better
	Substrate-Triggered SCR (STSCR)	*lower + tunable*	*fast*	*Yes*	*middle*	*better*
	Double-Triggered SCR (DTSCR)	*lower + tunable*	*faster*	*Yes*	*middle*	*best*
	Dummy-Gate-Blocking STSCR	*lower + tunable*	*faster*	*Yes*	*middle*	*best*
	Native-NMOS-Triggered SCR (NANSCR)	*lower + tunable*	*faster*	*Yes*	*low*	*best*
	Dynamic-Holding-Voltage SCR (DHVSCR)	lower	fast	No	middle	better
High-Voltage Process	Mirrored Lateral SCR (MILSCR)	high	slow	Yes	low	middle
	DENMOS with Self-Aligned STI-Blocked SCR	high	slow	Yes	low	middle
	Embedded SCR LDMOS	high	slow	Yes	low	middle

(1) Some of latchup issue can be solved by stacking the multiple SCR devices to have a total holding voltage greater than the maximum voltage level of VDD or input signals of CMOS ICs.
(2) HHI-SCR can also be applied in high-voltage process.

The HBM and MM ESD levels of SCR-based devices are always superior to other non-SCR ESD protection devices. The switching voltage and the turn-on speed of SCR-based devices must be finely tuned to fully and effectively protect the ultrathin gate oxide of input stages, especially against the fast CDM ESD events. The SCR-based devices with the improved turn-on speed will be more suitable for ESD protection against CDM ESD stress. The switching voltage and turn-on speed of SCR-based devices will be the dominated factors on the overall performances of on-chip ESD protection circuits with SCR-based devices in nanoscale CMOS processes with the maximum power supply voltage smaller than 1.2 V.

VI. CONCLUSION

The ESD protection circuits designed with the various SCR-based devices in CMOS IC products have been reviewed and discussed. The SCR device can sustain the highest ESD

robustness within the smallest layout area, as compared with other non-SCR ESD protection devices. However, the SCR device generally has a higher switching voltage, which is often higher than the gate-oxide breakdown voltage in CMOS ICs. Some trigger-assist techniques had been developed to reduce the switching voltage and to improve the turn-on speed of SCR-based devices. Two solutions (by increasing the triggering current or the holding voltage) to overcome latchup issue had been developed to safely apply the SCR-based devices in the ESD protection circuits of CMOS IC products. Besides, the static latchup issue will vanish certainly when the maximum power supply voltage of CMOS IC products is smaller than the holding voltage of SCR devices. In nanoscale CMOS processes, the SCR-based devices which have low enough switching voltage and fast enough turn-on speed can effectively protect the input/output circuits against HBM and MM ESD stresses. However, SCR application could be somewhat critical for CDM protection due to a relatively slow trigger speed, as compared to the transient of CDM ESD event. Therefore, additional precaution and trigger-assist circuit must be taken in particular if SCRs are used in the advanced sub-130-nm technologies for ultrathin gate-oxide protection.

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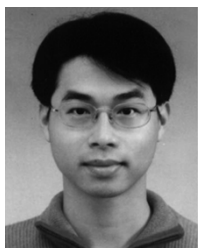

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