A 1.8-V 10-Gb/s Fully Integrated CMOS Optical Receiver Analog Front-End

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***Abstract*—A fully integrated 10-Gb/s optical receiver analog front-end (AFE) design that includes a transimpedance amplifier (TIA) and a limiting amplifier (LA) is demonstrated to require less chip area and is suitable for both low-cost and low-voltage applications. The AFE is fabricated using a 0.18-μm CMOS technology. The tiny photo current received by the receiver AFE is amplified to a differential voltage swing of 400 $mV_{(pp)}$. In order to avoid off-chip noise interference, the TIA and LA are dc-coupled on the chip instead of ac-coupled though a large external capacitor. The receiver front-end provides a conversion gain of up to 87 dBΩ and -3 dB bandwidth of 7.6 GHz. The measured sensitivity of the optical receiver is -12 dBm at a bit-error rate of 10^{-12} with a $2^{31}-1$ pseudorandom test pattern. Three-dimensional symmetric transformers are utilized in the AFE design for bandwidth enhancement. Operating under a 1.8-V supply, the power dissipation is 210 mW, and the chip size is 1028 μm$\times$ 1796 μm.**

***Index Terms*—Limiting amplifier, optical receiver, three-dimensional symmetric transformer, transimpedance amplifier.**

I. Introduction

THIS paper presents a 10-Gb/s fully integrated optical receiver that incorporates both a transimpedance amplifier (TIA) and a limiting amplifier (LA) in a single chip. In contrast with a conventional stand-alone TIA and a LA in separate packages [1]–[3], with our design the tiny photo currents generated from a photo detector can be on-chip amplified to a logic level to avoid off chip noise interference. To achieve both wide-bandwidth and high-gain design goals, three-dimensional (3-D) symmetric transformers [4] are utilized for bandwidth enhancement. Compared to using two asymmetric or one planar symmetric counterparts in a fully differential architecture, 3-D symmetric transformers greatly reduce chip size requirements. In addition, an automatic gain-control circuit (AGC) is built in to adjust the conversion gain of TIA, avoiding any timing jitter induced by signal overload. To the authors' knowledge, this is the first 10-Gb/s CMOS optical receiver AFE that integrates both a TIA and a limiting amplifier on a single chip.

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This paper begins with a description of the receiver AFE architecture and the use of inductive peaking for bandwidth enhancement in the broad-band amplifier design. Then the novel 3-D fully-symmetric transformer utilized in the AFE design is explained. Compared to the prior designs of planar symmetric [5] or stacked asymmetric [6], [7] structures, the chip area needed can be drastically reduced using the proposed 3-D transformers. Following the narrative on the 3-D transformer, the designs of the transimpedance amplifier, the AGC and the limiting amplifier are discussed. The gain-bandwidth requirement and power optimization are investigated in detail as well. Finally, the experimental results and our conclusion are presented.

II. Receiver Analog Front-End Architecture

Fig. 1 shows the receiver architecture, which integrates a transimpedance amplifier, an AGC, and a limiting amplifier on a single chip [8]. To alleviate bandwidth degradation caused by the parasitic capacitors of the photo detector and the IC package, a regulated cascode (RGC) topology is adopted as the input stage [9]. The TIA architecture is in a pseudodifferential configuration with a shunt-feedback for higher common-mode noise immunity. Furthermore, an AGC loop is built in to avoid data jitter induced by signal overload. As the TIA's output swings below a predetermined voltage level, the tunable feedback resistors M_{f1} and M_{f2} are switched off and the TIA is operated in the high-gain mode for low-noise performance. Otherwise, the AGC is activated to keep the output amplitude constant. The AGC is composed of an amplitude detector, a comparator, and an integrator [10]. The comparator generates a compensating current to charge or discharge the integrator, and the conversion gain of TIA can be adjusted by reducing the shunting resistance in the input stage. The single-ended TIA output is converted to a fully differential signal by the A_{sd} amplifier in conjunction with the R_1 and C_1 low-pass filter.

The LA consists of a chain of five gain cells, an offset cancellation circuit (A_0), a low-pass feedback filter $(A_{fb}, R_2, R_3, R_4, R_5, C_2, C_3, C_{ext})$, and a current-mode output buffer to drive a 50-Ω output load. In the feedback path, an additional gain cell (A_{fb}) is utilized to isolate the loading effects produced by the feedback network. C_2 and C_3 are MOS capacitors while C_{ext} is placed externally so it can have a lower $f_{L-3\text{dB}}$ frequency. The gain stage is chosen as a compromise between gain and bandwidth requirements [8].

In this design, the TIA converts the photo currents generated from the photo detector into a voltage signal for post amplification, and the LA amplifies the voltage swing to a logic level for data recovery. The TIA is directly coupled to the LA on the chip,

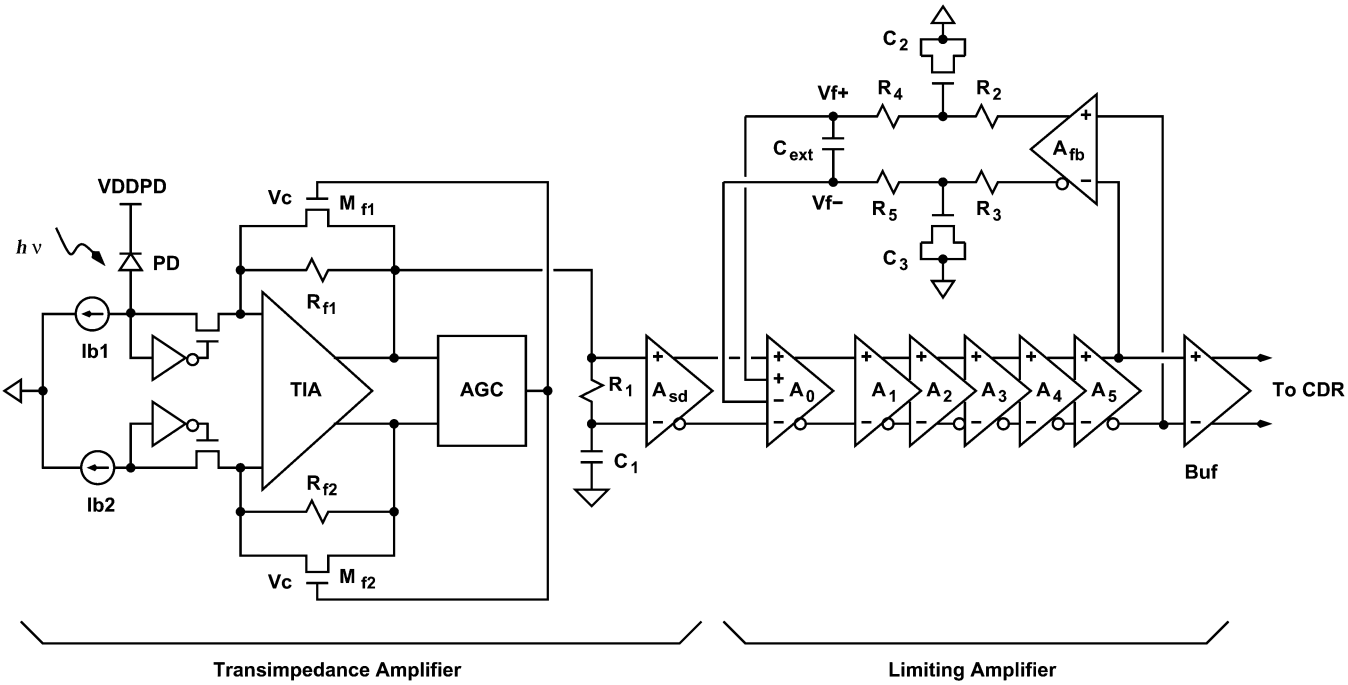

Fig. 1. Optical receiver analog front-end architecture.

so no external coupling capacitors are required to avoid noise interference. Additionally, no broad-band matching networks are required in the input stage of the LA and the output stage of the TIA, resulting in reduced power dissipation and alleviating gain loss in the buffer stage. Herein, an automatic dc-level control circuit is incorporated at the output stage of the TIA for dc matching between the TIA and the post amplifier.

III. 3-D Transformer

As the supply voltage continues to scale down along with the shrinkage of device size, the design of a wide-band and high-gain amplifier becomes more and more challenging due to the limitation of voltage headroom. An attractive solution for low-voltage broad-band amplifier design is by means of inductive peaking [11], which is applied in the designs of both the TIA and the LA. As the LA is composed of several gain stages and thus requires many bulky inductors, it occupies significant chip area. To achieve a low-cost design goal, a single innovative 3-D inverting-type transformer is utilized instead of two inductors in the fully differential gain stage.

Fig. 2(a) illustrates the 3-D transformer architecture and Fig. 2(b) displays its cross-sectional view. The metal wire winds downward with a right-half turn on the upper layer interleaved with a left-half turn on the adjacent lower layer and vice versa. When the wire reaches the bottom layer, it winds upward along the counter-path. The inverting type transformer is formed by center-tapping the middle point of the metal wire to a common-mode voltage, which is $V_{\rm DD}$ in this design.

The distributed and lumped-circuit models of the 3-D transformer are illustrated in Fig. 3(a) and (b) respectively. Here, $R_{s1,i}$ and $R_{s2,i}$ represent the distributed resistance of L_1 and L_2 on metal layer i. $C_{1,jk}$ and $C_{2,jk}$ denote the parasitic capacitance of L_1 and L_2 between metal layer j $(= 6, 5, 4, 3, 2)$,

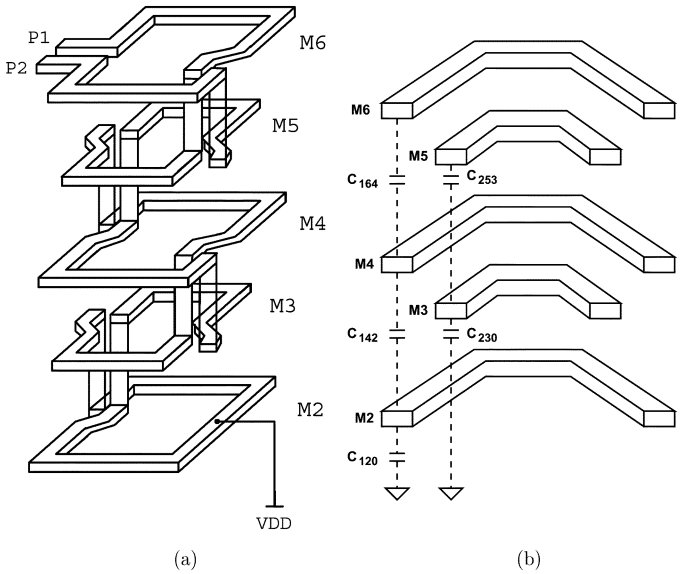

Fig. 2. (a) 3-D symmetric transformer architecture. (b) Cross-sectional view of 3-D transformer.

k $(= 4, 3, 2)$, and substrate k $(= 0)$. The outer radius of the loops on the adjacent layers are offset by the metal width, so that loops on M6, M4, and M2 have the same radius, while that of loops on M5 and M3 is smaller. Thus, the parasitic capacitance between the adjacent metal layers can be eliminated.

In addition, $C_{1,jk}$ and $C_{2,jk}$ are reduced by increasing the distance between metal plates, and the electrical potential between the top and bottom plates can be minimized [4]. Thus, the effective parasitic capacitance of the 3-D transformer can be reduced, resulting in better self-resonant frequency (f_{sr}). Furthermore, by means of the interleaving architecture in a relatively smaller area, the effective inductance in each branch is

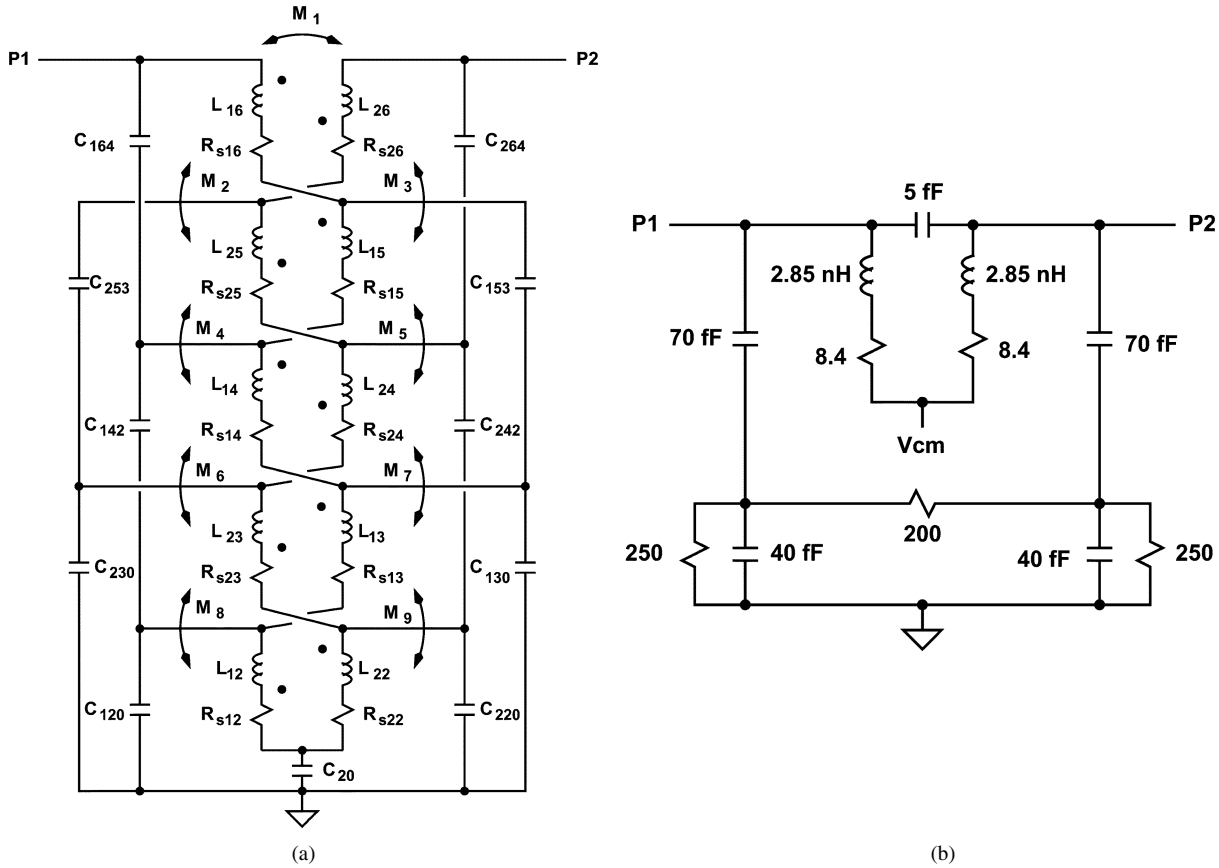

Fig. 3. (a) 3-D symmetric transformer distributed model. (b) 3-D symmetric transformer lumped model.

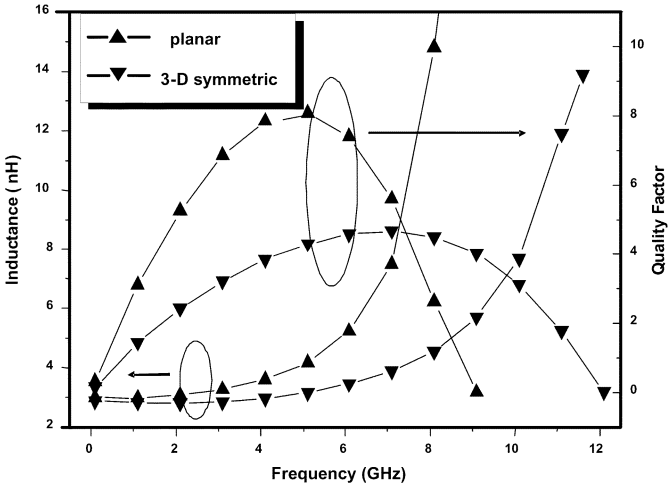

Fig. 4. Planar versus 3-D symmetric transformer performance comparison.

increased by enhancing the mutual coupling of the transformer (M), including the magnetic coupling on the same layer (M_1) and adjacent layer $(M_2$–$M_9)$. Thus, the total wire length of the 3-D transformer can be reduced and configured in a small area.

Fig. 4 compares the simulated performance of the proposed 3-D transformer with that of a conventional planar counterpart by ADS momentum. For an inductor pair with an inductance of 2.85 nH in each branch, five turns, metal width $= 10\ \mu$m, metal spacing $= 1.5\ \mu$m, and an inner diameter of 110 μm, the chip area of 3-D transformer is 47% smaller than that of its planar counterparts. Also it manifests a higher self resonant frequency (12 GHz versus 9 GHz) due to a smaller effective parasitic capacitance [4]. Although its quality factor may be degraded due to the use of lower metal layer, along with higher series resistance introduced by vias, this is not an issue for bandwidth enhancement applications.

IV. Circuit Design

A. TIA Circuit Schematic

Fig. 5 provides a detailed circuit schematic of the TIA, which is composed of a regulated cascode (RGC) input stage $(M_1$–$M_4)$, followed by a common-source gain stage $(M_5$–$M_6)$ with a shunt feedback [9]. R_{f1} and R_{f2} are made up of poly resistors. The right half circuit $(M_7$–$M_{12})$ is a replica of TIA for

$$T_z = (1 - g_{m5}R_F)\frac{R_F R_{c1}}{R_{c1}+R_F} \times \frac{1+s/z_1}{1+s/(\omega_{n1}Q_1)+s^2/\omega_{n1}^2} \times \frac{1+s/z_2}{(1+s/p_1)(1+s/(\omega_{n2}Q_2)+s^2/\omega_{n2}^2)-(1-g_{m5}R_F)R_{c1}/(R_{c1}+R_F)(1+s/z_2)} \quad (1)$$

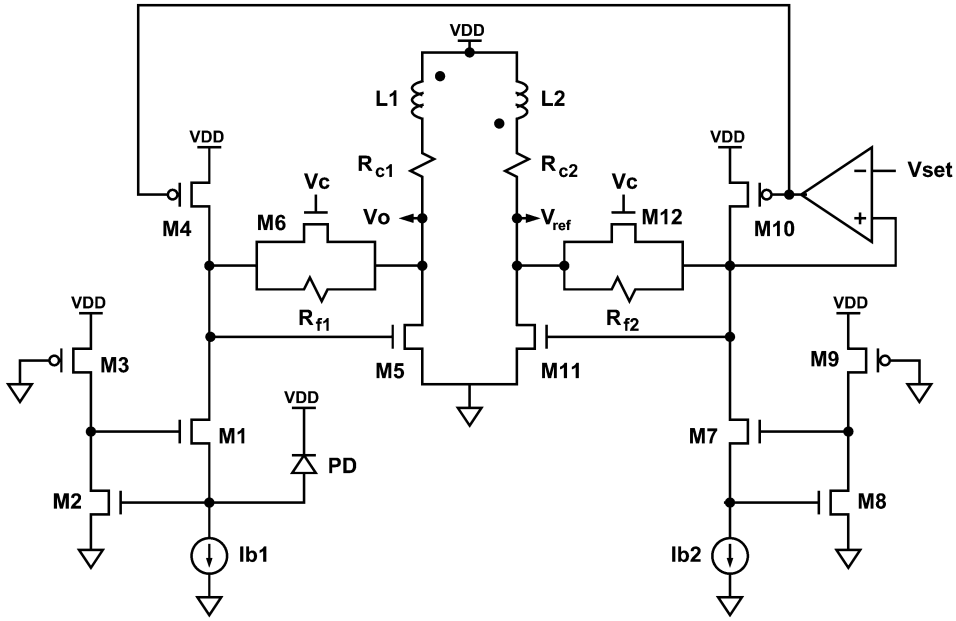

Fig. 5. Transimpedance amplifier circuit schematic.

dc level and automatic gain control. The input common-mode voltage of the shunt-feedback gain stage is preset to V_{set} by the local feedback amplifier, and $V_{\rm ref}$ is utilized as a reference voltage for the AGC.

The closed-loop conversion gain of the TIA can be approximated by (1), shown at the bottom of the previous page, where

$$z_1 = \frac{g_{m2}+g_{m3}+g_{ds2}+g_{ds3}}{C_{p1}}$$
$$z_2 = \frac{R_{c1}}{L_1} \quad p_1 = \frac{1}{R_F C_{p2}} \tag{2}$$
$$Q_1\omega_{n1} = \left[\frac{C_{p1}}{g_{m3}+g_{m2}+g_{ds2}+g_{ds3}} + \frac{C_{pd}(g_{m3}+g_{ds2}+g_{ds3})}{g_{m1}(g_{m2}+g_{m3}+g_{ds2}+g_{ds3})} + \frac{C_{gs1}}{g_{m1}}\right]^{-1} \tag{3}$$
$$\omega_{n1}^2 = \frac{g_{m1}(g_{m2}+g_{m3}+g_{ds2}+g_{ds3})}{C_{p1}C_{gs1}+C_{p1}C_{pd}} \tag{4}$$
$$Q_2\omega_{n2} = \frac{R_{c1}+R_F}{C_0R_FR_{c1}+L_1} \quad \omega_{n2}^2 = \frac{R_{c1}+R_F}{R_FC_0L_1}. \tag{5}$$

Here $R_F = (R_{f_1} \parallel R_{M6_{\rm on}})$, C_{pd} denotes the total capacitance at the input node, C_{p1} denotes the total parasitic capacitance at the drain of M_2, C_{p2} denotes the total parasitic capacitance at the drain of M_4, and C_o is the parasitic capacitance at the output node of M_5. The TIA is basically a fifth-order filter. The second term in (1) is contributed by the regulated cascode input stage, while the third term is determined by the shunt feedback amplifier in the second stage. The RGC input stage provides low input impedance in order to alleviate the severe bandwidth degradation caused by the parasitic capacitance (C_{pd}) of the photo detector [9]. In addition, the RGC input stage introduces another zero, z_1, which can be placed at the roll-off region of the gain curve for bandwidth extension.

On the other hand, the p_1 pole is introduced by the parasitic capacitance at the output of the common gate gain stage. The z_2 zero, which is generated by an inductive peaking technique, can be placed at the vicinity of p_1 to alleviate its impact on bandwidth limitations. Thus, (1) can be simplified as

$$T_z = \frac{R_{c1}(1-g_{m5}R_F)}{1+g_{m5}R_{c1}} \times \frac{1+s/z_1}{1+s/(\omega_{n1}Q_1)+s^2/\omega_{n1}^2} \times \frac{1}{1+s/(\omega_{n0}Q_0)+s^2/\omega_{n0}^2} \tag{6}$$

where

$$Q_0\omega_{n0} = \frac{R_F(1+g_{m5}R_{c1})}{R_{c1}+R_F} \times \omega_{n2}Q_2$$
$$\omega_{n0} = \sqrt{\frac{R_F(1+g_{m5}R_{c1})}{R_{c1}+R_F}}\omega_{n2}. \tag{7}$$

Since the RGC input stage is transparent to the photo current by choosing $\omega_{n1} > \omega_{n0}$, it turns out that the TIA bandwidth can be extended to ω_{n0} using shunt feedback and inductive peaking. At the same time, Q_0 is chosen for a maximally-flat Butterworth response.

The price paid in the RGC input stage is the extra noise introduced by the RGC feedback amplifier. The input-referred noise can be derived as [9]

$$\overline{i_{eq}^2} = 4kT\gamma(g_{m,Ib1}+g_{m4}) + 4kT\gamma g_{m6} + \frac{4kT}{R_{f1}} + \frac{4kT\gamma}{(g_{m2}+g_{m3})}\left[g_{ds,Ib1}^2+\omega^2(C_{\rm in}+C_{gs2})^2\right] + \frac{4kT(\gamma g_{m5}+\frac{1}{R_{c1}})\omega^2(C_{g5}+C_{d1})^2}{g_{m5}^2} + \frac{4kT\left[\frac{1}{R_{f1}}+\gamma(g_{m1}+g_{m6}+g_{m4})\right]\omega^2(C_{gs1}+C_{gd2})^2}{g_{m1}^2} \tag{8}$$

where γ is the noise factor of the MOSFET, $C_{\rm in}$ is the parasitic capacitance at the input node, and C_{g5} and C_{d1} respectively rep-

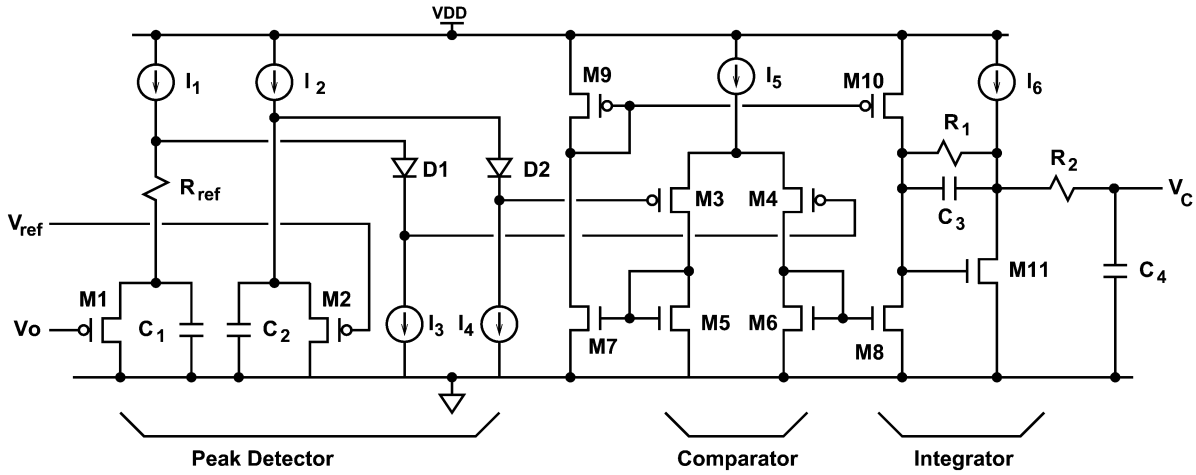

Fig. 6. Amplitude detector for AGC.

resent the total parasitic capacitance at gate of M5 and drain of M1. To mitigate this drawback, the transconductance of M2 is chosen to be as large as possible to reduce the input-referred noise coming from M2 and M3's thermal noise [9]. Additionally, the tail current source needs to be sufficiently large to tolerate the input dynamic range.

B. Automatic Gain Control Circuit

In the high-input current state, the common-source amplifiers in the second stage of the TIA may be driven into the deep triode region, which results in overload-induced data jitter. To mitigate this effect, the feedback resistors are adjusted by turning on the shunting resistance of M_6 and M_{12}. On the contrary, when the input current is below a predetermined threshold level, the shunting transistors are turned off for low-noise operation.

Fig. 6 shows the detailed circuit schematic of the AGC, which is comprised of a peak detector (M1, M2, C1, C2) followed by an operational transconductance amplifier (OTA) for amplitude comparison (M_3–M_{10}), a lossy integrator stage (M_{11}, R_1, C_3), and a low-pass filter (R_2, C_4) [10]. The loop bandwidth of the AGC is mainly determined by $1/R_2C_4$. Here M_1 acts as the nonlinear rectifying element on the output signal of the TIA. The threshold voltage of AGC is determined by $I_1R_{\rm ref}$. When the input photo current is low, the OTA is fully switched and the V_c is pulled low. Thus, the feedback resistor M_6 and M_{12} in the TIA core are switched off for high-gain and low-noise performance. On the contrary, as the photo current becomes higher, the TIA's output node, V_o, is driven to be lower. Thereafter, the OTA (M_3–M_{10}) would sense the voltage difference and generate the compensation current to charge or discharge the integrator, whose output V_c is utilized to control the turn-on resistance of M_6 and M_{12} in the TIA core. Fig. 7 shows the simulated transimpedance gain and output swing (single ended) under various input current levels by the automatic gain control loop. The figure reveals a conversion gain of 450 Ω in the nominal case and 150 Ω in the high-current state.

C. Limiting Amplifier Circuit Schematic

For an LA design, how to determine the number of gain stages with gain-bandwidth tradeoffs is an important issue. Assuming

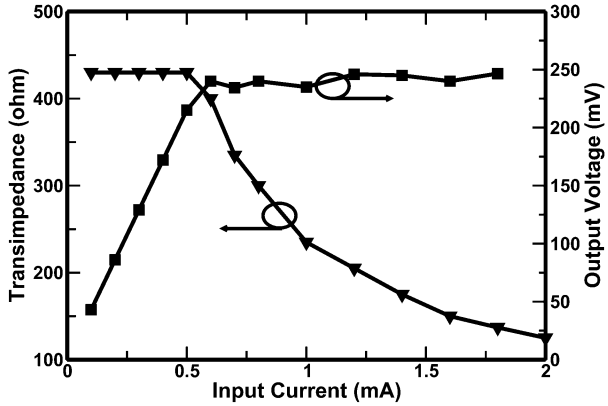

Fig. 7. Transimpedance gain and output swing versus input current.

each gain cell is identical and approximated by a two-pole amplifier, and its conversion gain can be described by $A(s)$, where

$$A(s) = \frac{A_s \cdot \omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}. \tag{9}$$

Here A_s denotes the small-signal dc gain, ζ is the corresponding damping factor, and ω_n is the natural frequency. Let the -3-dB bandwidth of a single-stage amplifier be ω_s, then the -3-dB bandwidth of the N stage's cascaded limiting amplifier is reduced to ω_c. It can be derived that

$$\omega_c = \left[1 - 2\zeta^2 + \sqrt{(1-2\zeta^2)^2 + 2^{1/N} - 1}\right]^{1/2} \omega_n. \tag{10}$$

For a flat response, we want to have $\zeta \approx \sqrt{2}/2$. Also, the bandwidth requirement for a single-stage amplifier (ω_s) in terms of the cascaded amplifier's -3-dB bandwidth (ω_c) can be derived as

$$\omega_s = \left(\frac{1}{2^{1/N} - 1}\right)^{1/4} \omega_c. \tag{11}$$

On the other hand, the gain requirement of the individual stage, A_s, in terms of the LA's conversion gain, A_c, can be expressed as

$$A_s = A_c^{1/N}.$$

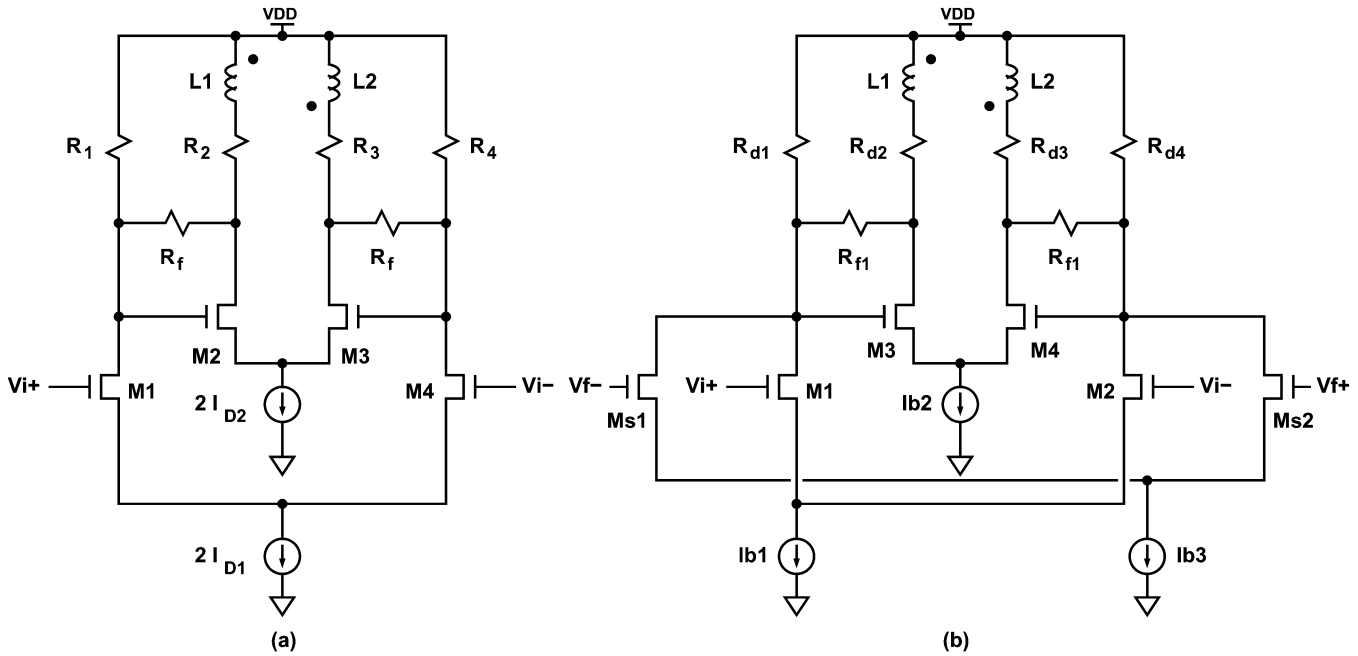

Fig. 8. Gain cell of limiting amplifier.

Under the above assumptions, one can easily derive the required unity gain bandwidth (ω_u) for the individual stages in terms of the targeted A_c and ω_c, where

$$\omega_u = \omega_c \times \left(\frac{1}{2^{1/N}-1}\right)^{1/4} \times \left(A_c^{2/N}-1\right)^{1/4}. \tag{12}$$

To achieve a conversion gain of 40 dB and −3-dB bandwidth of 10 GHz (ω_c), a five-stage limiting amplifier demands a ω_u of 24 GHz per stage, which is feasible for a 0.18 μm CMOS technology. Since the last two stages of cascaded amplifiers behave more like current switches as the gate drive of differential pairs becomes larger and larger, the bandwidth degradation caused by the last two stages becomes negligible [12]. The ω_u actually required would be more relaxed. On the other hand, although the ω_u for each stage can be reduced by choosing a larger N, the total power consumption and noise would be increased gradually [2], [8]. Thus, a five-stage architecture is chosen in this design.

Fig. 8(a) shows the LA's core circuit, which is based on the Cherry–Hooper circuit architecture [13] with inductive peaking. By shunt-shunt feedback, all the nodes in the circuit become low impedance nodes for wide bandwidth operations. The input stage of the LA is shown in Fig. 8(b), and it functions as both an input buffer and an offset subtractor. The offset voltage derived from the low-pass loop filter is converted to a compensation current and subtracted from the input signal. In addition, the input/output common-mode voltages of the transconductance and transimpedance amplifiers are designed to be equal for dc-coupling as the cascaded amplifiers are hooked up.

For the wide-band multistage amplifier, each gain cell is designed with an emphasis on minimizing power dissipation under the targeted specifications. To simplify the analysis, the transformer for inductive peaking is neglected temporarily. The voltage gain of each cell can be derived as

$$\frac{V_{\text{out}}(s)}{V_{\text{in}}(s)} = g_{m1}R_2(g_{m2}R_f-1)\frac{1-\frac{s}{z_1}}{As^2+Bs+C} \tag{13}$$

where

$$\begin{aligned}
A &= R_fR_2(C_L+C_{gd2})(C_{gs2}+C_{ds1}) + R_2R_fC_{gd2}C_L \\
B &= (R_2+R_f)(C_{gs2}+C_{ds1}) + R_2R_f(C_L+C_{gd2}) \\
&\quad \times \left[\frac{1}{R_1}+g_{m2}\right] + R_fC_{gd2} + C_LR_2(1-g_{m2}R_f) \\
C &= (R_2+R_f)\left[\frac{1}{R_1}+g_{m2}\right] + 1 - g_{m2}R_f \\
z_1 &= \frac{g_{m2}R_f-1}{R_fC_{gd2}} \quad \zeta = \frac{B}{2\sqrt{A\cdot C}} \quad \omega_n = \left(\frac{C}{A}\right)^{1/2}
\end{aligned} \tag{14}$$

$$\omega_{-3\text{dB}} = \left(1-2\zeta^2+\sqrt{(2\zeta^2-1)^2+1}\right)^{1/2}\cdot\omega_n. \tag{15}$$

Assuming

$$\begin{aligned}
I_{D1}R_1 &= I_{D2}R_2 = V_{\text{DD}}/2 \\
(W/L)_{M1} &: (W/L)_{M2} = 1:K \\
I_{D1} &: I_{D2} = 1:K
\end{aligned} \tag{16}$$

then we have

$$\begin{aligned}
g_{m1} &= \frac{g_{m2}}{K} = \frac{I_{D1}}{V_{\hat{G}}} \quad R_1 = KR_2 = \frac{V_{\text{DD}}}{2I_{D1}} \\
I_{\text{tot}} &= 2(I_{D1}+I_{D2}) = 2(1+K)I_{D1} \\
C_{gs2} &= KC_{gs1} \quad C_{gd2} = KC_{gd1}
\end{aligned} \tag{17}$$

$$C_{ds2} = KC_{ds1} \quad C_L \approx \frac{4}{3}C_{gs1}. \tag{18}$$

Given the supply voltage V_{DD} (1.8 V), overdrive voltage $V_{\hat{G}}$ ($\approx$ 200 mV), and conversion gain of each stage (8 dB),

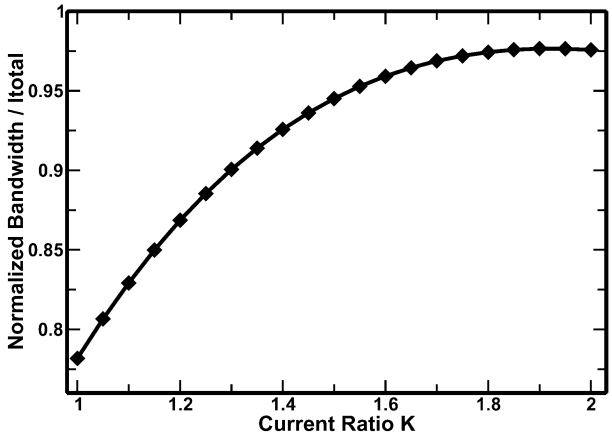

Fig. 9. Normalized $\omega_{-3\mathrm{dB}}/I_{\mathrm{tot}}$ as a function of current ratio K.

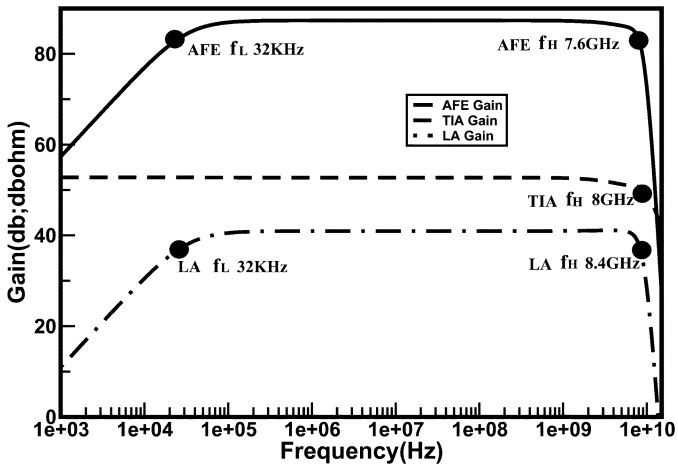

Fig. 10. Simulated gain-bandwidth response of the optical receiver AFE.

the feedback resistor R_f can be expressed in terms of K and I_{D1} by substituting (17) for (13). Also, the normalized -3-dB bandwidth $(\omega_{-3\mathrm{dB}})$ can be obtained by substituting (17) and (18) into (15). Taking power dissipation into consideration, the normalized $(\omega_{-3\mathrm{dB}}/I_{\mathrm{tot}})$ is chosen as a figure of merit and its relation to K is illustrated in Fig. 9. It can be shown that the achievable bandwidth at the cost of I_{tot} becomes saturated as K approaches 1.6. It corresponds to $R_f = 205\ \Omega$ and $I_{\mathrm{tot}} = 13$ mA per stage in this design. From another perspective, if K is too large, the achievable bandwidth becomes limited by the input pole of the transimpedance gain stage.

V. Simulation and Experimental Results

As the TIA and the LA are fully integrated on a single chip, it becomes difficult to measure and characterize their gain and bandwidth performance separately in this prototype. Fig. 10 shows the simulated gain response of the TIA, the post limiting amplifier (LA), and the optical receiver AFE when the two components are hooked up. The figure reveals that the conversion gain and the $f_{-3\mathrm{dB}}$ of the TIA and the LA are 53 dBΩ, 8 GHz, and 40 dB, 8.4 GHz, respectively. As the insertion loss of the inter-stage buffer is about 6 dB, the AFE provides a total gain of 87 dBΩ, and the -3-dB bandwidth is 7.6 GHz.

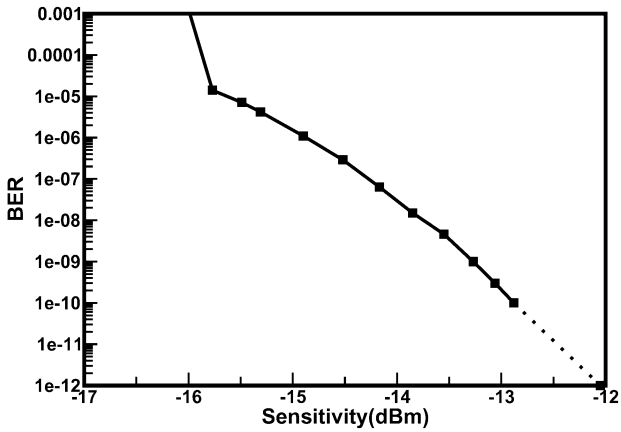

Fig. 11. 10-Gb/s bit-error rate performance with $2^{31}-1$ PRBS input.

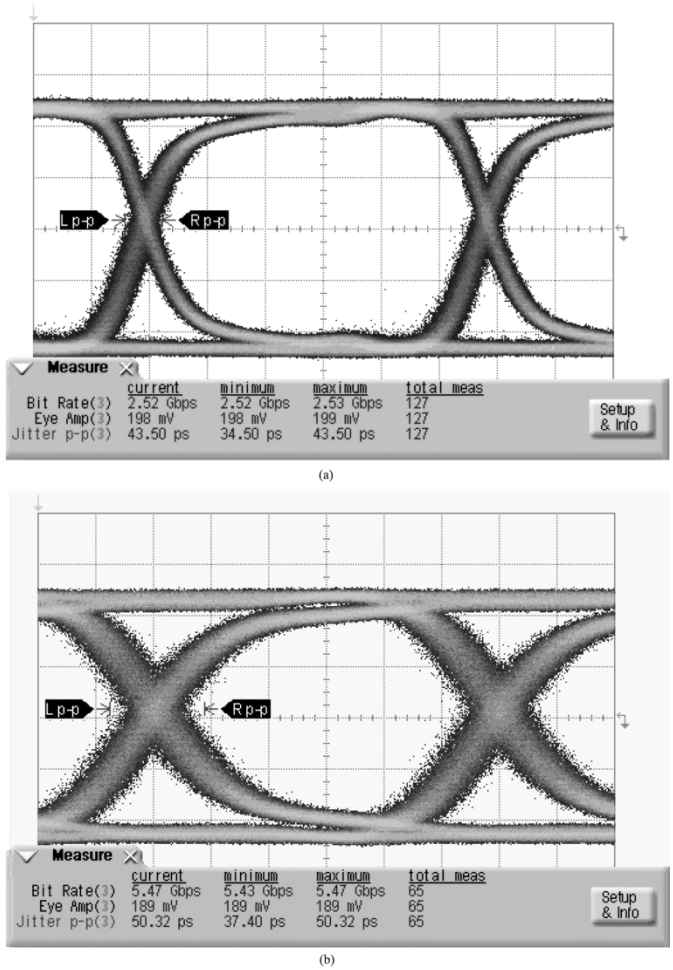

Fig. 12. (a) 2.5-Gb/s eye diagram with -16.8 dBm input power BER $= 10^{-12}$. y-scale: 43.9 mV/div, x-scale: 67.5 ps/div. (b) 5-Gb/s eye diagram with -16.2 dBm input power at BER $= 10^{-12}$. y-scale: 43.7 mV/div, x-scale: 30.6 ps/div.

With an Oepic P5030A photo detector, whose responsivity is 0.85 A/W and parasitic capacitance is about 0.15 pF, the measured sensitivity of the optical receiver AFE at 10 Gb/s is about -12 dBm for a bit-error rate of less than 10^{-12}. The bit-error rate performance at 10 Gb/s is summarized in Fig. 11. The tolerated power level is up to 0 dBm by the built-in automatic gain

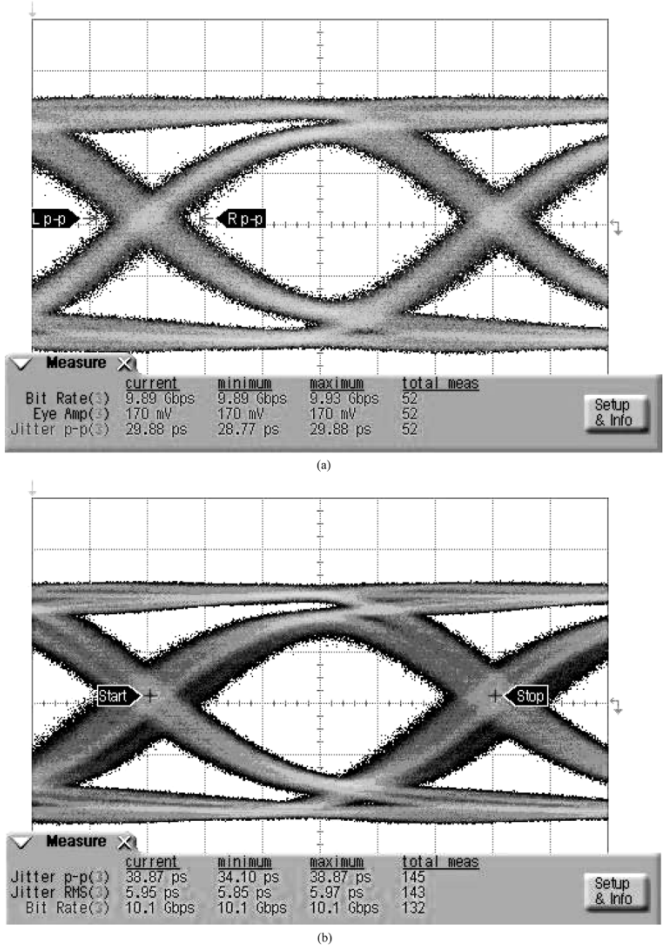

Fig. 13. (a) 10-Gb/s eye diagram with -12 dBm input power (sensitivity level) at $\mathrm{BER} = 10^{-12}$. y-scale: 43.6 mV/div, x-scale: 16.6 ps/div. (b) 10-Gb/s eye diagram with 0 dBm input power (overload level) @$\mathrm{BER} = 10^{-12}$. y-scale: 50 mV/div, x-scale: 16.5 ps/div.

control scheme. The input-referred noise current, I_N, of the optical receiver is derived from its sensitivity performance. As

$$\text{Sensitivity} \approx 10\log\left[\frac{14.1 I_N (r_e+1)}{2\rho(r_e-1)}1000\right] \text{ dBm} \qquad (19)$$

where ρ is the responsivity of the photo detector, and r_e is the extinction ratio. The corresponding I_N is approximately 7.3 $\mu\mathrm{A_{rms}}$.

Fig. 12(a) and (b) illustrate the measured eye diagrams at 2.5 and 5.5 Gb/s, respectively. The data jitter is about 43.5 ps (pp) for 2.5 Gb/s and 50.3 ps (pp) for 5.5 Gb/s. In these two cases the input sensitivity of the AFE is up to -16 dBm for bit-error rate less than 10^{-12}. Fig. 13(a) illustrates the measured 10-Gb/s eye diagram at the input power of sensitivity level (-12 dBm), Fig. 13(b) illustrates the measured 10-Gb/s eye diagram when the input power is overloaded. The measured jitter is about 29.8 and 38.8 ps, respectively. In all cases the test pattern is $2^{31}-1$ pseudorandom bit stream (PRBS). Operating under a 1.8-V supply, the power dissipation is 210 mW, of which 40 mW is consumed by the output buffer. Fig. 14 illustrates the chip photograph. Fabricated in a 0.18-μm CMOS technology, the chip size is 1028 μm$\times$ 1796 μm, of which the TIA occupies

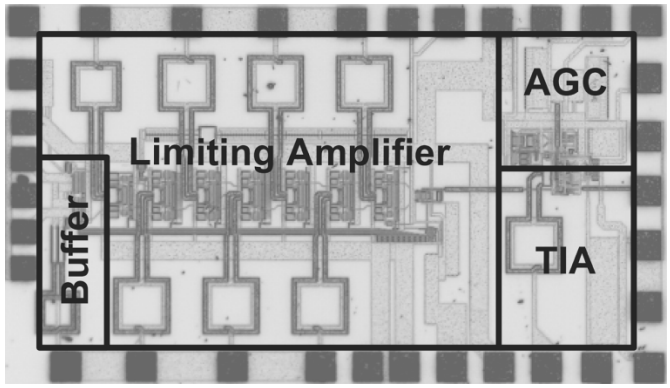

Fig. 14. Optical receiver AFE chip photograph.

a chip area of 330 μm$\times$ 550 μm. The area that the LA occupies on the chip is 1170 μm$\times$ 865 μm.

VI. Conclusion

This paper describes the design of a fully integrated 10-Gb/s optical receiver analog front-end using a generic 0.18-μm CMOS technology. The optical AFE provides a conversion gain of 87 dBΩ and a -3-dB bandwidth of about 7.6 GHz. The bandwidth is limited by the transimpedance amplifier for low-noise operation. A regulated cascode input stage is utilized to decouple the loading effect at the input node, and a wide bandwidth is achieved by means of shunt feedback and inductive peaking. Instead of using bulky planar inductors or two asymmetric 3-D inductors, our design utilizes an innovative, fully symmetric 3-D transformer for inductive peaking in each differential pair. With this innovation, the chip area can be greatly reduced. Moreover, an AGC is built in to alleviate overload-induced data jitter. Our proposed architecture is suitable for both low-cost and low-voltage applications.

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