High-Performance Poly-Silicon TFTs Incorporating $LaAlO_3$ as the Gate Dielectric

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***Abstract*—We have integrated a high-κ $LaAlO_3$ dielectric into low-temperature poly-Si (LTPS) thin-film transistors (TFTs). Good TFT performance was achieved—such as a high drive current, low threshold voltage and subthreshold slope, as well as an excellent on/off current ratio and high gate-dielectric breakdown field. This was achieved without hydrogen passivation or special crystallization steps. The good performance is related to the high gate capacitance density and small equivalent-oxide thickness provided by the high-κ dielectric.**

***Index Terms*—High-κ, $LaAlO_3$, thin-film transistors (TFTs), threshold voltage.**

I. Introduction

LOW-TEMPERATURE POLY-Si (LTPS) thin-film transistors (TFTs) are used for active matrix liquid crystal displays (AMLCDs) on glass substrates [1]–[9]. However, a difficult technological challenge is to develop high-performance TFTs that are useful for both pixel and display circuits [1]. Pixel TFTs need to operate at high voltages with low gate-leakage currents, to drive the liquid crystal. In contrast, high-speed display circuits require TFTs to operate at low voltages and high drive currents, with a low threshold voltage ($V_{\rm th}$). In this letter, we report high-κ [10]–[13] $LaAlO_3$ gate dielectric TFTs which show a high breakdown voltage and transistor drive current at 5 V. In addition to the very high-κ ($\sim$23), the $LaAlO_3$ has good device reliability of low bias-temperature Instability among high-κ CMOS devices [10]. The performance is due to the increase, by a factor of $\kappa_{\rm dielectric}/\kappa_{\rm SiO_2}$, in the gate capacitance density. This lowers the $V_{\rm th}$ and improves both the gate-leakage current and breakdown field, since the thickness of the high-κ dielectric layer can be increased. Although the high-κ Al_2O_3 TFT was previously reported [14], the relative lower κ of 9–10 [12], [13] and gate capacitance have smaller effect to lower down the $V_{\rm th}$. The $LaAlO_3$ TFTs showed a low $V_{\rm th}$ of 1.2 V, a high gate-dielectric breakdown field of 6.3 MV/cm, low subthreshold swing of 0.31 V/dec, high field-effect mobility of 40 cm^2/Vs, a large on-off-state drive current ratio ($I_{\rm on}/I_{\rm off}$) of 1.5×10^6 and high drive current up to 21 μA/μm. The high breakdown voltage and high transistor drive current suggest that the $LaAlO_3$ TFTs can meet the device requirements for both pixel and display circuits.

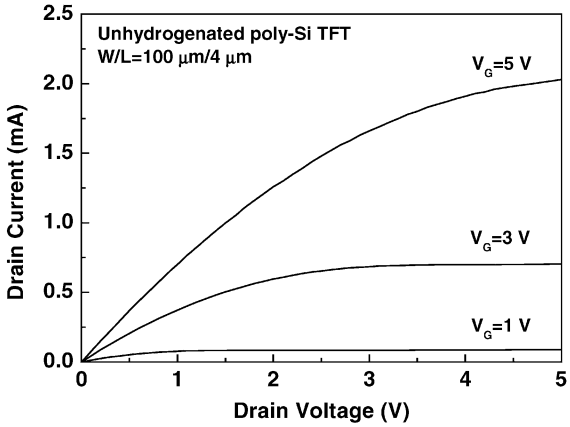

Fig. 1. Output characteristics (I_d–V_d) for a $LaAlO_3$ gate dielectric poly-Si TFT.

II. Experimental Details

Fabrication of the TFTs started with the formation of a poly-Si film, by depositing 100-nm amorphous Si on SiO_2–Si wafers (using LPCVD at 550 °C [3]), followed by crystallization at 600 °C and 20-h annealing in N_2. Then 500-nm-thick PECVD oxide was deposited for isolation and device active region was formed by patterning and etching the isolation oxide. The source and drain regions in the active device region were implanted with phosphorus (35 KeV at 5×10^{15} cm^{-2}) and activated at 600 °C for 12-h annealing under N_2. Then the 50-nm-thick $LaAlO_3$ gate dielectric was deposited on previously patterned active region by sputtering from a $LaAlO_3$ source with 150-W power and 30-sccm Ar flow rate. A 400 °C and 30 min furnace O_2 treatment was applied to improve the gate oxide quality. The TFT devices were completed by gate definition using H_3PO_4:HNO_3:CH_3COOH:H_2O (50:2:10:9) etching, contact formation, Al electrode patterning, and 400 °C N_2 sintering for 30 min. The fabricated device has gate length and width of 4 and 100 μm, respectively.

III. Results and Discussion

The output characteristics (I_d–V_d) of a high-κ $LaAlO_3$ TFT are shown in Fig. 1. The large drive current of 21 μA/μm, at 5 V, is attractive for high-speed display ICs. This good performance is related to the high gate-capacitance of 3.9×10^{-7} F/cm^2 from capacitance–voltage measurements, which gives a small equivalent-oxide thickness (EOT) of 8.7 nm at a κ value of $\sim$22.5 [10], [11]. This is the thinnest reported EOT TFT so far [3]–[6]. Our

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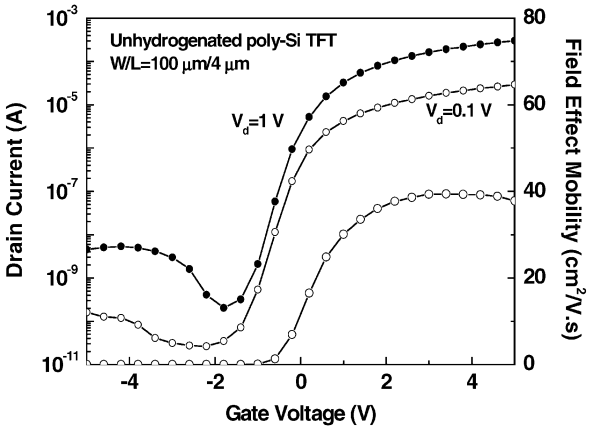

Fig. 2. Transfer characteristics (I_d–V_g) of a $LaAlO_3$ gate dielectric poly-Si TFT at $V_{\rm d} = 1$ and 0.1 V for the drain current, and at $V_{\rm d} = 0.1$ V for the field-effect mobility $\mu_{\rm FE}$.

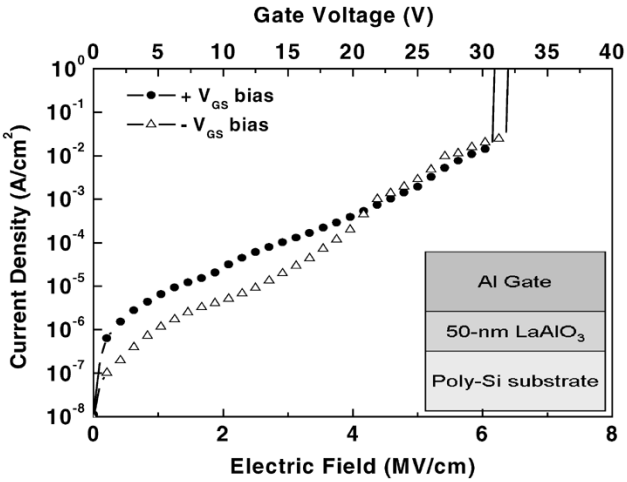

Fig. 3. Dependence of the gate current density on electric field (*J*–*E*), for a 50-nm-thick $LaAlO_3$ gate dielectric poly-Si TFT. The inset shows the layer structure.

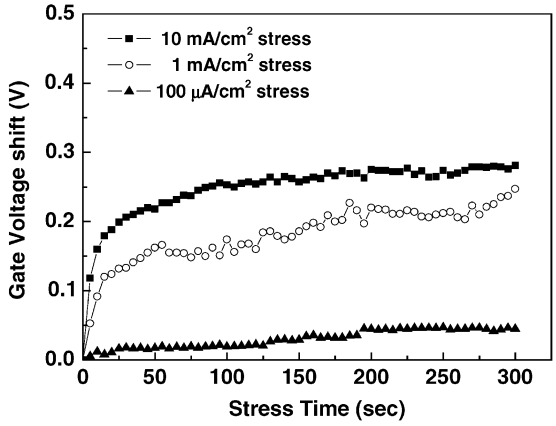

Fig. 4. Gate voltage shift of a $LaAlO_3$ gate dielectric poly-Si TFT under constant-current stress with current densities of 100, 1, and 10 mA/cm^2, respectively.

TABLE I
COMPARISON OF n-CHANNEL POLY-Si TFTs CREATED WITH A FURNACE-CRYSTALLIZATION PROCESS FOR $LaAlO_3$, LPCVD SiO_2, AND PECVD TEOS OXIDES AS GATE DIELECTRICS. IN ADDITION, WE ALSO ADD THE POLY-SiGe TFTs WITH Al_2O_3 AS GATE DIELECTRICS FOR COMPARISON

Gate dielectric	$LaAlO_3$ 50 nm (8.7 nm EOT)	LPCVD SiO_2 80 nm [4]	PECVD TEOS oxide 60 nm [5]	PECVD TEOS oxide 40 nm [6]	Al_2O_3 50 nm [14]
V_{th} (V)	1.2	5.6	8.14	Not extracted	3
μ_{FE} (cm^2/Vs)	40	20	12.44	3	47
Sub-threshold slope (V/decade)	0.31	1.4	1.97	2.67	0.44
I_{on}/I_{off}	1.5×10^6	3.5×10^5	2.97×10^5	Not extracted	3×10^5
Breakdown field (MV/cm)	6.3	Not extracted	Not extracted	5.4	Not extracted

design provides an alternative way to create high drive current, along with existing approaches such as excimer-laser crystallization (ELC) [3], [7]–[9], metal-induced lateral crystallization [15] and electric field-enhanced crystallization [16]. Good uniformity is also obtained due to the furnace crystallization [4], in contrast with the narrow process window and poor uniformity in ELC TFTs [17].

The I_d–V_g characteristics of a representative TFT are shown in Fig. 2. The $V_{\rm th}$ is 1.2 V with a subthreshold slope of 0.31 V/dec. This low subthreshold swing indicates a low interface trap density [2], [3], and is consistent with the good electron field-effect mobility of 40-cm^2/Vs. This is because the sputtering and subsequent 400 °C oxidation also oxidized the poly-Si surface. Although this is the undesired feature in high-κ CMOS to lower down the EOT [10]–[13], the slight oxidation of poly-Si can give a good high-κ/poly-Si interface and hence improve the mobility and subthreshold swing. The $I_{\rm on}/I_{\rm off}$ ratio of the high-κ $LaAlO_3$ TFT is 1.5×10^6, even without performing hydrogen passivation.

The field dependence of the gate current density (Fig. 3) shows a gate dielectric breakdown voltage of 31–32 V. This corresponds to an electric field of 6.2–6.4 MV/cm that is slightly larger than PECVD TEOS oxide of 5.4 MV/cm [6]. This is high enough to drive a liquid crystal display. This high breakdown field is comparable with or better than that for PECVD TEOS oxide [2]–[5]. This is important for achieving good dielectric reliability [10]–[13]. It may arise from the plasma-free process used, which does not damage the gate dielectric.

Fig. 4 shows the charge-trapping characteristics of the $LaAlO_3$ TFTs under constant-current stress from 0.1 to 10 mA/cm^2 (or ~2.9 to 5.8 MV/cm electric field). The gate voltage shift is only 0.28 V even under 10 mA/cm^2 stress, which is much better than the 2.2 V shift in TEOS oxide TFTs under the same stress condition [18]. Such low charge-trapping indicates the good quality of the gate dielectric and is consistent with high-κ $LaAlO_3$ CMOSFETs also fabricated at low temperature [10], [11]. Hence integrating high-κ gate dielectrics into TFT should not degrade the TFT device reliability, often dominated by the grain-boundary related hot-carrier degradation [19].

The important device parameters are summarized in Table I, where the data from devices using LPCVD SiO_2, PECVD TEOS oxides [4]–[6] and Al_2O_3 gate dielectric (with poly-SiGe) [14] are also shown for comparison. The better device performance of the $LaAlO_3$ TFTs, compared with LPCVD, PECVD TEOS oxide TFTs (using the same

furnace-crystallization process) and relative low κ Al_2O_3 devices, are the lower $V_{\rm th}$ due to the higher capacitance density ($V_{\rm th} = \phi_{\rm ms} + Q_{\rm total}/C_{\rm dielectric}$), the higher transistor current drive, and the plasma-free process.

IV. Conclusion

We have fabricated and characterized high-performance LTPS TFTs that incorporate high-κ $LaAlO_3$ as the dielectric—this provides good dielectric properties such as a high breakdown field, low leakage current and low charge trapping rate. These devices exhibit excellent electrical characteristics and high current drive, even without hydrogenation passivation or excimer laser crystallization process steps.

References

[1] T. Nishibe, "Low-temperature poly-Si TFT by excimer laser annealing," in *Proc. Mater. Res. Soc. Symp.*, vol. 685E, 2001, pp. D6.1.1–D6.1.5.

[2] C. A. Dimitriadis, P. Coxon, L. Dozsa, L. Papaddimitrious, and N. Economou, "Performance of thin film transistors on polysilicon films grown by LPCVD at various conditions," *IEEE Trans. Electron Devices*, vol. 39, no. 3, pp. 598–606, Mar. 1992.

[3] C. H. Tseng, T. K. Chang, F. T. Chu, J. M. Shieh, B. T. Dai, H. C. Cheng, and A. Chin, "Investigation of inductively coupled plasma gate oxide on low temperature polycrystalline-silicon thin film transistors," *IEEE Electron Device Lett.*, no. 6, pp. 333–335, Jun. 2002.

[4] Y. W. Choi, J. N. Lee, T. W. Jang, and B. T. Ahn, "Thin-film transistors fabricated with poly-Si films crystallized at low temperature by microwave annealing," *IEEE Electron Device Lett.*, vol. 20, no. 1, pp. 2–4, Jan. 1999.

[5] C. W. Lin, M. Z. Yang, C. C. Yeh, L. J. Cheng, T. Y. Huang, H. C. Cheng, H. C. Lin, T. S. Chao, and C. Y. Chang, "Effects of plasma treatments, substrate types, and crystallization methods on performance and reliability of low temperature polysilicon TFTs," in *IEDM Tech. Dig.*, 1999, pp. 305–308.

[6] K. M. Chang, W. C. Yang, and C. P. Tsai, "Electrical characteristics of low temperature polysilicon TFT with a novel TEOS/oxynitride stack gate dielectric," *IEEE Electron Device Lett.*, vol. 24, no. 8, pp. 512–514, Aug. 2003.

[7] G. K. Guist and T. W. Sigmon, "High-performance thin-film transistors fabricated using excimer laser processing and grain engineering," *IEEE Trans. Electron Devices*, vol. 45, no. 4, pp. 925–932, Apr. 1998.

[8] J.-H. Jeon, M.-C. Lee, K.-C. Park, S.-H. Jung, and M.-K. Han, "A new poly-Si TFT with selectively doped channel fabricated by novel excimer laser annealing," in *IEDM Tech. Dig.*, 2000, pp. 213–216.

[9] C. H. Tseng, C. W. Lin, T. K. Chang, H. C. Cheng, and A. Chin, "Effects of excimer laser dopant activation on the low temperature polysilicon thin-film transistors with lightly doped drains," *Electrochem. Solid-State Lett.*, vol. 4, pp. G94–G97, Nov. 2001.

[10] D. S. Yu, A. Chin, C. C. Laio, C. F. Lee, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, "3D GOI CMOSFETs with novel IrO_2(Hf) dual gates and high-κ dielectric on 1P6M-0.18 μm-CMOS," in *IEDM Tech. Dig.*, 2004, pp. 181–184.

[11] D. S. Yu, K. C. Chiang, C. F. Cheng, A. Chin, C. Zhu, M. F. Li, and D.-L. Kwong, "Fully silicided NiSi:Hf/$LaAlO_3$/smart-cut-Ge-on-insulator n-MOSFETs with high electron mobility," *IEEE Electron Device Lett.*, vol. 25, no. 8, pp. 559–561, Aug. 2004.

[12] C. H. Huang, M. Y. Yang, A. Chin, W. J. Chen, C. X. Zhu, B. J. Cho, M.-F. Li, and D. L. Kwong, "Very low defects and high performance Ge-on-insulator p-MOSFETs with Al_2O_3 gate dielectrics," in *Symp. VLSI Tech. Dig.*, 2003, pp. 119–120.

[13] A. Chin, Y. H. Wu, S. B. Chen, C. C. Liao, and W. J. Chen, "High quality La_2O_3 and Al_2O_3 gate dielectrics with equivalent oxide thickness 5–10 Å," in *Symp. VLSI Tech. Dig.*, 2000, pp. 16–17.

[14] Z. Jin, H. S. Kwok, and M. Wong, "High-performance polycrystalline SiGe thin-film transistors using Al_2O_3 gate insulators," *IEEE Electron Device Lett.*, vol. 19, no. 12, pp. 502–504, Dec. 1998.

[15] S.-W. Lee and S.-K. Joo, "Low temperature poly-Si thin-film transistor fabrication by metal-induced lateral crystallization," *IEEE Electron Device Lett.*, vol. 17, no. 4, pp. 160–162, Apr. 1996.

[16] B. Kim, H.-Y. Kim, H.-S. Seo, S. K. Kim, and C. D. Kim, "Surface treatment effect on the poly-Si TFTs fabricated by electric field enhanced crystallization of Ni/a-Si:H films," *IEEE Electron Device Lett.*, vol. 24, no. 12, pp. 733–735, Dec. 2003.

[17] C. W. Lin, L. J. Cheng, Y. L. Lu, Y. S. Lee, and H. C. Cheng, "High-performance low-temperature poly-Si TFTs crystallized by excimer laser irradiation with recessed-channel structure," *IEEE Electron Device Lett.*, vol. 22, no. 6, pp. 269–272, Jun. 2003.

[18] K. M. Chang, W. C. Yang, and B. F. Hung, "High-performance RSD poly-Si TFTs with a new ONO gate dielectric," *IEEE Trans. Electron Devices*, vol. 51, no. 6, pp. 995–1001, Jun. 2003.

[19] T. Yoshida, K. Yoshino, M. Takei, A. Hara, N. Sasaki, and T. Tsuchiya, "Experimental evidence of grain-boundary related hot-carrier degradation mechanism in low-temperature poly-Si thin-film-transistors," in *IEDM Tech. Dig.*, 2003, pp. 219–222.