Hot-Carrier Effects in P-Channel Modified Schottky-Barrier FinFETs

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***Abstract*—High-performance p-channel modified Schottky-barrier SOI FinFETs (MSB pFinFETs) with low temperature source/drain annealing process was recently suggested for future nano-scale devices. In this letter, the hot-carrier (HC) immunity of the MSB pFinFETs with different gate lengths (L_g) and fin widths (W_f) are presented. The experimental data shows that the MSB pFinFET with narrower W_f has less hot carrier degradation than that with wider W_f. The effects of electrical field in Si fins induced from lateral-gate electrode and the degree of uniformity of source/drain extension are illustrated cautiously by two-dimensional simulation and transmission electron microscopy (TEM) micrographs, respectively. It is found that the devices with narrower W_f have weaker electrical field from gate electrode and better uniformity of source/drain extension resulting in superior hot-carrier immunity. The projected operation voltage at ten years dc lifetime exceeds 1.6 V as the W_f is narrower than 60 nm. It is thus concluded that the MSB pFinFET would be a very promising nano device.**

***Index Terms*—FinFET, hot carrier, Schottky-barrier (SB), silicon-on-insulator (SOI).**

I. Introduction

A high-performance tri-gate modified Schottky-barrier (SB) p-channel FinFET (MSB pFinFET) with ultrashort source/drain extension (SDE) at the interface of silicide and inverted channel has been recommended recently to overcome the drawbacks of SB MOSFETs while preserving the advantages such as the low S/D external resistance and the low temperature process [1], [2]. When the devices are scaled down, MSB pFinFETs may also suffer from hot-carrier (HC) effects. For the prediction of the long-term reliability of the proposed tri-gate MSB pFinFETs; therefore, the HC reliabilities of the proposed devices are firstly investigated for various bias stress conditions and device dimensions. The superior HC reliability of the devices with narrower fins is confirmed. It is also pointed out that the proper balance and decrease of gate electric field in the narrow fin is the major reason of extraordinary hot carrier immunity in MSB pFinFET. On the other hand, as the gate length (L_g) decreases, the quite exceedingly uniform of the SDE region in the narrow Fins is also regarded as the possible dominative mechanism of excellent HC reliability of MSB pFinFETs.

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II. Experiments

Detail fabrication processes for the MSB pFinFETs used in this letter have already been reported elsewhere [2]. The fully depleted devices were fabricated on SIMOX substrate with 150-nm-thick buried oxide (BOX), 40-nm-thick Si active layers ($T_{\rm Si}$), 4-nm-thick thermally grown gate oxide, and 50-nm composite SiO_2/Si_3N_4 spacer. After NiSi was formed at the S/D contact, the SDE in the devices between silicide and channel was formed by implant-to-silicide process (ITS) and furnace annealing at 600 °C for 30 min [3].

To investigate the HCE of the proposed MSB pFinFETs, the worst-case bias condition for HC stress was determined first. The degradations of device parameters including threshold voltage ($V_{\rm th}$), transconductance (G_m), and drain current ($I_{\rm lin}$) were found to be higher when the gate voltage was set at $V_g = V_d$ in comparison with $V_g = 1/2V_d$. Therefore, all the stress experiments were performed at $V_g = V_d$ for a wide range of stress biases at 300 K. Degradation in device parameters under several $V_g = V_d$ stress conditions were then tracked over time for MSB pFinFETs with two different L_g and several fin widths (W_f). The degradations of the maximum transconductance and drain current were measured in the linear region ($V_g = 1$ V and $V_d = 50$ mV). The electric field distribution in Si fins was simulated for MSB pFinFETs with various $W_f/T_{\rm Si}$ ratios [4]. The roughness of the silicide front with $W_f = 40$ nm and 200 nm were examined by planar view transmission electron microscopy (TEM) micrographs.

III. Results and Discussions

The degradations of G_m and $I_{\rm lin}$ for the MSB pFinFETs with $L_g = 49$ nm and different W_f stressed at $V_g = V_d = -2.3$ V were shown in Fig. 1, respectively. Perhaps due to the sharp Si fin corner and mechanical stress induced by S/D silicide; the hot-carrier integrity (HCI) of MSB pFinFETs is slightly worse than that of conventional fully depleted SOI devices. Hole trapping at the interface of SiO_2/Si were still observed to dominate the HC degradation, similar to the conventional bulk and fully depleted SOI pMOSFETs [5]–[7]. We also discovered that the degradation of MSB pFinFETs with wider W_f is more serious than that of devices with narrower W_f. The HC lifetimes of the devices with different L_g (49 and 130 nm) and various W_f were plotted against the reciprocal of the stress voltage in the inset of Fig. 2. The lifetime is defined as the stress time to reach 10% degradation in G_m because the G_m is the most degradable parameters among $I_{\rm lin}$, $V_{\rm th}$, and G_m. As shown in the inset of Fig. 2, MSB pFinFETs with both $L_g = 49$ nm and 130 nm meet the 10-yr lifetime requirement under normal operating condition at $V_d = 1$ V.

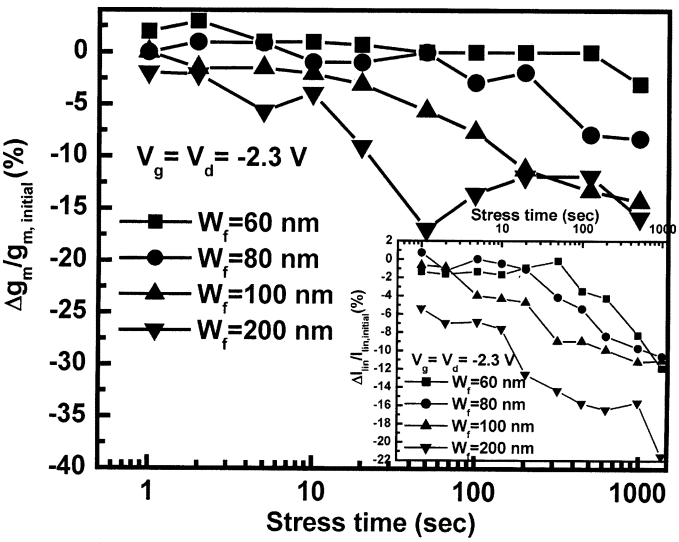

Fig. 1. Degradation of the maximum transconductance (G_m) and the drain current ($I_{\rm lin}$) versus stress time for MSB pFinFETs with $L_g = 49$ nm and different W_f.

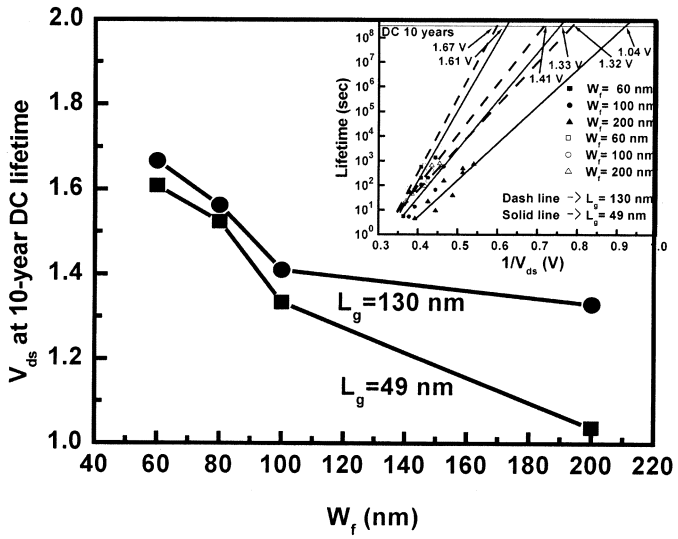

Fig. 2. Projected operation voltages to twn-year lifetime of the MSB pFinFETs with different L_g and W_f. The inset figure shows dc hot-carrier lifetime of the MSB pFinFETs with $L_g = 49$ and 130 nm and various W_f versus the reciprocal of the drain voltage. The failure criterion is 10% degradation in G_m.

The extrapolated operation voltages to a ten-year lifetime of devices with two different L_g as a function of W_f were displayed in Fig. 2. It is surprising that when the W_f decreases from 200 to 60 nm, the allowable operation voltage of the device with $L_g = 130$ nm increases steeply from 1.33 to 1.67 V. For the devices with $L_g = 49$ nm, the allowable voltage increases from 1.04 Vto 1.61 V. In order to explain the HC degradation dependence on W_f, the cross-sectional electrical field simulations of Si fins with different ratio of $W_f/T_{\rm Si}$ were performed. The potential distribution in Si fin of the proposed device biased at $V_g = -2.3$ V with $W_f = 200$ nm and 40 nm were shown in Fig. 3(a) and (b). Obviously, as the fin becomes wider, almost the energetic hot carriers are accelerated toward the top gate oxide as shown in Fig. 3(a). Nevertheless, in the narrow fin, the lateral gate voltages relax the electric field apparently due to the different direction of electric fields induced by the top gate and the two lateral gates, as shown in Fig. 3(b). With this result,

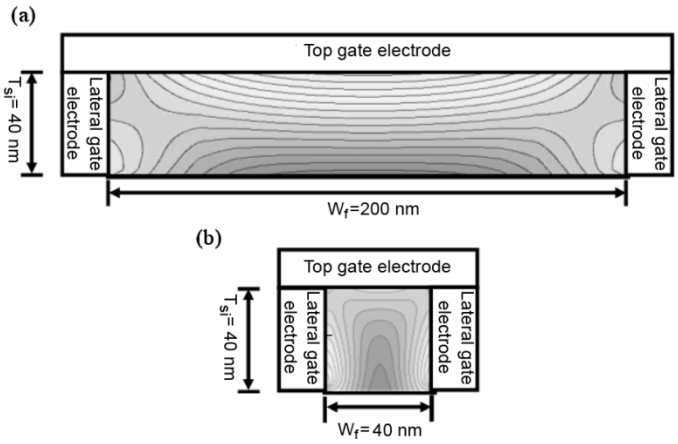

Fig. 3. Cross-sectional potential distribution in Si fins of the MSB pFinFETs with (a) $W_f/T_{\rm Si} = 200$ nm/40 nm and (b) $W_f/T_{\rm Si} = 40/40$ nm. The gate voltage is -2 V.

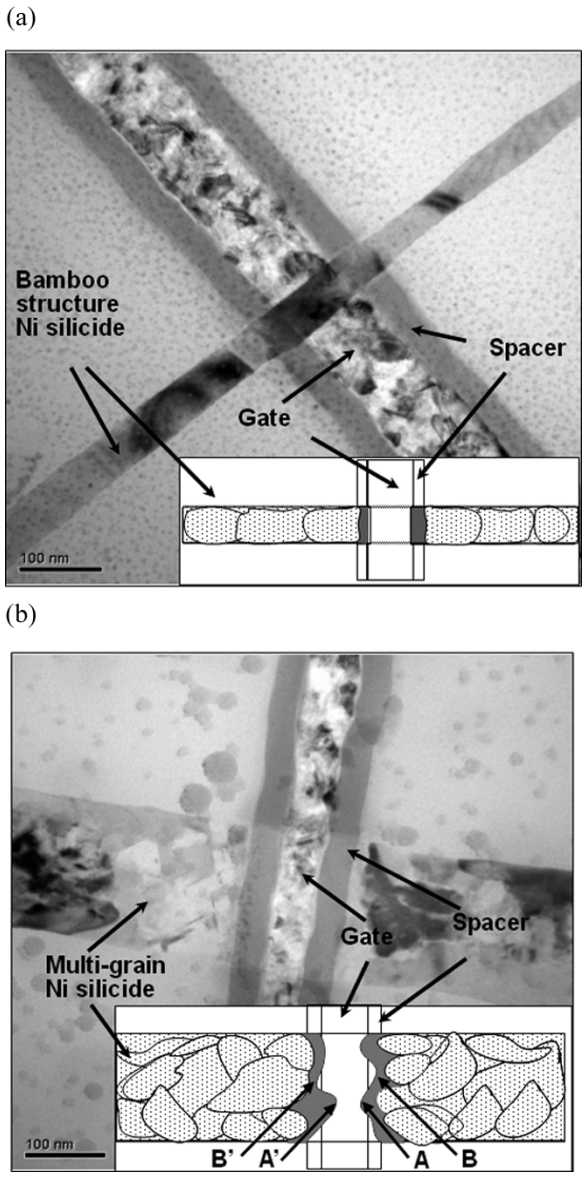

Fig. 4. Plane view TEM and schematic images of the MSB pFinFETs with (a) narrow ($W_f = 40$ nm) and (b) wide ($W_f = 200$ nm) fins.

the electric field and then the HC degradation of narrower fin is distinctly smaller than that of wide ones.

Another important observation from Fig. 2 is the allowable operation voltage decrease apparently with the decrease of L_g when the W_f increases from 100 to 200 nm. In order to explain the different HC degradation rates of the devices with different L_g, it is postulated that the roughness of SDE may affect the HCI. The TEM micrographs and schematic images of the MSB pFinFETs with W_f of 40 and 200 nm are shown in Fig. 4. Whenever the W_f becomes wider, not only the microstructure of the silicided fin changes from bamboo structure to multigrain structure, but also the silicide/Si interface becomes rougher. Therefore, the uniformity of channel length of the wider devices degrades more than that of the narrower ones. For example, as the wide W_f device shown in the inset of Fig. 4, because the channel length along A-A$'$ is shorter than that along B-B$'$, the lateral electric field at A is higher than that at B, and then the HCI of wide device becomes poor.

IV. Conclusion

In this letter, we first demonstrated that the MSB pFinFETs with low temperature process also have strong resistance against HC degradation. The mechanisms of HC degradation of the devices with different geometries are demonstrated. The electric field in fins induced by the top and the two lateral gates dominate the HCI of the MSB pFinFETs. As the fin width decreases, the net electric field in fin is balanced off by the lateral gates, and therefore, predominately reduces the HC degradation of the devices. Moreover, the roughness of SDE regions also affects the HCI, especially for devices with wide W_f and short L_g. As the result, in the devices with $L_g = 49$ nm, the uniform SDE diffused from the bamboo-like silicide fin relieves the HC degradation in the narrow fin devices. To conclude, it is thus expected that the ultranarrow W_f MSB pFinFETs with strong resistance against HC degradation would be a very promising nano device at sub-45-nm technology nodes.

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