The Effect of IrO_2–IrO_2– Hf–$LaAlO_3$ Gate Dielectric on the Bias-Temperature Instability of 3-D GOI CMOSFETs

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***Abstract*—We have studied the bias-temperature instability of three-dimensional self-aligned metal-gate/high-κ/Germanium-on-insulator (GOI) CMOSFETs, which were integrated on underlying 0.18 μm CMOSFETs. The devices used IrO_2–IrO_2–Hf dual gates and a high-κ $LaAlO_3$ gate dielectric, and gave an equivalent-oxide thickness (EOT) of 1.4 nm. The metal-gate/high-κ/GOI p-and n-MOSFETs displayed threshold voltage (V_t) shifts of 30 and 21 mV after 10 MV/cm, 85 °C stress for 1 h, comparable with values for the control two-dimensional (2-D) metal-gate/high-κ–Si CMOSFETs. An extrapolated maximum voltage of −1.2 and 1.4 V for a ten-year lifetime was obtained from the bias-temperature stress measurements on the GOI CMOSFETs.**

***Index Terms*—Bias-temperature instability (BTI), Germanium-on-insulator (GOI), high κ, $LaAlO_3$, metal gate, three-dimensional (3-D).**

I. Introduction

FOR the downscaling of MOS devices to continue, high-κ gate dielectrics [1]–[11] are required to reduce the gate-leakage current and the dc power consumption. Unlike SiO_2, high-κ gate dielectrics exhibit significant charge trapping, causing the threshold voltage (V_t) to shift under applied voltage and raised temperature conditions. Such bias-temperature instability (BTI) [1], [6], [7] of V_t with time creates a severe reliability concern for ICs, where the use of high-κ gate dielectrics is more problematic than oxynitrides in devices [12], [13]. In addition to the charge trapping, the poor BTI in high-κ CMOSFETs may be related to impurity diffusion from the gate [5], and from the use of processing water and/or hydrogen annealing after device fabrication [12], [13]. In this paper we report the BTI of three-dimensional (3-D) self-aligned metal-gate/high-κ/Germanium-on-insulator (GOI) CMOSFETs and compare the results with those from control Si devices. The GOI devices were fabricated above the interconnects of a 1-Poly-6-Metal (1P6M) process and the underlying 0.18 μm CMOSFETs [14]. The effects of 3-D device integration are similar to a scaling of the devices, but are not as challenging or as costly. It also helps reduce the ac power consumption in the backend interconnects [14]. Our 3-D IrO_2–IrO_2–Hf dual-gated high-κ $LaAlO_3$–GOI CMOSFETs [2], [14] showed results which are comparable or better than devices using lower κ HfAlON [5] and HfSiON [6] dielectrics, where the BTI is improved by trading off the κ value of HfO_2.

Manuscript received January 3, 2005; revised February 28, 2005. This work was supported in part by the National Science Council of Taiwan, R.O.C., under the NRC-NSC joint project under Grant NSC93-2215-E-009-001. The review of this letter was arranged by Editor A. Wang.

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Digital Object Identifier 10.1109/LED.2005.848130

II. Experimental Details

The GOI on 1P6M 0.18 μm Si MOSFETs were formed by depositing PECVD oxide on a processed Si wafer and on a Ge wafer, O_2-plasma enhanced bonding at 400 °C, and thinning down using a "smart-cut" process [1], [5]. The "smart cut" of the SiO_2–Ge was done using a 200 keV H^+ implant which, after heating the bonded structure, permitted a separation/break at the peak of the implant damage concentration, by using mechanical stress. (This method is widely used in SOI manufacturing.) After forming the 1.6 μm thick (110) n- or (100) p-GOI, the active device region was defined using thick field oxide and patterning. The $LaAlO_3$ gate dielectric was deposited by PVD from a $LaAlO_3$ source $(\kappa = 25.1)$ followed by a 400 °C oxidation step [2]–[4], [14]. Then a 150-nm IrO_2 or 150-nm IrO_2/15–nm Hf gate was deposited on the $LaAlO_3$ by PVD, for the p-or n-MOSFETs respectively. The Hf shows a low work function for n-MOSFETs, similar to that for fully silicided NiSi:Hf–Al_2 O_3 devices [2]. The $IrO_2/LaAlO_3$ p-MOSFETs or IrO_2/ $HfLaAlO_3$ n-MOSFETs were created using self-aligned 25-keV boron or 35-keV phosphorus implantation, and followed by a 500 °C RTA. For comparison, self-aligned 2-D [IrO_2–IrO_2/Hf]–$LaAlO_3$ CMOSFETs were fabricated using the same process, but with a higher RTA temperature of 950 °C. These are treated as our control devices.

III. Results and Discussion

Fig. 1(a)–(c) show the I_d–V_d and I_d–V_g characteristics for the 3-D GOI and the control 2-D Si p-and n-MOSFETs. The 3-D metal-gate/high-κ CMOS transistors show good device characteristics such as ~4 orders lower gate leakage current than SiO_2 dielectric devices, at 1.4-nm EOT (measured from C–V) [14]. They also have 2.2–2.4 times higher drain drive current than the Si control devices. However, the drain-source leakage current of $\sim 5 \times 10^{-10}$ A/μm is inferior to that of standard Si devices. Further improvements are required to create ultrathin body GOI

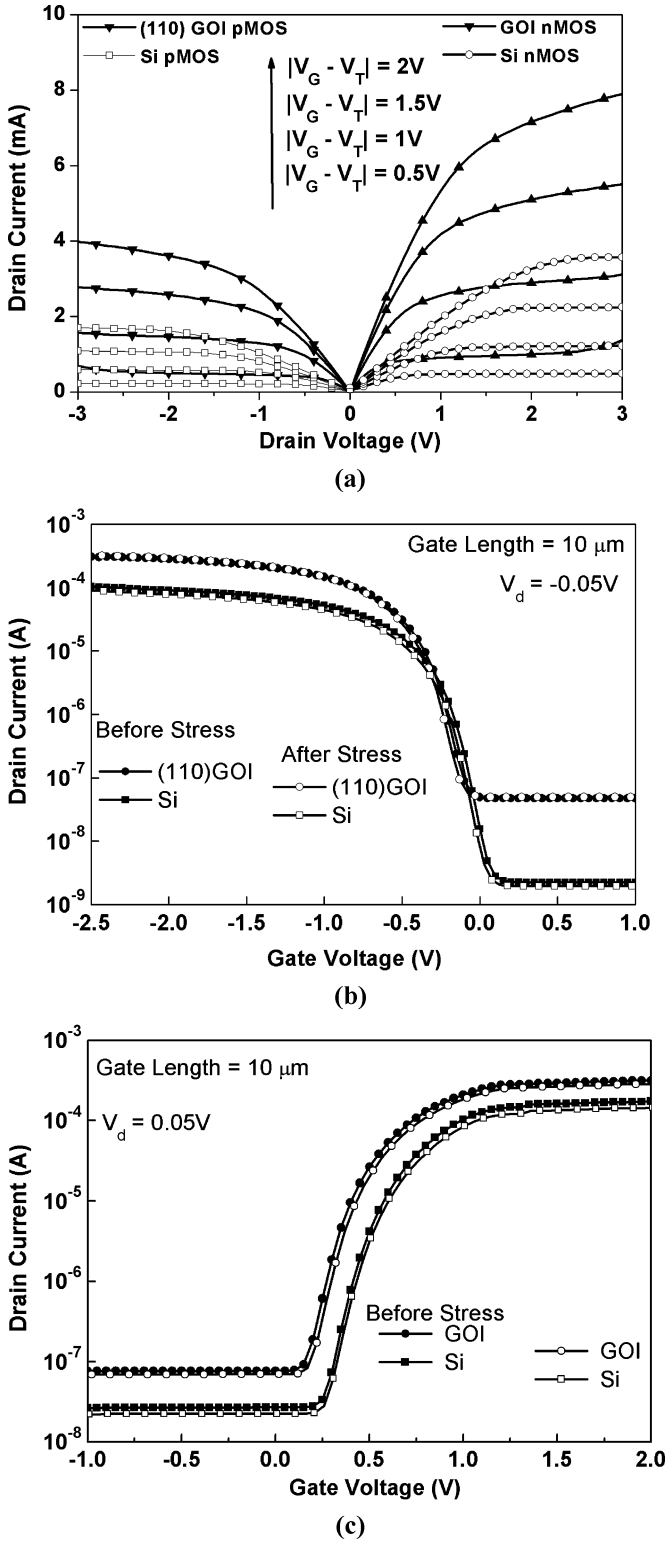

Fig. 1. (a) I_d–V_d characteristics of [IrO_2–IrO_2/Hf]/$LaAlO_3$ CMOSFETs, (b) I_d–V_g for IrO_2/$LaAlO_3$ p-MOSFETs and (c) I_d–V_g for IrO_2/Hf/$LaAlO_3$ n-MOSFETs on 3-D GOI and control Si devices. The stress conditions were 10 MV/cm at 85 °C for 1 h.

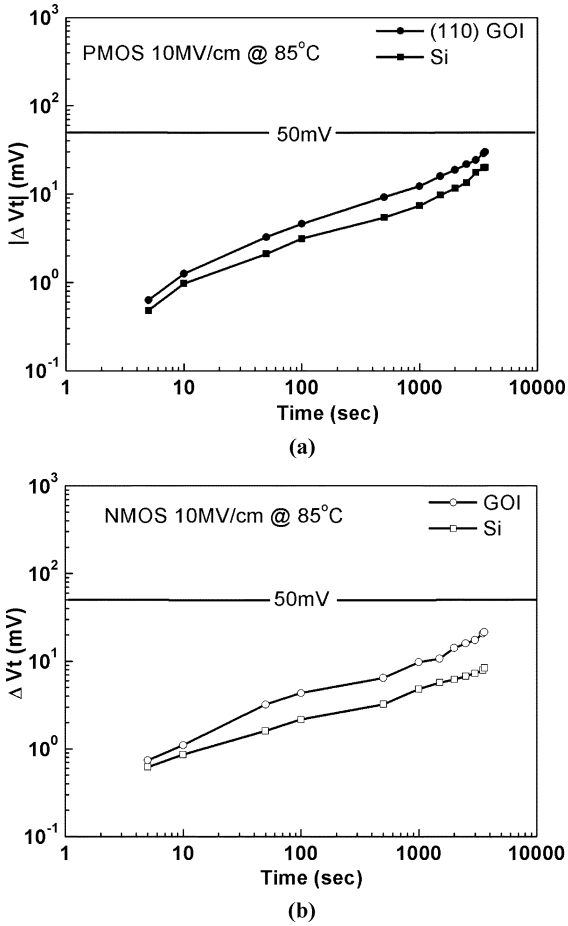

Fig. 2. Threshold voltage shifts (ΔV_t) as a function of time for (a) IrO_2–$LaAlO_3$ p-MOSFETs and (b) IrO_2–Hf–$LaAlO_3$ n-MOSFETs on 3-D GOI, compared with the control 2-D Si devices. The stress conditions were 10 MV/cm at 85 °C for 1 h.

by thinning down the top Ge. This is feasible and should be successful since recent ultrathin body $Si_{1-x}Ge_xOI$ ($x = 0.96$ and close to GOI) pMOS showed a small I_{ds} of 10^{-12} A and >7 orders of magnitude I_{on}/I_{off} [15]. However even the current 3-D device technology should be useful for special multifunctional ICs, such as those used for integrated opto-electric applications [16]. The I_d–V_g after 10 MV/cm, 85 °C stress for 1 h are also displayed for the BTI study. Both negative BTI (NBTI) in p-MOS and positive BTI (PBTI) in n-MOS related V_t shifts were measured, suggestingthat charge traps are generated in the $LaAlO_3$ gate dielectric.

In Fig. 2(a) and (b), we show the ΔV_t with BT stress time at 10 MV/cm and 85 °C for the 3-D GOI and control 2-D Si p- and n-MOSFETs, respectively. After 1 h of BT stress, the ΔV_t of 3-D metal-gate/high-κ/GOI CMOSFETs was −30 and 21 mV for the p- and n-MOSFETs, respectively, which is slightly larger than the control 2-D Si CMOSFETs. These results are comparable with TaN– HfAlO [5] and poly-Si–HfSiON [6] devices, suggesting that the major BTI issue is related to the metal-gate/high-κ dielectric rather than the low-temperature processed 3-D GOI. The observed BTI is much better than that for TiN-HfO_2 devices [6], indicating that the strong bonding of AlO in $LaAlO_3$ most probably plays a key role in the BTI improvement. This is also consistent with the better BTI for TaN–HfAlO devices compared with those using TiN–HfO_2 [5]. In this case the improvements were at the expense of a lower κ for HfAlO compared with HfO_2.

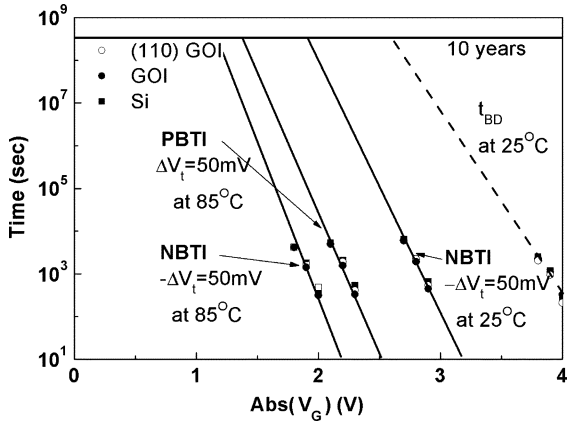

Fig. 3. Extrapolated maximum operation voltage for a ten-year BTI lifetime, under the failure conditions of a 50-mV change in V_t at 85 °C. The $t_{\rm BD}$ is included for comparison.

The IrO_2-metal gate is a diffusion barrier, which is consistent with the observed high electron and hole mobilities of 203 and 67 $\rm cm^2/Vs$ in control metal-gate/high-κ 2-D Si CMOSFETs [14]. Thus the BTI degradation is unlikely due to metallic diffusion into the high-κ gate dielectric [5]. Hence the possible BTI mechanism may be due to the higher interface traps and oxide charges in the high-κ $LaAlO_3$ [1], [5], [6].

We measured the BTI at other gate electric fields to estimate the ten-year lifetime. Fig. 3 shows the lifetime ($|\Delta V_t| = 50$ mV) as a function of $|V_{gs}|$ for various metal-gate/high-κ MOSFETs, BT stressed at 85 °C. The extrapolated $V_{\rm max-10\ years}$ values are -1.2 and 1.4 V for p- and n-MOSFETs, respectively. These values can meet the BTI reliability requirements at 1 V operation, with a 20% safety margin. Note that the $V_{\rm max-10\ years}$ value from the time-to-breakdown $(t_{\rm BD})$ is much higher than that from BTI measurements, and is an overestimate of the reliability of the high-κ CMOSFETs. The high $V_{\rm max-10\ years}$ for BTI in these metal-gate/high-κ 3-D GOI and control 2-D CMOSFETs is related the absence of impurities in gate [5], the presence of a good IrO_2 diffusion barrier [14], and the avoidance of hydrogen annealing or process water [12], [13] in the device fabrication.

IV. Conclusion

We have studied the NBTI and PBTI of 1.4 nm EOT [IrO_2–IrO_2– Hf]–$LaAlO_3$ 3-D GOI CMOSFETs. Good NBTI and PBTI performance was shown by the relatively small $|\Delta V_t|$ of -30 and 21 mV, and the high extrapolated $V_{\rm max-10\ years}$ value of -1.2 V under 10 MV/cm, 85 °C stress.

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