A Novel Process-Compatible Fluorination Technique With Electrical Characteristic Improvements of Poly-Si TFTs

Shen-De Wang, *Student Member, IEEE*, Wei-Hsiang Lo, Tzu-Yun Chang, and Tan-Fu Lei

***Abstract*—A process-compatible fluorine passivation technique of poly-Si thin-film transistors (TFTs) was demonstrated by employing a novel CF_4 plasma treatment. Introducing fluorine atoms into poly-Si films can effectively passivate the trap states near the SiO_2/poly-Si interface. With fluorine incorporation, the electrical characteristics of poly-Si TFTs can be significantly improved including a steeper subthreshold slope, smaller threshold voltage, lower leakage current, higher field-effect mobility, and better On/Off current ratio. Furthermore, the CF_4 plasma treatment also improves the reliability of poly-Si TFTs with respect to hot-carrier stress, which is due to the formation of strong Si–F bonds.**

***Index Terms*—CF_4 plasma, fluorine, fluorine passivation, poly-Si, process-compatible, reliability, TFTs.**

I. Introduction

POLYSILICON THIN-FILM transistors (poly-Si TFTs) have attracted much attention due to the possibility of realizing the integration of driving circuits and pixel elements on one glass substrate, and the potential to accomplish the system-on-panel (SOP) [1]. High-performance poly-Si TFTs are required for this goal. A hydrogenation process has been utilized to reduce the trap states of poly-Si films to improve the device performance [2]. However, hydrogenated poly-Si TFTs suffer from a serious instability issue due to weak Si–H bonds, which will break easily under an electrical stress [3]. Using fluorine to passivate the trap states of poly-Si TFTs has been reported recently [4]–[6]. Strong Si–F bonds, more stable than Si–H bonds, can maintain the device performance under long-term electrical stress. Conventional fluorine ion implantation might be not suitable for large-sized glass substrate applications. Moreover, a subsequent high temperature annealing is required to activate the fluorine atoms and recover the defects created by ion implantation. However, high-temperature process is not compatible with current production due to the low-melting point of low-cost glass substrate. Kim *et al.* demonstrated the use of fluorinated oxide (SiO_xF_y) to serve as a diffusion source [7], [8]. However, an extra film deposition and etching are required. To date, although hydrogen-based plasma treatments have been widely investigated in poly-Si TFTs, there is still a lack of an investigation of the fluorine-based plasma treatment.

In this letter, a novel fluorination technique is proposed by employing a low-temperature CF_4 plasma treatment. This technique provides a simple, effective and process-compatible method to introduce fluorine atoms into poly-Si films and high-performance and high-reliability poly-Si TFTs were fabricated.

II. Experimental

The schematic diagram of fabrication processes is illustrated in Fig. 1. First, a 100-nm-thick amorphous silicon layer was deposited on a thermally oxidized Si wafer by dissociation of SiH_4 gas in a low-pressure chemical vapor deposition (LPCVD) system at 550 °C. Next, a semi-Gaussian-shaped KrF excimer laser ($\lambda = 248$ nm) at an energy density of 420 mJ/cm^2 was performed for the phase transformation from amorphous to polycrystalline silicon. The average grain size of the poly-Si measured using scanning electron microcscopy (SEM) is approximately 300 nm, as shown in Fig. 1(b). Individual active regions were then patterned and defined. After the clean process, the samples were subjected to the CF_4 plasma treatment, conducted in a plasma-enhanced chemical vapor deposition (PECVD) system at 350 °C for 15 s, under a pressure of 200 mtorr and a power of 10 W, followed by a deposition of 100-nm-thick TEOS oxide by PECVD at 350 °C. Then, a 200-nm-thick poly-Si was deposited by LPCVD at 620 °C to serve as the gate electrode. A self-aligned phosphorous ion implantation was preformed at the dosage and energy of 5×10^{15} cm^{-2} and 40 keV, respectively. The dopant activation was performed by excimer laser annealing (ELA), followed by a deposition of passivation layer and the definition of contact holes. Finally, a 500-nm-thick Al electrode was deposited and patterned. For comparison, the control TFTs were prepared without the CF_4 plasma treatment process. No hydrogenation and thermal annealing process were performed after the Al formation.

III. Results and Discussion

There was no significant surface contamination on the poly-Si samples after chemical cleaning detected using total reflection X-ray fluorescence (TRXRF). Also, the variation of the thickness of the poly-Si films before and after CF_4 plasma treatment measured using ellipsometer was within 5%. Therefore, the surface cleaning effect and the thinning effect of the

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The authors are with the Department of Electronics Engineering and Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, R. O. C.

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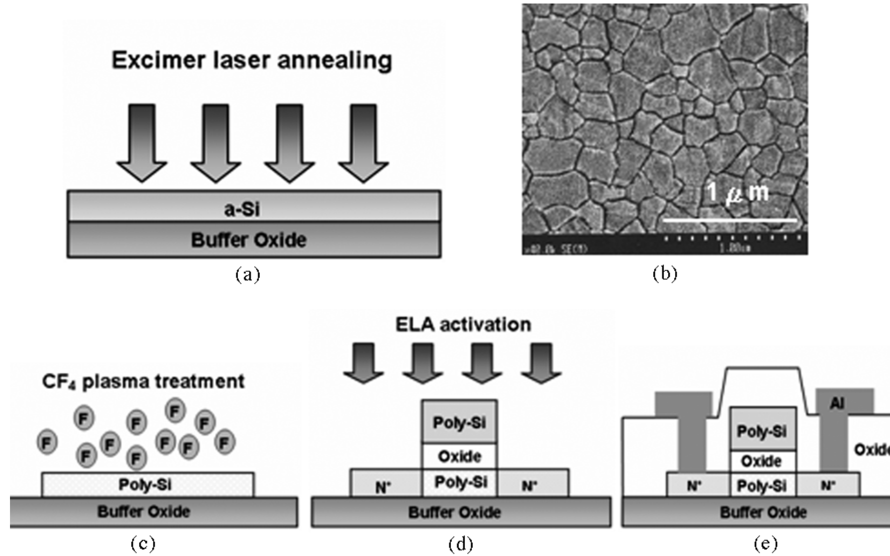

Fig. 1. Schematic diagram of the fabrication process of poly-Si TFT with CF_4 plasma treatment. (a) Depositing amorphous silicon and ELA processing. (b) SEM image of ELA-processed poly-Si film after secco-etch. (c) Defining active region and CF_4 plasma treatment. (d) S/D implantation and dopand activation by ELA. (e) Depositing passivation oxide, opening contact holes, depositing metal, and patterning metal.

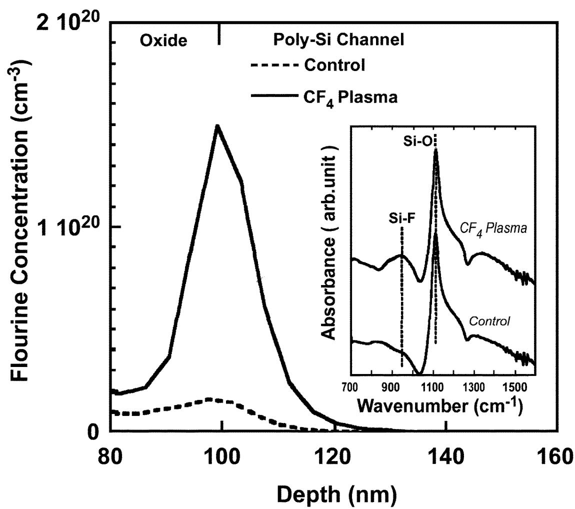

Fig. 2. SIMS profiles of conventional and CF_4 plasma-treated poly-Si films. Inset shows the FTIR spectra of the control and the CF_4 plasma-treated poly-Si films.

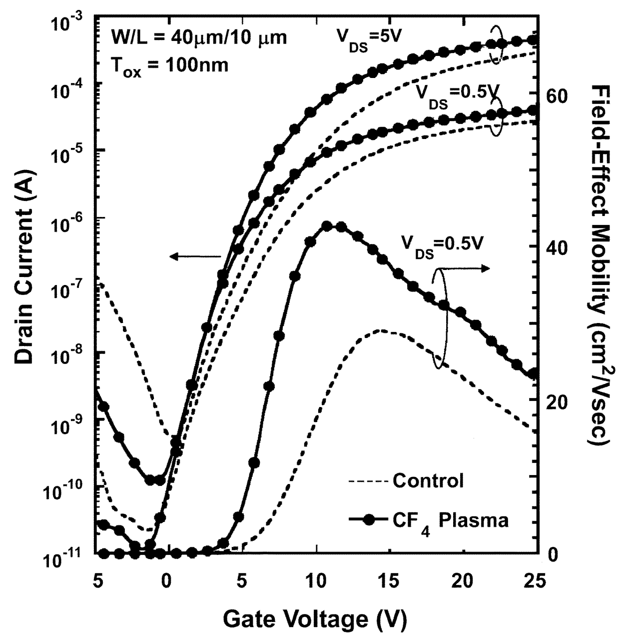

Fig. 3. Transfer characteristics and field-effect mobility versus gate voltage for the control and the CF_4 plasma-treated poly-Si TFTs with $V_{\rm DS} = 0.5$ and 5 V.

CF_4 plasma treated poly-Si films were excluded in this experiment. Fig. 2 shows the SIMS profiles of the control and CF_4 plasma-treated poly-Si films. Fluorine atoms are introduced into the SiO_2/poly-Si interface by the CF_4 plasma treatment. These piled-up fluorine atoms can provide an effective trap states termination, because the channel is formed near the interface. The inset shows the Fourier transform infrared spectroscopy (FTIR) spectra of the control and CF_4 plasma-treated poly-Si samples. The spectra exhibit absorption peaks corresponding to Si-F bonds centered at round 940 cm^{-1} [9], [10]. The strong peak of Si–O bond is related to the SiO_2 substrate. Therefore, Si–F bonds were formed in the poly-Si by employing the CF_4 plasma treatment.

Fig. 3 shows the transfer characteristics and field-effect mobility versus the gate voltage for the devices. The measurements were performed at $V_{\rm DS} = 0.5$ and 5 V. The threshold voltage $(V_{\rm th})$ was defined as the gate voltage required to achieve a normalized drain current of $I_D = (W/L) \times 100$ nA at $V_{\rm DS} = 5$ V. Accordingly, the $V_{\rm th}$ and the subthreshold slope (SS) of the CF_4 plasma-treated TFT are 4.35 V and 1.28 V/dec., respectively, which are superior to 5.75 V and 1.92 V/dec. of the control TFT. Notably, the leakage current of the CF_4 plasma treated TFT is more than one order in magnitude lower than that of the control TFT, especially under a large negative gate bias. The corresponding *On/Off* current ratios for the CF_4 plasma-treated poly-Si TFT and the control TFT are 4.03×10^6 and 0.52×10^6 at $V_{\rm DS} = 5$V, respectively. The *On/Off* current ratio of the CF_4 plasma-treated TFT is approximately eight times larger than that

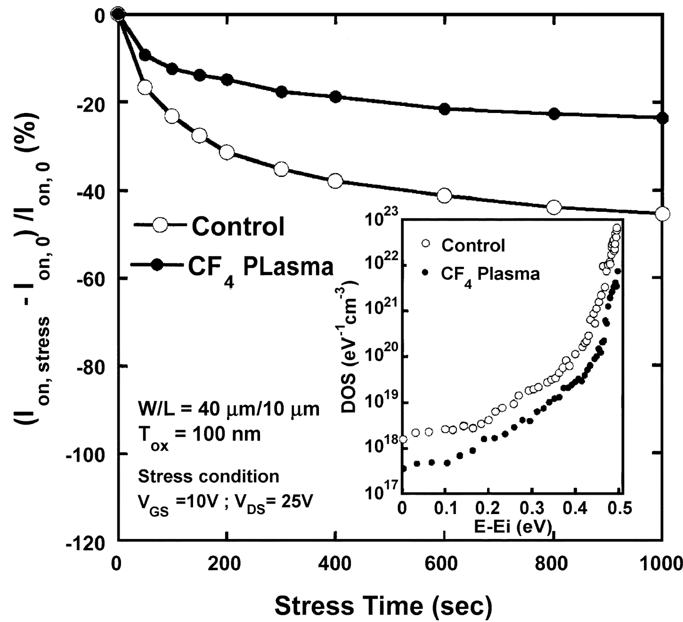

Fig. 4. On-current variations as a function of stress time under a hot carrier stress for the control and the CF_4 plasma-treated poly-Si TFTs. Inset shows the density of states (DOS) in the energy bandgap of the control and the CF_4 plasma-treated TFTs.

of the control TFT. Additionally, the CF_4 plasma-treated TFT has an about 50% enhancement in the maximum field-effect mobility. Note that great improvements on device characteristics were obtained even though the conditions of ELA were not optimized, which resulted in the rather poor field-effect mobility compared with other reports.

In order to verify the passivation effect of the CF_4 plasma treatment, the effective trap states densities (N_t) near the SiO_2/poly-Si interface were calculated form the SS. By neglecting the depletion capacitance, the N can be expressed as [11]

$$N_t = \left[\left(\frac{SS}{\ln 10}\right)\left(\frac{q}{kT}\right) - 1\right]\left(\frac{C_{ox}}{q}\right) \quad (1)$$

where the C_{ox} is the capacitance of the gate oxide. The N_t of the control TFT and the CF_4 plasma treated TFT are 6.72×10^{12} cm^{-2} and 4.42×10^{12} cm^{-2}, respectively. The N_t values reflect both interface sates and grain boundary trap states near the SiO_2/poly-Si interface. Therefore, those states near the SiO_2/poly-Si interface can be effectively terminated using CF_4 plasma treatment. Combined with the SIMS profiles, we believe that the passivation effect is due to the piled-up fluorine atoms.

As shown in the inset of Fig. 4, the density of states (DOS) in the energy bandgap of the TFTs were calculated using field-effect conductance method [12]. Both deep states and tail states are significantly reduced using the CF_4 plasma treatment. We deduce that for the control TFT, there exists lots of dangling bonds and strain bonds near the SiO_2/poly-Si interface, resulting in high deep states and tail states [13]. On the contrary, for the CF_4 plasma treated TFT, fluorine atoms were introduced into the SiO_2/poly-Si network to terminate the dangling bonds, release the strain bonds and form the S–F bonds, improving the device characteristics [5].

Additionally, hot carrier stress was carried out at $V_{DS} = 25$ V and $V_{GS} = 10$ V for 1000 s to examine the device reliability. Fig. 4 shows the variations of the On-current (I_{on}) under hot carrier stress. The I_{on} degradation rate of the control is almost twice that of the CF_4 plasma treated TFT. It is attributed to the strong Si–F bonds formed at the SiO_2/poly-Si interface. The Si–F bonds are hard to be broken under hot carrier stress, leading to a great improvement in the device reliability.

IV. Conclusion

Significant improvements on the device performance, including threshold voltage, subthreshold slope, leakage current, field-effect mobility, and On/Off current ratio have been demonstrated. This is due to the reduction of the interface states and grain boundary trap states near the SiO_2/poly-Si interface. The CF_4 plasma treatment also improves the hot-carrier immunity due to the formation of Si-F bonds. It is concluded that the CF_4 plasma treatment is a simple, effective and process-compatible method to fabricate high-performance and high-reliability poly-Si TFTs.

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