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Characterization of CF_4-plasma fluorinated HfO_2 gate dielectrics with TaN metal gate

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In this paper, fluorine incorporation into the HfO_2 gate dielectrics by post CF_4 plasma treatment was proposed to improve the electrical characterization. TaN–HfO_2–*p*-Si capacitors were demonstrated in this work. The characteristics of fluorinated HfO_2 gate dielectrics were improved, including the capacitance-voltage hysteresis and current-voltage behaviors. This may be attributed to the fluorine incorporated into the HfO_2 gate dielectrics as revealed by secondary ion mass spectroscopy. Moreover, the formation of Hf-F bonding was observed through electron spectroscopy for chemical analysis spectra. © *2005 American Institute of Physics*. [DOI: 10.1063/1.1944230]

An equivalent oxide thickness of less than 1.0 nm will be needed for sub-65 nm MOSFETs (Metal-Oxide-Semiconductor-Field-Effect-Transistors) as illustrated in the International Technology Roadmap for Semiconductors.[1] Silicon oxide gate dielectric is now being pushed to both its technological and theoretical limits. The equivalent oxide thickness (EOT) in the 4-Gbit generation dynamic random access memory (DRAM) will be scaled down further to 0.22 nm which is very close to the structural limit of silicon dioxide, as the Si–O bond in silicon oxide is 0.17 nm. The high tunneling leakage current is not acceptable for the scaling of SiO_2 below the thickness of 1.0 nm. Numerous attempts in the search for alternate gate dielectrics have been carried out by using hafnium dioxide to replace SiO_2 as the gate dielectric due to its high dielectric constant (25–30), wide energy bandgap (~5.68 eV), and high stability with the Si surface.[2–4] Unfortunately, for high-*k* gate dielectrics, there is a hysteresis phenomenon in its capacitance-voltage (*C*-*V*) characteristics.[5,6] This hysteresis induces a flatband voltage shift, and threshold voltage instability when it is applied to MOSFETs. Therefore, some methods, such as co-sputtering of silicon, and aluminum with hafnium to deposit hafnium silicate and aluminate dielectrics,[7,8] the use of nitric gas for chemical vapor deposition (CVD)[9] or oxidizing sputtered metal nitride like HfN[10] to form hafnium oxynitride (HfON) films, and post-deposition NH_3 plasma treatment methodology[11] were used to improve the hysteresis phenomenon and thermal stability. In this work, we propose a CF_4 plasma treatment methodology to investigate its effects on HfO_2 gate dielectrics. Leakage current and hysteresis phenomenon were much improved for the HfO_2 gate dielectrics treated by CF_4 plasma. The results show that fluorine atoms were accumulate into the HfO_2 dielectrics to form Hf–F bonding by CF_4 plasma, resulting in the reduction of gate leakage current, charge trapping, and the hysteresis.

Metal–insulator–semiconductor (MIS) capacitors were fabricated. The starting material for MIS capacitor fabrication is ⟨100⟩ *p*-type Si substrate with a resistivity in the range of 10–15 Ω cm. Following the standard cleaning process, an HfO_2 layer of about 10 nm thick was deposited by reactive sputtering of hafnium metal in oxygen and argon ambient. This thickness is too thick to use as an application of the high-*k* dielectric in future Si technology. The purpose of using a thicker film at the present stage is for the ease of studying both the physical properties of bulk and interface using secondary ion mass spectroscopy (SIMS), and electron spectroscopy for chemical analysis (ESCA). Compared to the control sample (without CF_4 plasma, denoted as W/O), after the gate dielectric deposition, some samples were processed by CF_4 plasma at 50 W for 1 and 5 min, denoted as P-1 and P-5, respectively. In order to know the thermal stability for the MIS capacitors, post deposition annealing (PDA) under the rapid thermal system for 1 min in an N_2 ambient at 700 °C was demonstrated for W/O, P-1, and P-5 samples, denoted as W/O/A, P-1/A, and P-5/A, respectively. TaN film of 50 nm was deposited by reactive RF sputter. Thereafter, a 300 nm thick Al film was deposited on the TaN film by thermal evaporator. The gate of the capacitor was defined lithographically and then etched. Finally, a 300 nm thick Al film was deposited on the backside of the wafer to form the ohmic contact. The high frequency (100 kHz) capacitance-voltage (*C*-*V*) characteristics and current-voltage (*J*-*V*) curves were measured by HP4284 and Keithly 4200, respectively, and the effective oxide thickness (EOT) was extracted from the high frequency capacitance under the accumulation region without considering the quantum effect. In addition, the fluorine concentration was analyzed by SIMS. The Hf–O

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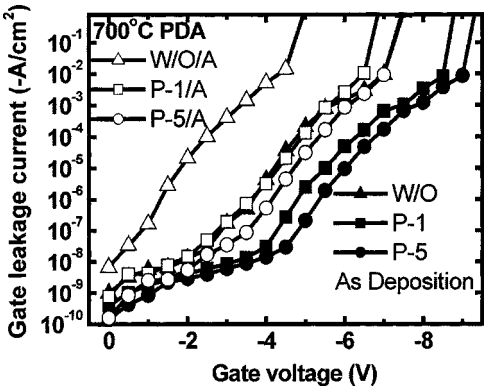

FIG. 1. The *J-V* curves (gate leakage current) for all samples. The gate leakage current was decreased for the sample with CF_4 plasma treatment. The same tendency was evident for the samples with post deposition annealing.

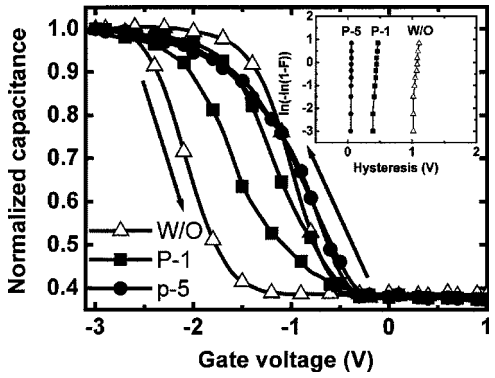

FIG. 2. The normalized *C-V* hysteresis curves for all samples without PDA. The inset figure is the Weibull distribution for *C-V* hysteresis. The hysteresis was improved for the sample with CF_4 plasma treatment.

and Hf–F bondings were analyzed by ESCA.

The CF_4 plasma and PDA effects on the current voltage characteristics are shown in Fig. 1. For the CF_4 plasma effects, the gate leakage current of the CF_4 plasma treated samples (P-1 and P-5) was much smaller than that of the W/O (without plasma) sample. The gate leakage current was decreased with the increase in CF_4 plasma treatment. The gate leakage current of the HfO_2 gate dielectrics after 700 °C PDA, was increased due to the crystallization after thermal annealing for HfO_2 gate dielectrics, and the resulting grain boundaries are thought to act as significant leakage pathways. Possible crystallization of HfO_2 can occur, and when it does it results in an increase in the leakage current for all samples, whether treated by CF_4 plasma or not. Compared to the as-deposited sample without post-CF_4 plasma treatment (solid triangle markers in Fig. 1, the leakage current at a gate voltage of 2 volts increases three orders after PDA (open triangle markers). However, for the as-deposited samples with post-CF_4 plasma (solid square and circle markers in Fig. 1, the leakage current at gate voltage of 2 volts increased slightly after PDA (open square and circle markers). This was due to the fact that the fluorine incorporation retarded the crystallisation of HfO_2 gate dielectrics, and improved the thermal stability of the HfO_2 thin film. In addition, the breakdown voltage was also improved for CF_4 plasma treated samples (P-1 and P-5). This means that fluorine incorporation into the HfO_2 gate dielectrics to strengthens the HfO_2 thin film. The normalized *C-V* hysteresis curves are shown in Fig. 2 for all samples without PDA. According to the inner-interface trapping model,[12] majority carriers would trap at the inner-interface of the HfO_2 thin film. This phenomenon makes the *C-V* curve shift during the capacitance-voltage measurement. After CF_4 plasma treatment, the fluorine atoms were incorporated into the interfacial layer (HfO_2–Si interface) resulting in less charge trapping. The *C-V* hysteresis was improved with an increasing CF_4 plasma treatment time. As is evident, the HfO_2 thin films with CF_4 plasma treatment at 5 min (P-5) showed the smallest *C-V* hysteresis, of only 10 mV. The inset of Fig. 2 was the Weibull distribution for the magnitude of *C-V* hysteresis for all samples without PDA. The samples with CF_4 plasma treatment showed less *C-V* hysteresis, especially for the samples with long CF_4 plasma treatment time (sample, P-5).

A typical fluorine profile measured by secondary ion mass spectroscopy (SIMS) proves that the fluorine atoms were incorporated into the HfO_2 thin films after post- CF_4 plasma treatment, as shown in Fig. 3. The amount of the fluorine atoms increased with the increase in CF_4 plasma treatment time. In addition, the fluorine atoms showed two peaks in the SIMS analysis, indicating that fluorine atoms almost entirely distributed in the surface of the Si substrate and the interface between the TaN gate and the HfO_2 thin film. This phenomenon shows that after post-CF_4 plasma treatment, the fluorine atoms would first accumulate at the surface of the HfO_2 thin film and then diffused through the HfO_2 thin film to terminate the dangling bond and accumulate at the interfacial layer between the HfO_2 thin film and the Si substrate as illustrated in Fig. 3. However, we still can find some fluorine atoms accumulated in the HfO_2 thin film, thus we can conclude that the fluorine will distribute in all the HfO_2 gate dielectrics after CF_4 plasma treatment. Figure 4 shows the Hf 4*f* ESCA spectra of the as-deposited and P-5 samples (CF_4 plasma treated at 5 min), respectively. A take-off angle (TOA) of 90° was used to measure the ESCA spectra. In Fig. 4(a), two distinct peaks of the Hf–O bonding at 18.7 and 20.3 eV are evident from the as-deposited sample. The intensity of the Hf 4*f* of HfO_2 dielectrics with CF_4 plasma treatment was very high and the original peak value at 20.3 eV was blurry as we can see in Fig. 4(b). This phenomenon means that there was another Hf bonding formation. Therefore, comparing the Hf–O bonds in Hf 4*f* spectra of HfO_2 gate dielectrics in Fig. 4(a) to those of the HfO_2 dielectrics with CF_4 plasma treatment in Fig. 4(b) reveals the Hf–F bonding, indicating fluorine incorporation after post-

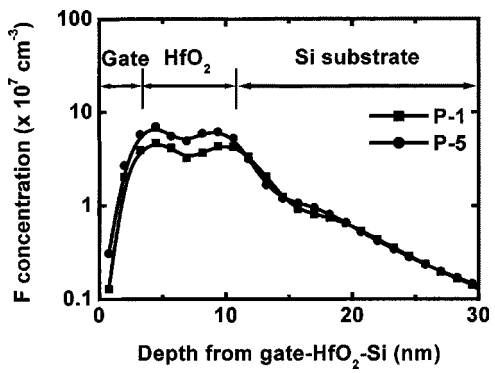

FIG. 3. The SIMS depth profile of fluorine atoms for all samples. The fluorine atoms distributed in HfO_2 gate dielectrics and show two peaks in the interface between TaN–HfO_2 and HfO_2–Si.

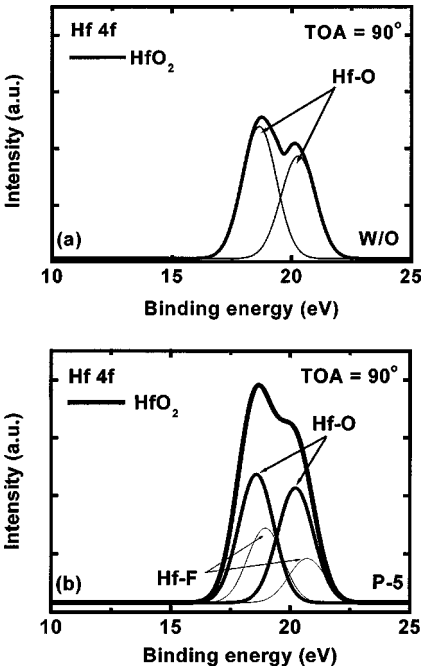

FIG. 4. Hf 4*f* ESCA spectra of (a) as-deposited sample, and (b) CF_4 plasma treated 5 min sample, respectively. A take-off angle (TOA) of 90° was used to measure the ESCA spectra.

CF_4 plasma treatment, as evident from the SIMS profiles in Fig. 3.

An approach to improve the dielectric properties of the HfO_2 films by using post-CF_4 plasma treatment was proposed. The incorporation of fluorine atoms into the HfO_2 gate dielectrics improved the characteristics including gate leakage current, breakdown voltage and *C-V* hysteresis. After the incorporation of fluorine atoms, the Hf–F bonding formation led to the reduction of charge trapping. The post-CF_4 plasma treatment technology used in high-*k* gate dielectrics is a manufacturing approach for future ULSI application.

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