Low-power low-voltage reference using peaking current mirror circuit

M.-H. Cheng and Z.-W. Wu

A low-power low-voltage bandgap reference using the peaking current mirror circuit with MOSFETs operated in the subthreshold region is presented. A demonstrative chip was fabricated in 0.35 µm CMOS technology, achieving the minimum supply voltage 1.4 V, the reference voltage around 580 mV, the temperature coefficient 62 ppm/°C, the supplied current 2.3 µA, and the power supply noise rejection ratio of −84 dB at 1 kHz.

Introduction: Since the bandgap reference was proposed in [1], many bandgap reference circuits have been designed to decrease the temperature sensitivity, the power dissipation, and the supply voltage [2–4]. Recently, particular research on generating a low-power and low-voltage reference was based on exploiting the properties of devices operated in the subthreshold region [5]. To obtain a low-power consumption, the operated current should be modest. The peaking circuit [2, 6, 7], with the MOSFETs operated in the weak-inversion region, has been recognised as a useful low-current reference. This Letter exploits the peaking circuit to realise a low-power low-voltage reference source. The proposed reference circuit merely consists of a self-biased peaking current source with a series resistor; thus it is easy to design, simple to realise and can meet the low-power, low-voltage requirement.

Circuit configuration: The proposed reference circuit is depicted in Fig. 1. The elements M_3, M_4 and R_1 constitute the peaking current source, while the elements M_1 and M_2, connected in a current mirror, serve for realising the function of self-biasing. The MOSFETs M_3, M_4 are designed to operate in the subthreshold region such that the required low supply voltage, low power consumption, and low reference voltage output can be achieved. The M_1, M_2 mirror is designed to make the drain currents of M_3 and M_4 operate in the peaking relation, then the voltage across R_1 is proportional to the absolute temperature (PTAT). Hence, the resistor ratio R_2/R_1 can be used to compensate for the variation of the gate-source voltage of M_3 with respect to the temperature. A steady reference voltage output, V_{out}, is therefore obtained.

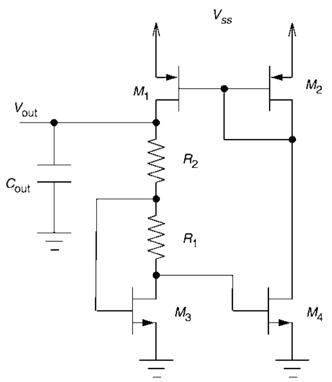

Fig. 1 *Schematic diagram of reference voltage*

Circuit analysis: For an n-MOSFET of aspect ratio W/L operated in the subthreshold region, its drain current is given by [2],

$$I_D = \frac{W}{L} qXD_n n_{p0} \exp\left(\frac{V_{GS}/N + C}{V_T}\right) \times \left[1 - \exp\left(-\frac{V_{DS}}{V_T}\right)\right] \qquad (1)$$

where X denotes the thickness of the depletion layer, D_n the electron diffusion constant, n_{p0} the electron density in the p-type silicon, $V_T = \kappa T/q$ the thermal voltage, and N, C are constants. Denote $K_i = (W/L)_i$, $I_0 = qXD_n n_{p0}$ exp(C/V_T), the drain currents of M_3, M_4 can be expressed as

$$I_{D3} = K_3 I_0 \exp\left(\frac{V_{GS3}}{NV_T}\right), \quad I_{D4} = K_4 I_0 \exp\left(\frac{V_{GS4}}{NV_T}\right) \qquad (2)$$

Note that the factor exp$(-V_{DS}/V_T)$ is neglected because in the circuit the operated drain-source voltage of each MOSFET is much greater than $3V_T$. The relation between two currents, therefore, is

$$I_{D4} = I_{D3} \frac{K_4}{K_3} \exp\left(\frac{V_{GS4} - V_{GS3}}{NV_T}\right) \qquad (3)$$

The circuit configuration, as shown, constrains the difference between two gate-source voltages of M_3, M_4 in a relation given by

$$V_{GS4} - V_{GS3} = -I_{D3} R_1 \qquad (4)$$

Substituting (4) into (3), we obtain

$$I_{D4} = I_{D3} \frac{K_4}{K_3} \exp\left(-\frac{I_{D3} R_1}{NV_T}\right) \qquad (5)$$

The peaking circuit is designed such that I_{D4} is at its peaking value. It can be achieved by zeroing the derivative of I_{D4} with respect to I_{D3} using (5), yielding the design condition to maintain the current peaking

$$I_{D3} R_1 = NV_T \qquad (6)$$

If the condition is satisfied, then the drain currents of M_3, M_4, via (5), are related by

$$I_{D4} = I_{D3} \frac{K_4}{K_3} e^{-1} \qquad (7)$$

Hence, the self-biasing mirror is designed to make I_{D3}, I_{D4} satisfy the relation in (7); consequently, the peaking condition (6) is maintained. For example, if $K_4/K_3 = e$, then setting $K_1 = K_2$ will make $I_{D3} = I_{D4}$ and the peaking condition is satisfied.

The voltage across R_1 under the peaking condition, as shown by (6), is therefore PTAT. Using this property, we obtain the reference voltage output V_{out} as follows

$$V_{out} = I_{D3} R_2 + V_{GS3} = \frac{R_2}{R_1} NV_T + V_{GS3} \qquad (8)$$

Note that the drain current of M_3 is also PTAT. It has been known [2] that for an n-MOSFET with a PTAT drain current, the voltage V_{GS3} with respect to the temperature can be expressed as

$$V_{GS3} = A_0 + A_1 T + A_2 T \ln T \qquad (9)$$

where the constants A_0, A_1 and A_2 are dependent on the process technology. Hence, the resistor ratio R_2/R_1 can be designed to make the temperature coefficient of V_{out} equal zero at a selected temperature T_0; i.e. which yields

$$\frac{R_2}{R_1} = -\frac{q}{\kappa N}(A_1 + A_2 + A_2 \ln T_0) \qquad (10)$$

Table 1: Element dimensions and values

Element	Value
M_1	4/16
M_2	4/16
M_3	32/16
M_4	79.04/16
R_1	50 kΩ
R_2	58 kΩ
C_{out}	4.5 pf

Design example: An example design has been implemented in standard 0.35 µm CMOS technology for verification. In this design, we let $I_{D4} = I_{D3}$ by setting the dimensions of M_1, M_2 identical to each other in the mirror circuit. Thus, using (7) we obtain $K_4/K_3 = e$, the ratio between the aspect ratio of M_3 and that of M_4 is determined. Since the process technology has the parameter N at about 2.06, we set $R_1 = 50$ kΩ such that the drain current of M_3 at room temperature, by (6), is approximately equal to 1 µA. We obtain the parameters A_0, A_1, A_2 using the curve-fitting technique via the least-squares method from the SPICE post-simulation data. Then, setting the nominal temperature $T_0 = 300$°K (27°C) and using (10), we have $R_2 = 58$ kΩ. The designed aspect ratios of MOSFETs and other element values are listed in Table 1. Note that small aspect ratios of M_1, M_2 are chosen to obtain a higher output impedance and yield a better performance of line regulation. The required area of the chip is about 0.126 mm^2.

The reference output voltages of six test chips have been measured with the supply voltages V_{ss} set at 1.4, 1.7, 2, 2.3, 2.6, 2.9, 3 or 3.3 V and temperatures at 0, 27, 43, 57 or 70°C. The measured reference output voltages against temperatures with V_{ss} of 1.4, 2, 3 V are shown in Fig. 2. In Fig. 3, the output voltages against supply voltages with the temperature at 0, 27, 57°C are depicted. The nominal specifications are listed in Table 2.

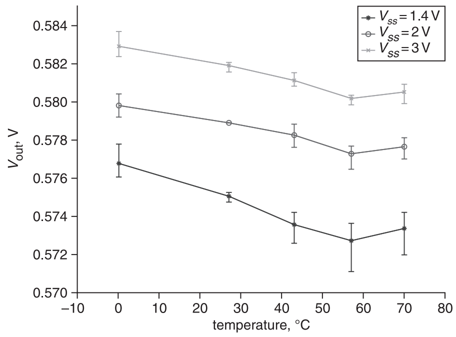

Fig. 2 *Reference voltage V_{out} against temperature T at various supply voltages*

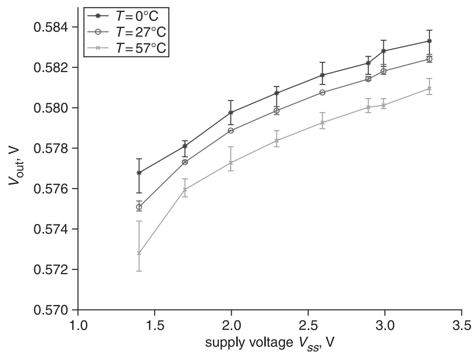

Fig. 3 *Reference voltage V_{out} against supplied voltage V_{ss} at various temperatures*

Table 2: Specifications

Specification	Value
Supplied current	2.3 µA at V_{ss} = 2 V
Minimum operating voltage	1.4 V
Output voltage	0.579 V at V_{ss} = 2 V
PSRR	−84 dB at 1 kHz
Line regulation	3.9 mV/V at 27°C
Temperature coefficient	62 ppm/°C at V_{ss} = 2 V

Conclusion: A low-power, low-voltage reference circuit using the peaking circuit with MOSFETs operated in the subthreshold region is reported. The reference output voltage is around 580 mV, the operated current 2.3 µA, and the minimum supply voltage 1.4 V. This circuit is easy to design, simple to realise, and suitable for use in low-power, low-voltage applications.

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