THE ANNEALING AND THE HYSTERISIS EFFECTS OF AU^+ IMPLANTED MOS STRUCTURES

L. I. Chen (陳 龍 英)

(Received 17 Feb. 1975)

Abstract

Firstly, this work provides a convenient method, with C-V, I-V and lifetime measurements as the analytic tools, to study the annealing and hysterisis effects in Au^+ implanted SiO_2 MOS structures. With 70 keV Au^+ implanted into 560Å thick SiO_2 layer, the optimum annealing condition is at 400°C, 15 to 30 minutes in dry nitrogen gas. With stress voltages range from +24 to −30 volts applied for 1 second, the flatband voltage shift is 14 volts which corresponds to an accumulated or stored charge of $-8\times10^{12}e$ cm^{-2} in the oxide layer. Thus the resulting MOS structure behaves similarly to a floating gate or multilayer device with obvious simplifications in the processing.

I. INTRODUCTION

It has been shown[1] that when gold ions are implanted into thermally oxidized silicon dioxide, the damage in the outer part of the insulator caused by the passage of the energetic ions will change the carrier transport mechanism in that region. The different transport mechanisms in the ion-implanted oxide together with the ion-induced trapping centers could give rise the charge storage in the oxide. In this work, we shall study the effects of annealing temperatures on that ion-implanted MOS characteristics. The charge storage and hysterisis effects of that MOS structure will also be studied.

The experimental devices were silicon MOS structures with a gold ion implanted SiO_2 layer. The silicon substrates were of 1 ohm-cm n-type, (111) oriented. For Au^+ ion in SiO_2 with 70 and 100 keV energies the projected range R_p are 320Å and 380Å and the projected straggling length $\triangle R_p$ are 70Å and 86Å respectively[2].

II. EFFECTS OF ANNEALING TEMPERATUPE ON DEVICE CHARACTERISTICS

In order to reduce the high Si-SiO_2 interface state density, the optimum annealing condition should achieve the following two requirements: (1) The SiO_2 interface state density after annealing should be as low as possible, and (2) The gold distribution in SiO_2 should not be affected appreciably after annealing. Unfortunately, the foregoing conditions are conflicting requirements. If one wants the interface state density to be low, the annealing temperature should be high; but at a high annealing temperature, the gold ion in SiO_2 would begin to diffuse and spread appreciably. Therefore, it is important to obtain an optimum annealing condition. As will be shown later the optimum condition is annealing at 400°C for 15 to 30 minutes in dry nitrogen.

The effects of Si-SiO_2 interface states on the interface properties can be studied by means of measuring the MOS capacitance-voltage (C-V) characteristics[3]. The effect of high Si-SiO_2 interface state density on the MOS capacitance characteristics makes the C-V curves highly distorted with much smaller slops as compared with the "control" sample. For the convenience of discussion, an "effective"flatband voltage shift $\triangle V_{FB}$ is defined as

$$\triangle V_{FB} = V_{imp.}\ (C_{FB}) - V_{cont.}\ (C_{FB})$$

where C_{FB} is the capacitance of the control at flat-band condition, $V_{cnot.}$ (C_{FB}) is the flat-band voltage of the control and the $V_{imp.}$ $(C_{FB.})$ is the

voltage of implanted sample when its capacitance is C_{FB}. The value of $\triangle V_{FB}$ as well as the shape of C-V curve serve as a measure of interface states and also of the effects associated with the ion implantation.

Fig. 1 shows the effects of isochronal annealing on the normalized effective flat-band voltage shift N, which is defined as

$$N(T) = \frac{\triangle V_{FB} \text{ (annealed at temperature } T)}{\triangle V_{FB} \text{(no annealing)}}$$

The annealing time interval is 5 minutes at each annealing temperature, and the data are taken with averaging over four samples which are implanted by 70 *keV* Au^+ to a dose of $10^{14}/cm^2$ with oxide thickness of 560 Å.

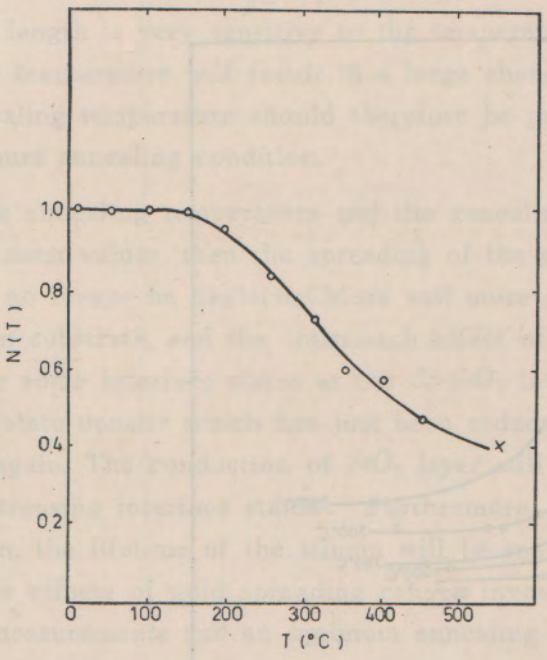

Fig 1

The normalized effective flat-band voltage shift vs. annealing temperature annealed for 5 minutes. The oxide layer, with a thickness of 560Å, is implanted by 70 keV gold ions to a dose of 10^{14} ions/cm^2.

As can be seen from Fig. 1, the value of $N(T)$ and thus the interface density begins to drop appreciable at an annealing temperature of 300°C. Because the annealing time interval is very short, saturation values of $N(T)$ at each temperature are not likely to be reached. Therefore, the values of $N(T)$ still decrease noticeably as the annealing temperatures go beyond 400°C.

It shows in Fig. 2 the isothermal annealing effects on the value of $N(T)$ of the same sample used in Fig. 1. At each temperature of annealing the minimum saturation value of $N(T)$ has been reached before increasing the annealing temperature to perform another isothermal annealing. At each annealing temperature, the value of $N(T)$ decreases toward its saturation value very rapidly at the first 30 minutes, then the rate of decrease of $N(T)$ starts to slow down. The inconsistency between the saturation $N(T)$ and the initial $N(T')$ value of the following annealing temperature is believed to be caused by the back annealing effect at room temperature for a long time. Again, we see that after the 400°C annealing for 30 minutes, most of the interface state density can be eliminated for the 70 *keV* implanted samples.

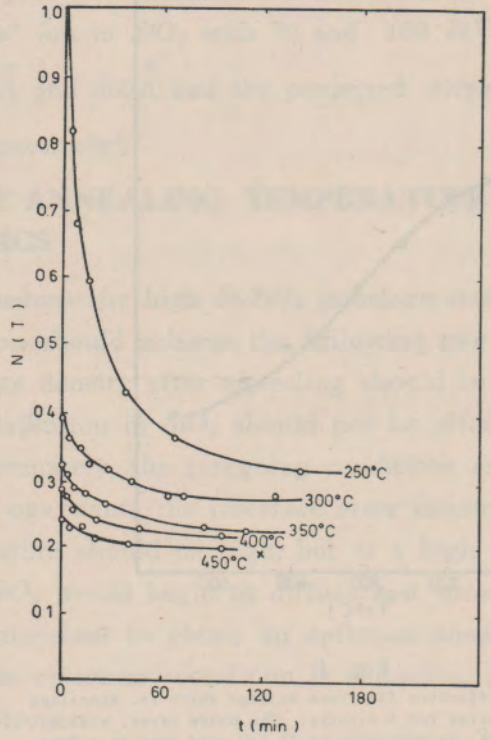

Fig 2

The normalized effective flat-band voltage shift vs. isothermal annealing time interval.

As mentioned before, the annealing temperature as well as the annealing time interval should bee high enough to reduce the interface state density appreciably, but not too high to cause significant spreading of gold ion distribution in SiO_2. It is believed that at high temperatures, atoms acquire some thermal energy to rearrange themselves to occupy suitable new positions. If there exists an atom concentration gradient, then diffusion of atoms occurs, and the concentration of diffusant n will satisfy the transport equation

$$\frac{\partial n}{\partial t}=D(T)\nabla^2 n=D(T)\frac{\partial^2 n}{\partial x^2}$$

In the foregoing equation, the diffusion coefficient $D(T)$ in a limited temperature range can be described by

$$D(T)=D_0 \exp(-E_a/kT)$$

where D_0 is the diffusion coefficient extrapolated to infinite temporature, E_a is the activation energy of diffusion, and k is the Boltzmann's constant.

From dimensional analyis, it is obvious that

$$x\propto\sqrt{D(T)\mathrm{t}}\ \propto e^{-C/T}t^{1/2}$$

where x is the diffusion length of the diffusant; t is the time interval of diffusion; and C is a constant equal to $E_a/2k$. One can see that the diffusion length is very sensitive to the temperature. A small change in annealing temperature will result in a large change of diffusion length. The annealing temperature should therefore be precisely determined to give the optimum annealing condition.

If the annealing temperature and the annealing time interval exceed their optimum values, then the spreading of the gold ion distribution in SiO_2 can no longer be neglected.More and more gold ion will diffuse into the silicon substrate, and the mismatch effect of foreign heavy gold atoms will cause some interface states at the Si-SiO_2 interface. Therefore, the interface state density which has just been reduced by annealing will increase again. The conduction of SiO_2 layer will also become larger due to the increasing interface states[4]. Furthermore, as gold atoms enter into the silicon, the lifetime of the silicon will be reduced. All these phenomena due to the effects of gold spreading can be investigated by C-V, I-V, and lifetime measurements and an optimum annealing condition can thus be determined.

The minority carrier lifetime in silicon of several samples have been measured. The precise value of lifetime is not important here, only the relative values of lifetime after each annealing treatment are interested. For the thin SiO_2 implanted samples the lifetime is very short (10^{-8} sec). This is believed to be due to the influence of high densities of traps and defects induced by the ion implantation damage near the Si-SiO_2 interface.

Fig. 3 shows the effects of isochronal annealing (for 5 minutes time interval) on the normalized lifetime $L(T)$ which is defined as

$$L(T)=\frac{\text{Lifetime } \tau' \text{ (annealed at temperature } T)}{\text{Lifetime } \tau \text{ (unannealed)}}$$

As can be seen in Fig. 3, the value of $L(T)$ begins to increase appreciably as the annealing temperatures exceed 200°C and up to 400°C; then $L(T)$

decreases appreciably as the annealing temperatures are higher than 400°C. This can be explained as following: For the annealing temperature between 200°C and 400°C, the Si-SiO_2 interface states and defects which are induced by gold ion implantation damage can be effectively reduced thus resulting an increasing minority carrier lifetime. As the annealing temperatures exceed 400°C, the gold atoms in SiO_2 begin to spread into the silicon substrate appreciably, the lifetime is therefore decreased due to the presence of appreciable quantity of gold atoms which serve as lifetime killer. This indicates that a temperature at about 400°C will be the optimum annealing temperature.

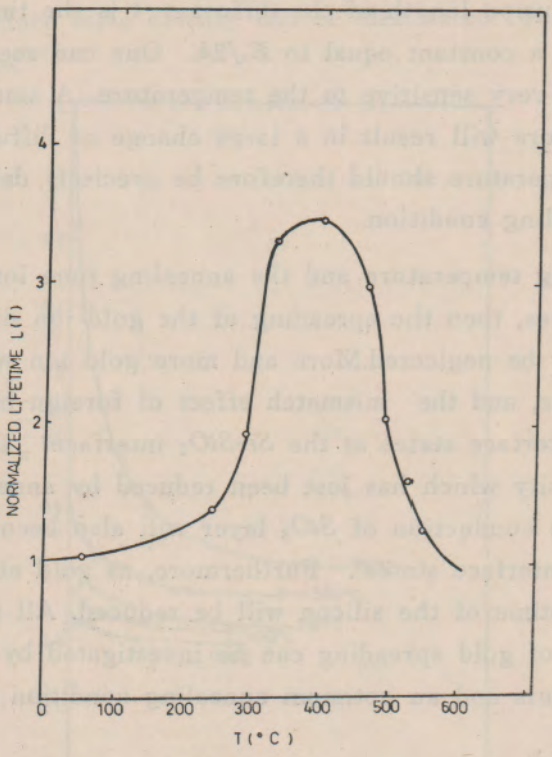

Fig 3

The normalized lifetime vs. annealing temperature annealed for 5 minutes.

Fig. 4 shows the isothermal annealing effect on the minority carrier lifetime of the same sample at two temperatures 400°C and 425°C respectively. The value of $L(T)$ increases to a maximum in about 15 minutes, remaining almost unchanged for about 30 minutes, then $L(T)$ decreases if the isothermal annealing continues to proceed. The increase of $L(T)$ is due to the annealing effect of reducing the interface states and defects in silicon induced by implantation damage; while the decrease of $L(T)$ indicates that the effect of distribution spreading becemes important as the annealing time intervals exceed 45 minutes.

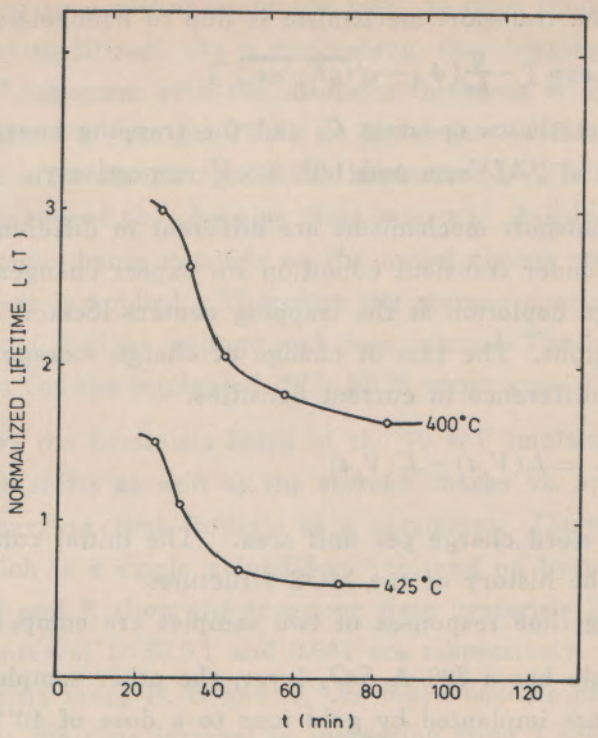

Fig 4

The minority carrier lifetime vs. annealing time interval at 400°C and 425°C respectively.

If we compare the two isothermal annealing curves of Fig. 4, we can find that for $T=425°C$ the value of $L(T)$ is smaller than unity, $L(T)<1$, for annealing time interval longer than about 35 minutes. This phenomenum indicates the highly sensitive dependence of annealing effects on temperatures, and that the effects of the gold spreading in SiO_2 is much more significant for the case $T=425°C$ compared with that of $T=400°$. Therefore, 425°C is too high to be used as the optimum annealing temperature. It is evident from Figs. 3 and 4 that the optimum annealing condition is at a temperature of 400°C for an interval from 15 to 30 minutes.

III. CHARGE STORAGE AND HYSTERISIS EFFECTS

It has been shown by the author[1] that the carrier transport mechanism of the implanted SiO_2 layer is converted from Fowler-Nordheim tunneling conduction to Frenkel-Poole bulk conduction. The current-voltage characteristics of the ion implanted sample are as follow: In inner region of the sample, the transport mechanism is due to the Folwer-Nordheim tunneling:

$$J_1 = C_o E^2 e^{-E_o/E_1}$$

where J_1 is the current density, E_1 is the electric field, and the constants were found[1] to be $C_o=10^{-11}\ A/V^2$ and $E_o=1.76\times10^8 V/cm$. In outer region

of the sample, the transport mechanism is due to Frenkel-poole emission:

$$J_2 = C_2 E_2 \exp\left[-\frac{q}{k_T}(\phi_2 - \sqrt{(qE_2/\pi\varepsilon_1)}\,)\right]$$

where the characteristics constant C_2 and the trapping energy level ϕ_2 were found[1] to be $4\times10^{-13} A/V$-cm and $1.2\pm0.2 eV$ respectively.

Since the transport mechanisms are different in different region ot the implanted SiO_2, under transient condition we expect changes in the charge storage or charge depletion at the trapping centers located at the boundary of these two regions. The rate of change of charge storage at the boundary is given by the difference in current densities:

$$\frac{dQ(V,t)}{dt} = J_2(V,t) - J_1(V,t)$$

where Q is the stord charge per unit area. The initial condition for Q is determined by the history of the MOS structure.

The charging time responses of two samples are compared in Fig. 5. One of the sample has a 720 Å SiO_2 layer, the other sample has a 560 Å SiO_2 layer, and are implanted by gold ions to a dose of 10^{14}cm^{-2} at 100 and 70 keV respectively. It is shown in the figure that for the thinner sample the charging time response becomes faster even at lower applied voltages. It is evident that the thickness of both regions of implanted SiO_2 has great effect on the transient behavior of Au^+ implanted SiO_2 structure.

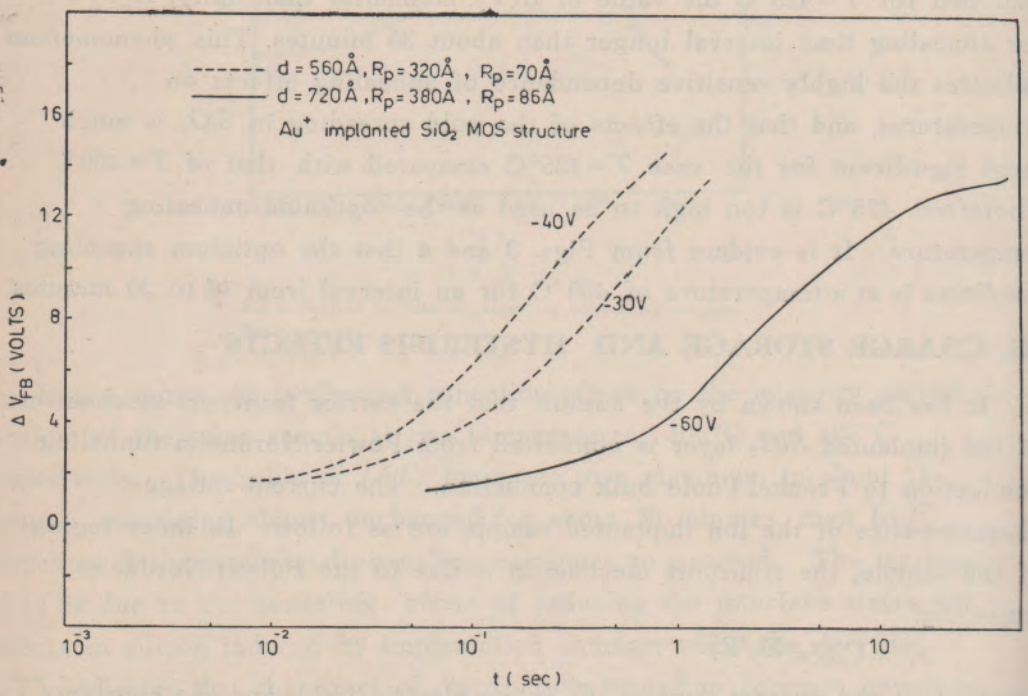

Fig. 5 The charging time responses of two samples of the implanted SiO_2 MOS Structures.

The charging time responses of the two samples used in Fig. 5 are between 10^{-1} sec to 10 sec. As a comparison, the charging time responses of the MNOS[5,6] structure with the insulator thickness at 1000 Å applied by 50 volts is from 10^3 sec (at 77°K) to 1 sec (at 300°K).

The change of storge charge in the implanted SiO_2 is a function of the applied voltage and the charging time interval. Besides, the total quantity of storage charge depends on the initial charge stored in the oxide before the voltage is applied. Therefore the storage charge is not a single valued function of a given voltage and time interval. The hysterisis behavior is thus expected for the implanted SiO_2 MOS structures.

Fig. 6 shows the hysterisis loops of the 70 *keV* implanted samples. The flat-band voltage shifts as well as the storage charge vs. applied voltage are plotted with charging time interval as a parameter. Curve A is the steady state curve, which is a single valued function, and no hysterisis occurs. Curves B, C, D and E show the transient state hysterisis loops with charging time interval t=50,5,1 and 0.001 sec respectively. As one can see from the hysterisis loops B, C and D, the loops become closer to the steady state curve A as the time interval is increasing from 1 sec. to 50 sec. For charging time becomes infinitely large, the hysterisis would reduce to the single valued A corresponding to the steady state. Therefore, the

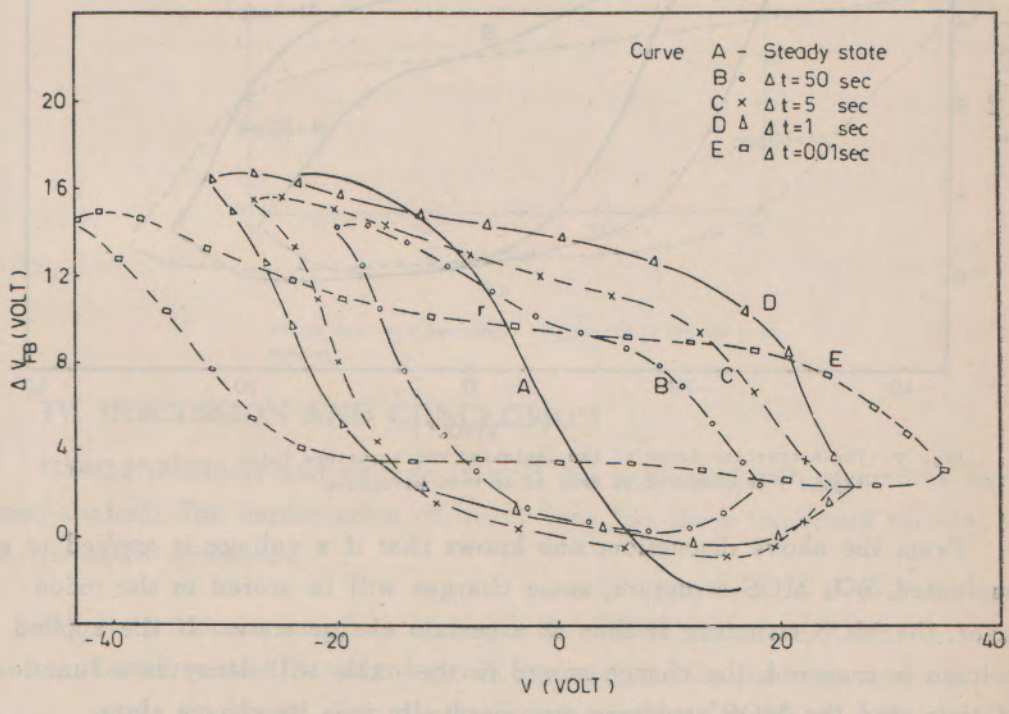

Fig 6

The hysterisis loops of 70 keV ion implanted MOS structures. The oxide thickness is 560Å.

height of the hysterisis loops, which represents the separation of the two charge states, should increase as the charging time intervals decrease (see loops B, C and D in Fig. 6). But if the charging time is too small, the storage charge can not change appreciably in this small time interval, thus the height of the hysterisis loop reduces, and a larger voltage is required to change the charge state (see loop E in Fig. 6).

Fig. 7 provides a comparison of the hysterisis loop between the implanted SiO_2 MOS structures (loop A and B) and the MNOS[5, 6] double layer structure (loop C). The implanted SiO_2 has a thickness of 560 Å implanted by 70 *keV* gold ions. The MNOS structure has both Si_3N_4 and SiO_2 layers with thickness at 800Å and 200Å respectively, By comparing both the separation of the charge states and the voltages required to change the charge states, one can see that the implanted SiO_2 MOS sturcture is potentially more useful as a non-volatile memory device.

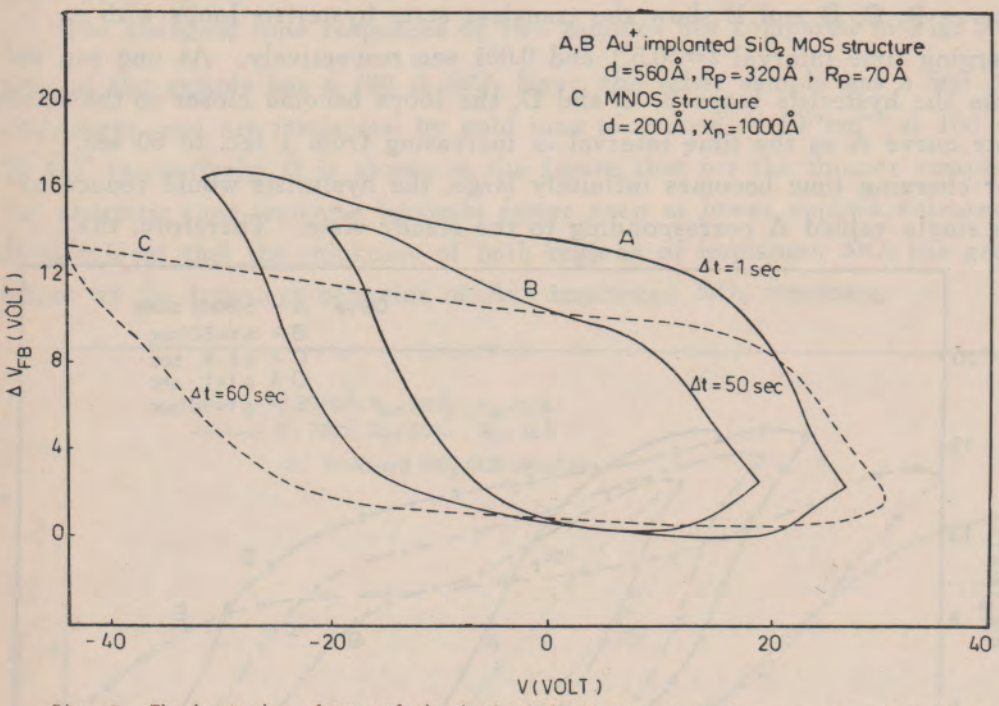

Fig. 7 The hysterisis loops of the implanted MOS structure (same sample as that in Fig.6) as compared to that of an MNOS structure.

From the above discussion, one knows that if a voltage is applied to an implanted SiO_2 MOS structure, some charges will be stored in the oxide layer, the MOS structure is thus at a certain charge state. If the applied voltage is removed, the charge stored in the oxide will decay as a function of time, and the MOS structure may gradually lose its charge state.

The path of charge decay is the very-low-conductivity oxide layer. The electric field in the structure after removal of applied voltage is due to

the stored charge and is sufficiently low that the discharge current is negligibly small.

The charge decay plot as a function of time is shown in Fig. 8. The 70 *keV* implanted SiO_2 MOS sample are used for this measurement. The initial decay is rapid, and then saturate with time. An extrapolation of the charge-decay results indicates that 70% of the initial charge can be retained for 10^5 min or one year. The retention time is quite long compared with the results of MNOS structure which is ranging from 10 to 10^5 min[7, 8].

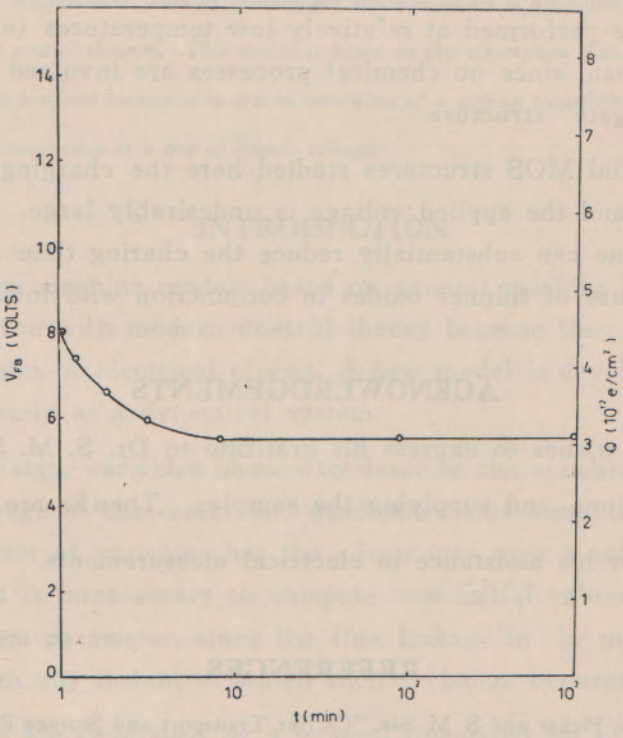

Fig 8

Charge decay as a function of time for the 70 keV implanted samples.

IV. DISCUSSION AND CONCLUSION

Charge transport and storage in gold ion implanted SiO_2 structures have been studied. The implantation of heavy ions has these important effects on the MOS structures:

(1) It introduces interface states at the Si-SiO_2 interface. The interface-state density depends strongly on the ion dose and the oxide thickness. For relatively thick oxides (compared with the ion projected range), most of the interface states can be annealed at temperatures below 400°C.

(2) It alters the conduction properties in the outer part of the insulator to a bulk-limited Frenkel-Poole mechanism.

(3) It introduces charge storage centers at the projected ion range.

The ion implanted MOS structure offers some favorable features as a potential multilayer-gate IGFET memory device: (1) it is repeatable, since the ion dose and energy are accurate to 1%, (2) it is pinhole free, since one can use relatively thick oxide (say 100Å) for structure instead of 20 to 30Å SiO_2 as in the MOS structure; (3) it involves low temperature processes since the implantation is done at room temperature and the subsequent annealing can be performed at relatively low temperatures (e.g., 400°C); and (4) it is clean, since no chemical processes are involved in forming the "multilayer-gate" structure.

For the initial MOS structures studied here the charging time is relatively long and the applied voltage is undesirably large. It is believed, however, that one can substantially reduce the charing time and the applied voltage by the use of thinner oxides in conjunction with lower implantation energies.

ACKNOWLEDGEMENTS

The author wishes to express his gratitute to Dr. S. M. Sze for his helpful discussions and supplying the samples. Thanks are also due to Mr. H. J. Wu or his assistance in electrical measurements.

REFERENCES

1. L. I. Chen, K. A. Pickar and S. M. Sze, "Carrier Transport and Storage Effects in Au Ion Implanted SiO_2 Structures", Solid-state Electronics, 1972. Vol. 15, pp. 979-986. Also presented at the 1971 Device Research Conference. Ann Arbor, Michigan, U.S.A.
2. H. E. Schiott, Private Communication,
3. A. Goetzberger, "Ideal MOS Curves for Silicon", Bell Syst. Tech. J., 45, 1070 (1966).
4. W. E. Dahlke, and S. M. Sze, "Tunneling in Metal Oxide-Silicon tructures", Solid-State Electron. 10, 865 (1967).
5. D. Frohman-Bentchkowsky, "The Metal-Nitride-Oxide-Silicon MNOS Transistor-Characteistics and Applications," Proc. IEEE, 58, 1207 (1970).
6. D. Frohman-Bentchkowsky, "Memory Behavior in a Floating-Gate Avalanche-Injection MOS (FAMOS) Structure", Applied Physics Letters, 18, 332 (1971).
7. E. C. Ross and J. T. Wallmark, "Theory of the Switching Behavior of MIS Memory Transistors", RCA Review, 30, 366 (1969).
8. D. Frohman-Bentchkowsky and M. Lezlinzer, "Charge Transport and Storage in Metal-Nitride-Oxide-Silicon (MNOS) Structures", J. Appl. Phys., (40), 3307 (1969).