The Design of Wideband and Low-Power CMOS Active Polyphase Filter and its Application in RF Double-Quadrature Receivers

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***Abstract*—In this work, a new technique to implement the transfer function of polyphase filter with CMOS active components is proposed and analyzed. In the proposed polyphase filter structure, the currents mirrored from capacitors and the transistors in a single-stage are used to realize high-pass and low-pass functions, respectively. The multistage structure expands the frequency bandwidth to more than 20 MHz. Furthermore, a constant-gm bias circuit is employed to decrease the sensitivity of image rejection to temperature and process variations. HSPICE simulations are performed to confirm the performance. With the current-mode operation, the low-voltage version of proposed active polyphase filters was designed. It can be operated at 1-V power supply with similar performance but with only 50% of the power dissipation of the normal-voltage version. The proposed four-stage polyphase filter is fabricated in 0.25-μm CMOS 1P5M technology. The measured image rejection ratio is higher than -48 dB at frequencies of 6.1 MHz $\sim$ 30 MHz. The measured voltage gain is 6.6 dB at 20 MHz and IIP3 is 8 dBm. The power dissipation is 11 mW at a supplied voltage of 2.5 V and the active chip area is 1162×813 μm^2.**

***Index Terms*—CMOS technology, double-quadrature architecture, low intermediate frequency architecture, polyphase filter, RF receiver.**

I. Introduction

THE fast growth of wireless applications in recent years has driven intense efforts to design highly integrated, high-performance, low-cost RF integrated circuits (ICs). Both low intermediate frequency (IF) [1]–[3] and double-quadrature [4]–[6] architectures have been adopted as promising receiver topologies to realize these design goals because they combine the advantages of IF and zero-IF architectures. In the low-IF receiver [1]–[3], the RF signal is amplified and down-converted to a low IF signal in a single step through the quadrature converter. After down-conversion, polyphase filters must be used to filter image signals at the intermediate frequency for both I and Q channels. DC offsets and $1/f$-noise do not disrupt the desired signal since this signal is brought to the intermediate frequency beyond the $1/f$-noise corner. The use of on-chip polyphase filters facilitates the integration of low-IF receivers. In the double-quadrature receiver (DQR) [4]–[6], the low-IF architecture is incorporated to further improve the sensitivity in multipath mismatches on a low-IF receiver. In the DQR, both RF and image signals are separated into quadrature phases. After down-conversion, on-chip polyphase filters are also required to sieve out the desired signal at the intermediate frequency and achieve high integration.

To avoid the signal-to-noise ratio (SNR) degradation by image interferences, a polyphase filter should provide high selectivity between the desired and image signals. Moreover, the power consumption must be low to prolong the lifetime of the batteries for use in portable wireless communications systems. Polyphase filters in some current standard applications require wide bandwidths. For example, a 20-MHz channel bandwidth is required for WLAN IEEE 802.11a and HIPERLAN. Accordingly, the design of high-performance, wideband, and low-power on-chip polyphase filters for these applications are critically needed.

So far, many polyphase filters have been proposed [3], [7]–[11]; they can be divided into two types, namely passive *RC* polyphase filters and active polyphase filters. Passive *RC* polyphase networks are used in passive *RC* polyphase filters [3], [7], [8]. The voltage transfer function of the *RC* polyphase networks depends on the phase order of the input sequence; it can distinguish between signals with positive frequencies and those with negative frequencies. The passive *RC* polyphase filter can exhibit a high image rejection ratio (IRR), but has a limited range of operating frequencies. The desirable filtering function can only be obtained in the narrow band around the pole frequency, which depends on the *RC* time constant. To increase the bandwidth, a multistage network is proposed to achieve the broadband response [3], [7], [8].

The expense of the multistage passive polyphase filter is that it is lossy, so its output signal decays. Additional buffers should be inserted among the stages to compensate the loss. However, these buffers significantly increase the power consumption. More power is consumed as more stages are used to increase the bandwidth. Furthermore, the variation of resistances and capacitances should be kept within a desired small range to achieve a high IRR. This means large chip area is required because the variations of adjacent on-chip resistances and capacitances are inversely proportional to their surface area. As the area of resistors increases, it also increases the parasitic capacitance and lowers the cut-off frequencies of resistors. Thus, a critical tradeoff must be made among IRR, chip area

Manuscript received April 1 2004; revised October 5, 2004. This work was supported by the National Science Council (NSC), Taiwan, R.O.C., under Grant NSC 91-2215-E-009-080. This paper was recommended by Associate Editor B. Maundy.

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Digital Object Identifier 10.1109/TCSI.2005.846672

and maximum operational frequency of passive *RC* polyphase filters.

Active polyphase filters have the general advantages of low power dissipation, small chip area and high signal gain. All the active polyphase filters proposed so far [9]–[11] have operating frequencies in the range of several hundreds of kilohertz to several of megahertz. The polyphase filter in [9] provides a good IRR at 250 kHz by using op-amp circuits. In [10], the active gm-c polyphase filter provides a -53 dB of IRR at 3 MHz without tuning circuits by using a well-controlled special analog process. In [11], the gm-c polyphase filter with common-mode feedback (CMFB) and common-mode feed forward (CMFF) circuits and frequency-tuning circuits, can achieve more than -45 dB of IRR in a bandwidth of 1 MHz with a central frequency of 2 MHz.

In this work, a new broadband CMOS active polyphase filter with a wide range of operating frequencies is proposed and designed by using the basic polyphase filter architecture which is used to implement passive *RC* polyphase filter. A constant-gm bias circuit is used to decrease the sensitivities of the filter gain and the bandwidth to temperature and process variations. Additionally, the multistage approach is also applied to achieve the wide bandwidth. Due to the high input impedance in each stage, the proposed active polyphase filter can avoid the degradation of gain between pairs of stages when connected in cascade. Thus, power-consuming buffers are not required. Using 0.25-μm CMOS 1P5M technology, the proposed four-stage active polyphase phase filter can achieve an IRR of -48 dB in the 6.1 MHz $\sim$ 30 MHz band. The filter consumes 11 mW (5.5 mW) with a power supply of 2.5 V (1 V). A higher IRR can be achieved by increasing the number of cascaded stages although the achievable IRR is limited by matching.

The active polyphase filter has been designed and integrated into a DQR in 0.18-μm CMOS 1P6M technology [5], [6]. The measured -50.6 dB IRR verifies that the proposed active polyphase filter is suitable for wireless communication applications.

The rest of this paper is organized as follows. Section II presents the models of a polyphase filter and DQR. Section III describes the circuit implementations of the proposed active polyphase filter. HSPICE simulation results verify the functions of the circuits. Section IV presents experimental results. Finally, Section V draws conclusions.

II. Models for Polyphase Filters and DQR

A. Model for Polyphase Filters

The polyphase filter is a complex filter because its frequency response is not symmetrical around dc. The transfer function $H(s)$ of a complex filter can be represented as [8]

$$H(s) = H_1(s) + jH_2(s) \tag{1}$$

where $H_1(s)$ and $H_2(s)$ are the real and imaginary parts of the complex transfer function. If a complex signal $C_i(s) = I_i(s) + jQ_i(s)$ is applied to this complex filter, the output signal $C_o(s)$ can be written as

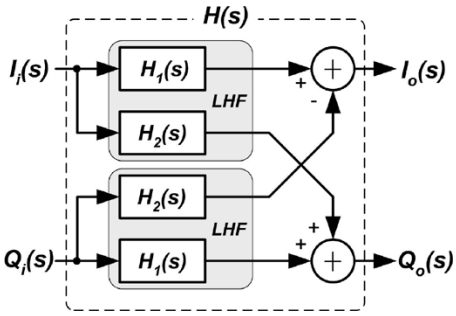

Fig. 1. Signal flowgraph for realizing a single-stage complex filter [8].

$$C_o(s) = C_i(s)H(s) = I_o(s) + jQ_o(s) \tag{2}$$

$$I_o(s) = I_i(s)H_1(s) - Q_i(s)H_2(s) \tag{3}$$

$$Q_o(s) = I_i(s)H_2(s) + Q_i(s)H_1(s) \tag{4}$$

where $I_o(s)$ and $Q_o(s)$ are the real and imaginary parts of $C_o(s)$, respectively. If $C_o(s)$ can be generated by a circuit from the input complex signal $C_i(s)$ according to (3) and (4), then the complex transfer function $H(s)$ can be realized by this circuit. Fig. 1 [8] shows the signal flowgraph for the realization of $H(s)$ by using (3) and (4). In this way, any complex filter can be realized by a combination of the real and imaginary parts of its transfer functions.

The transfer function $H(s)$ of the one-stage *RC* network can be used to implement a polyphase filter, according to the approach presented above. The resultant transfer function $H(s)$ is represented as

$$H(s) = H_1(s) + jH_2(s) = \frac{A\omega_P}{s+\omega_P} + j\frac{As}{s+\omega_P} \tag{5}$$

where A and ω_P are the gain and pole frequency, respectively, of the first-order low-pass filter $H_1(s)$ and the high-pass filter $H_2(s)$. The combination of $H_1(s)$ and $H_2(s)$ forms a block denoted as the low-high-pass filter (LHF) in Fig. 1. According to (5), the transfer curves of $|H(j\omega)|$ and $|H(-j\omega)|$ versus frequency for $A = 1$ and $\omega_P = 10$ MHz are shown in Fig. 2 in solid lines. Notably, the desired signal with negative frequency falls in the filter's passband while the image signal at positive frequency is attenuated. $|H(j\omega)|$ is lowest at $\omega = \omega_P$ where ω_P is also called the rejected frequency. Using the equation in (5), the IRR $\mathrm{IRR_{PPF}}$ of the polyphase filter defined as the ratio of the magnitude in the attenuation band to that in the passband, can be derived as

$$\mathrm{IRR_{PPF}}(\omega) = \frac{|H(s=j\omega)|}{|H(s=-j\omega)|} = \left|\frac{\omega_p - \omega}{\omega_p + \omega}\right|. \tag{6}$$

As may be seen from (6), the $\mathrm{IRR_{PPF}}$ can be zero at frequency ω_P if the gains and pole frequencies of $H_1(s)$ and $H_2(s)$ are perfectly matched.

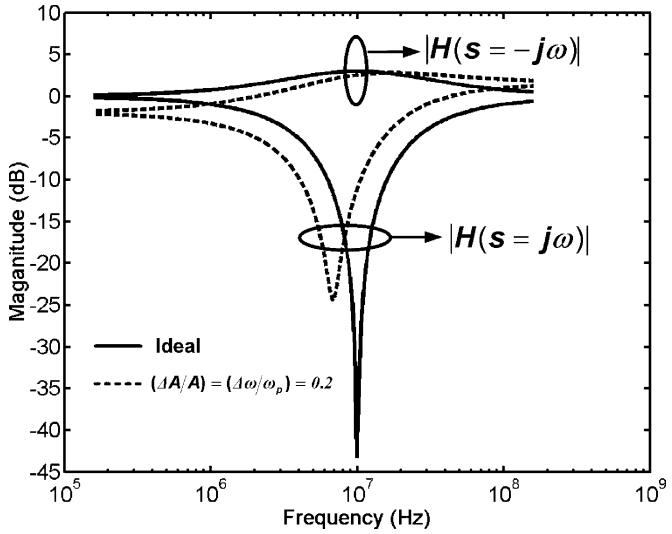

Fig. 2. Transfer curves of $|H(s)|$ versus frequency.

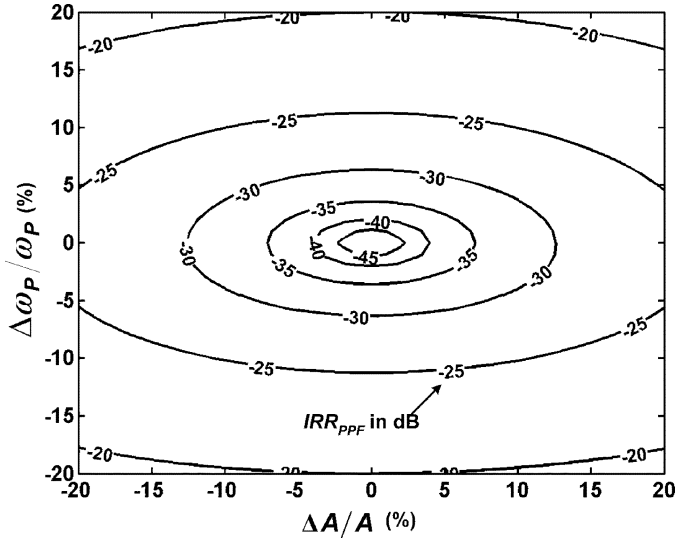

Fig. 3. Simulated $\mathrm{IRR_{PPF}}$ values (indicated on the curves) of one-stage polyphase filter at $\omega = \omega_p$ with gain and pole frequency variations.

If the gains and pole frequencies of $H_1(s)$ and $H_2(s)$ are not identical because of mismatching, then (5) can be rewritten as

$$H(s) = \frac{A\omega_P\left(1-\frac{\Delta A}{2A}\right)\left(1-\frac{\Delta\omega_P}{2\omega_P}\right)}{s+\omega_P\left(1-\frac{\Delta\omega_P}{2\omega_P}\right)} + j\frac{A\left(1+\frac{\Delta A}{2A}\right)s}{s+\omega_P\left(1+\frac{\Delta\omega_P}{2\omega_P}\right)} \tag{7}$$

where ΔA and $\Delta\omega_P$ are the mismatch quantities of A and ω_P, respectively. The simulated $|H(j\omega)|$ and $|H(-j\omega)|$ versus frequency with 20% variations are shown by the dashed lines in Fig. 2. It is shown that the transfer curves of $H(s = j\omega)$ and $H(s = -j\omega)$ are shifted to the opposite directions and the resulting $\mathrm{IRR_{PPF}}$ at $\omega = \omega_P$ is degraded. Using (7) and neglecting high-order terms, the IRR $\mathrm{IRR_{PPF}}$ with mismatch effects can be derived as (8) at the shown at the bottom of the page. Fig. 3 depicts the exact $\mathrm{IRR_{PPF}}(\omega = \omega_p)$ with the corresponding mismatches $\Delta\omega_P/\omega_P$ and $\Delta A/A$, where the numbers on the curves denote the $\mathrm{IRR_{PPF}}$ values in decibels. The figure demonstrates that if $|\ \Delta A/A\ | > 12\%$ or $|\ \Delta\omega/\omega_P\ | > 5\%$, then the $\mathrm{IRR_{PPF}}$ at $\omega = \omega_P$ is degraded to -30 dB. Therefore, the gains and locations of the pole frequencies in $H_1(s)$ and $H_2(s)$ should be kept highly consistent to achieve the desired image rejection performance.

A broadband polyphase filter can be realized by cascading several stages of one-stage polyphase filter. The resultant IRR $\mathrm{IRR_{PPFN}}$ of the N-stage polyphase filter can be derived by multiplying all $\mathrm{IRR_{PPF}}$ values of the constituent one-stage polyphase filters as

$$\mathrm{IRR_{PPFN}}(\omega) = \prod_{n=1}^{N} \mathrm{IRR_{PPF},}_{n}(\omega) \tag{9}$$

where $\mathrm{IRR_{PPF},}_{n}$ is the $\mathrm{IRR_{PPF}}$ of the nth-stage polyphase filter. Ideally, the IRR can be improved with a cascaded multistage structure, as indicated by (9). But in the practical case, the highest achievable IRR is limited by the inevitable circuit mismatches among stages. Note that the range of operating frequencies can also be expanded by assigning a different value of ω_P to each one-stage polyphase filter.

B. Model for the DQR

Fig. 4 shows the structure of a DQR, in which polyphase filters are used in both I and Q channels. The difference between the DQR and the conventional low-IF receiver is that, after the LNA has amplified the RF input signal, the quadrature generator transforms this into the in-phase and quadrature-phase signals RF_I and RF_Q. Both RF_I and RF_Q signals are sent to the four down-conversion mixers, along with the input quadrature signals LO_I and LO_Q from the quadrature VCO, to realize the complex multiplication function $\mathrm{IF}_I + j\mathrm{IF}_Q = (\mathrm{RF}_I - j\mathrm{RF}_Q)\cdot$

$$\mathrm{IRR_{PPF}}(\omega) \cong \left\{ \frac{\left[64A^2(\omega^4-\omega_P^4)\frac{\Delta A}{A} + 64A^2\omega\omega_P(\omega-\omega_P)^2\frac{\Delta\omega_P}{\omega_P} + 64A^2(\omega^2+\omega_P^2)(\omega-\omega_P)^2 + 16A^2(\omega^2+\omega_P^2)(\omega+\omega_P)^2\left(\frac{\Delta A}{A}\right)^2 + 32A^2\omega_P^2(\omega^2-\omega_P^2+\omega\omega_P)\left(\frac{\Delta\omega_P}{\omega_P}\right)^2\right]}{\left[64A^2(\omega^4-\omega_P^4)\frac{\Delta A}{A} - 64A^2\omega\omega_P(\omega+\omega_P)^2\frac{\Delta\omega_P}{\omega_P} + 64A^2(\omega^2+\omega_P^2)(\omega+\omega_P)^2\right]} \right\}^{1/2} \tag{8}$$

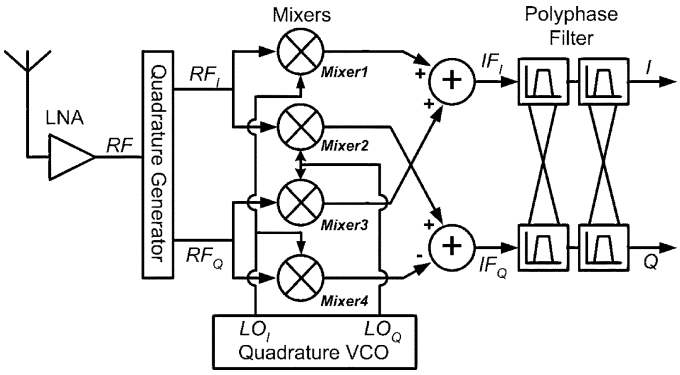

Fig. 4. Block diagram of DQR.

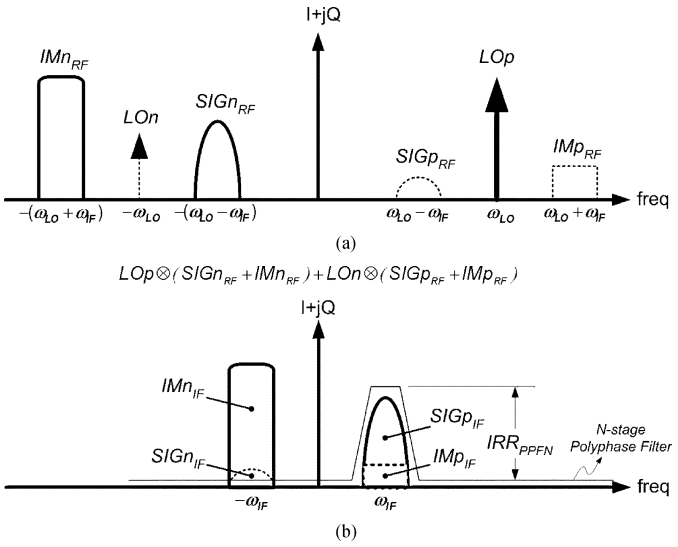

Fig. 5. Signal spectra in the DQR (a) before the down-conversion and (b) after the down-conversion.

$(\mathrm{LO}_I + j\mathrm{LO}_Q)$ and generate the intermediate frequency signals IF_I and IF_Q. The poylphase filters are used to filter the image signals at the intermediate frequency to prevent interference with the desired signals.

Using the complex signal representation [4], Fig. 5(a) and (b) display the signal spectra in the DQR before and after down-conversion, respectively. $\mathrm{SIG}n_{\mathrm{RF}}$ and $\mathrm{IM}n_{\mathrm{RF}}$ in Fig. 5(a) refer to the spectra of the desired signals and the image signals at the output of the quadrature generator, respectively. $\mathrm{LO}p$ refers to the spectrum of the quadrature local oscillation signals. Thus, $\mathrm{RF}_I - j\mathrm{RF}_Q = \mathrm{SIG}n_{\mathrm{RF}} + \mathrm{IM}n_{\mathrm{RF}}$ and $\mathrm{LO}_I + j\mathrm{LO}_Q = \mathrm{LO}p$. $\mathrm{SIG}p_{\mathrm{RF}}$, $\mathrm{IM}p_{\mathrm{RF}}$ and $\mathrm{LO}n$ represent the crosstalk image signals of $\mathrm{SIG}n_{\mathrm{RF}}$, $\mathrm{IM}n_{\mathrm{RF}}$ and $\mathrm{LO}p$, respectively. The image-to-signal ratio (ISR) $\mathrm{SIG}p_{\mathrm{RF}}/\mathrm{SIG}n_{\mathrm{RF}}$, $\mathrm{IM}p_{\mathrm{RF}}/\mathrm{IM}n_{\mathrm{RF}}$ and $\mathrm{LO}n/\mathrm{LO}p$ can be calculated by the corresponding phase and amplitude mismatches [4]. After the frequency translation, as shown in Fig. 5(b), the $\mathrm{SIG}p_{\mathrm{RF}}$, $\mathrm{SIG}n_{\mathrm{RF}}$, $\mathrm{IM}p_{\mathrm{RF}}$ and $\mathrm{IM}n_{\mathrm{RF}}$ are down-converted to $\mathrm{SIG}n_{\mathrm{IF}}$, $\mathrm{SIG}p_{\mathrm{IF}}$, $\mathrm{IM}p_{\mathrm{IF}}$ and $\mathrm{IM}n_{\mathrm{IF}}$, respectively. The image $\mathrm{IM}p_{\mathrm{IF}}$ mixes with $\mathrm{SIG}p_{\mathrm{IF}}$ at ω_{IF} and cannot be removed by the following polyphase filters. The value of $\mathrm{IM}p_{\mathrm{IF}}$ can be represented as

$$\mathrm{IM}p_{\mathrm{IF}} = \mathrm{IM}n_{\mathrm{RF}}\mathrm{LO}p\,(\mathrm{ISR}_{QG}\mathrm{ISR}_{\mathrm{LO}} + \mathrm{ISR}_{\mathrm{Mixers}}) \quad (10)$$

where ISR_{QG}, $\mathrm{ISR}_{\mathrm{LO}}$ and $\mathrm{ISR}_{\mathrm{Mixers}}$ denote the ISRs caused by imbalances in the quadrature generator, the local oscillator and the mixers, respectively. For ISR_{QG}, $\mathrm{ISR}_{\mathrm{LO}}$ and $\mathrm{ISR}_{\mathrm{Mixers}} \ll 1$, the $\mathrm{ISR}_{QG}\mathrm{ISR}_{\mathrm{LO}}$ term in (10) is negligible relative to $\mathrm{ISR}_{\mathrm{Mixers}}$. Therefore, $\mathrm{IM}p_{\mathrm{IF}}$ is determined by the gain/phase errors of the mixers and $\mathrm{IM}n_{\mathrm{RF}}Lop$. The DQR exhibits better image rejection performance than the conventional low-IF receiver, because $\mathrm{IM}p_{\mathrm{IF}}$ is smaller and almost unaffected by $\mathrm{ISR}_{\mathrm{LO}}$.

The image $\mathrm{IM}n_{\mathrm{IF}}$, which is down-converted from $\mathrm{IM}n_{\mathrm{RF}}$, is located at $-\omega_{\mathrm{IF}}$ whereas the desired signal $\mathrm{SIG}p_{\mathrm{IF}}$ is at ω_{IF}. The polyphase filters should reject $\mathrm{IM}n_{\mathrm{IF}}$ at $-\omega_{\mathrm{IF}}$ to prevent interference with the $\mathrm{SIG}p_{\mathrm{IF}}$. If the multistage polyphase filter can provide an IRR $\mathrm{IRR}_{\mathrm{PPFN}}$, then the total IRR $\mathrm{IRR}_{\mathrm{DQR}}$ of the DQR can be derived by using (10), and the relations $\mathrm{IM}n_{\mathrm{IF}} = \mathrm{IM}n_{\mathrm{RF}}\mathrm{LO}p$, $\mathrm{SIG}p_{\mathrm{IF}} = \mathrm{SIG}n_{\mathrm{RF}}Lop$ and $\mathrm{SIG}n_{\mathrm{IF}} = \mathrm{SIG}n_{\mathrm{RF}}\mathrm{LO}p(\mathrm{ISR}_{QG}\mathrm{ISR}_{\mathrm{LO}}+\mathrm{ISR}_{\mathrm{Mixers}})$. Neglecting the high-order terms yields

$$\begin{aligned}\mathrm{IRR}_{\mathrm{DQR}} &\equiv \frac{\frac{(\mathrm{IM}p_{\mathrm{IF}}+\mathrm{IM}n_{\mathrm{IF}}\mathrm{IRR}_{\mathrm{PPFN}})}{(\mathrm{SIG}p_{\mathrm{IF}}+\mathrm{SIG}n_{\mathrm{IF}}\mathrm{IRR}_{\mathrm{PPFN}})}}{\frac{\mathrm{IM}n_{\mathrm{RF}}}{\mathrm{SIG}n_{\mathrm{RF}}}} \\ &= \frac{\mathrm{ISR}_{QG}\mathrm{ISR}_{\mathrm{LO}} + \mathrm{ISR}_{\mathrm{Mixers}} + \mathrm{IRR}_{\mathrm{PPFN}}}{1 + (\mathrm{ISR}_{QG}\mathrm{ISR}_{\mathrm{LO}} + \mathrm{ISR}_{\mathrm{Mixers}})\mathrm{IRR}_{\mathrm{PPFN}}} \\ &\cong \mathrm{ISR}_{\mathrm{Mixers}} + \mathrm{IRR}_{\mathrm{PPFN}}. \end{aligned} \quad (11)$$

As may be seen from (11), the overall IRR of the DQR is determined mainly by the ISR of the mixers and the IRR of the polyphase filter. To achieve high $\mathrm{IRR}_{\mathrm{DQR}}$, the symmetry of the layout in mixers between the I and Q channels should be regarded as reducing the amplitude of crosstalk image signals. Additionally, the polyphase filter must have a high capacity for rejecting images at intermediate frequencies.

III. Circuit Implementation

A. 2.5-V Polyphase Filter

The proposed polyphase filter structure in Fig. 1 consists of a low-pass filter $H_1(s)$ and a high-pass filter $H_2(s)$ in each of the two LHF blocks. The CMOS realization of a LHF block is shown in Fig. 6(a) where the functions of $H_1(s)$ and $H_2(s)$ are combined. In Fig. 6(a), the nMOS device M_1 converts the input voltage V_I to current i_1 and then the current is mirrored to i_3 and i_4 by the pMOS current mirrors M_2, M_3, and M_4. The diode-connected transistor M_L and the capacitor C_H then divide the mirrored current i_3 into i_L and i_H, , respectively. The currents i_L and i_H can be derived as

$$i_L = V_I \frac{gm_1\left(\frac{gm_L}{C_H}\right)}{s + \left(\frac{gm_L}{C_H}\right)} \quad (12)$$

$$i_H = V_I \frac{gm_1 s}{s + \left(\frac{gm_L}{C_H}\right)} \quad (13)$$

where gm_1 and gm_L are the transconductances of M_1 and M_L, respectively. Using the mirrored currents i_L and i_H, the required

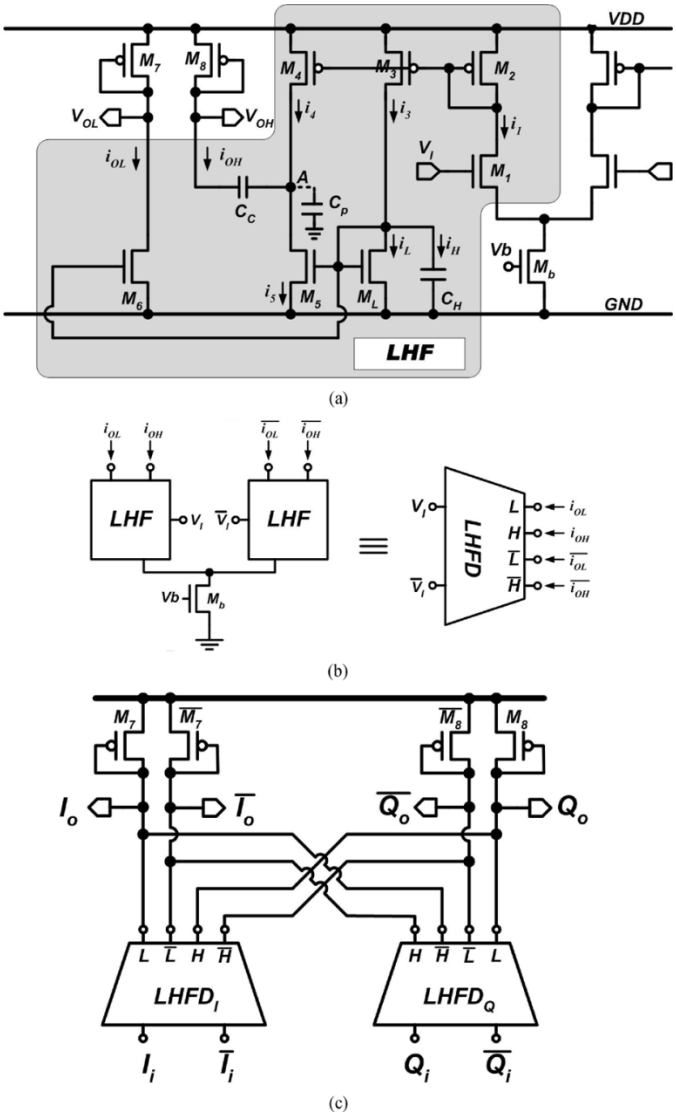

Fig. 6. (a) Circuit of LHF. (b) Differential type of LHF and its equivalent functionality block LHFD. (c) Block diagram of $H(s)$.

low-pass and high-pass transfer functions $H_1(s)$ and $H_2(s)$ can be realized as

$$\begin{aligned} H_1(s) &= \frac{V_{OL}}{V_I} = \frac{1}{gm_7} i_{OL} \\ &= \frac{1}{gm_7} K_L i_L \\ &= K_L \frac{\left(\frac{1}{gm_7}\right) gm_1 \left(\frac{gm_L}{C_H}\right)}{s + \left(\frac{gm_L}{C_H}\right)} \end{aligned} \tag{14}$$

$$\begin{aligned} H_2(s) &= \frac{V_{OH}}{V_I} = \frac{1}{gm_8}(i_{OH}) \\ &= -\frac{1}{gm_8}(i_4 - i_5) \\ &= -\frac{1}{gm_8}(K_H i_3 - K_H i_L) \\ &= -\frac{1}{gm_8} K_H i_H \\ &= -K_H \frac{\left(\frac{1}{gm_8}\right) gm_1 s}{s + \left(\frac{gm_L}{C_H}\right)} \end{aligned} \tag{15}$$

where K_L is the current ratio of M_6 and M_L, K_H is the current ratio of $M_4(M_5)$ and $M_3(M_L)$, and $gm_7(gm_8)$ is the transconductance of $M_7(M_8)$. The capacitor C_C connected between node A and V_{OH} is used to pass the ac current $i_{OH} = i_4 - i_5$, but block the dc voltage. The rejected frequency ω_P can be adjusted by changing C_H since the poles of both transfer functions $H_1(s)$ and $H_2(s)$ are determined by $\omega_P = gm_L/C_H$.

The parasitic effects of the LHF circuit in Fig. 6(a) are analyzed. The parasitic capacitance C_P at node A has the largest value as compared to those at other nodes, because C_P consists of the parasitic capacitance of C_C and the device capacitance of M_4 and M_5. With C_P at node A, the transfer function of $H_2(s)$ can be derived as

$$H_2(s) = -K_H \left[\frac{\left(\frac{1}{gm_8}\right) gm_1 s}{s + \left(\frac{gm_L}{C_H}\right)}\right] \left[\frac{\frac{gm_8}{C_P}}{s + \frac{gm_8(C_C + C_P)}{C_C C_P}}\right]. \tag{16}$$

As (16) shows, the second pole at $\omega_{P2} = gm_8(C_C + C_P)/C_C C_P$ is generated. Since ω_{P2} may affect the magnitude and phase of $H_2(s)$ and thus degrade the IRR of the polyphase filter, ω_{P2} should be kept at least ten times larger than ω_P to minimize the degradation of IRR.

Based on the structure illustrated in Fig. 1, a one-stage polyphase filter $H(s)$ with a differential structure can be realized by the combination of LHF circuits. In general, the mixers used in the receiver are designed in differential circuits to cancel the LO-to-IF feedthrough. Thus the proposed polyphase filter is designed in differential type to process the differential output signals from the mixers. Fig. 6(b) shows the differential LHF, LHFD. The LHFD consists of two LHFs with a common current source device M_b, which is used to provide the bias current of LHF and reject the input common mode signal. Fig. 6(c) shows the complete circuit of one-stage polyphase filter, based on the structure in Fig. 1. The output node $L(\overline{L})$ of LHFD_I is connected to the output node $\overline{H}(H)$ of LHFD_Q to realize the subtraction function in Fig. 1, whereas the summation function in Fig. 1 is realized by connecting the output node $H(\overline{H})$ of LHFD_I to the output node $L(\overline{L})$ of LHFD_Q. Finally, the output currents are converted to voltages by connecting them to diode-connected transistors M_7, $\overline{M_7}$, M_8 and $\overline{M_8}$. Fig. 6(c) realizes the signal flowgraph of Fig. 1 in differential structure.

A broadband multistage polyphase filter can be realized by cascading several stages of one-stage polyphase filters. Unlike the passive *RC* polyphase filter, cascading the proposed active polyphase filters can avoid the degradation of gain among stages because the input impedance in each stage is high. In each stage, C_H should be adjusted to obtain different reject frequencies. All other circuits in Fig. 6(c) remain unchanged, greatly reducing the complexity of the design of a multistage polyphase filter.

According to (14) and (15), both the gains and the poles of the transfer functions $H_1(s)$ and $H_2(s)$ are dependant on the transconductances of transistors. Therefore, the transconductances are important parameters and must be stabilized. The stability of gm is achieved by using a constant-gm bias circuit [12], as shown in Fig. 7. With the parameters shown in Table I, the HSPICE simulation shows that the transconductance variations of M_1 in Fig. 7 can be kept within 2.3% and 2% with the four corners (FF, FS, SF, and SS) of device model parameters and

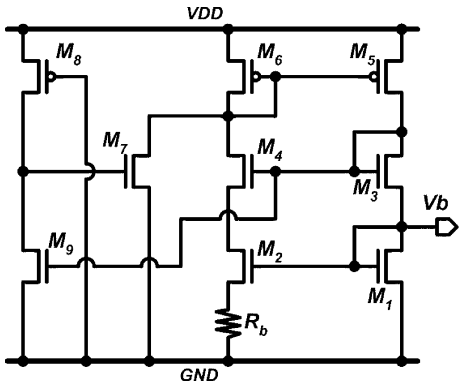

Fig. 7. Circuit of constant-gm bias.

TABLE I
DIMENSIONS OF DEVICES IN CONSTANT-GM BIAS CIRCUIT AND POLYPHASE FILTER

Constant-gm bias circuit	
M_1	(4um/1um)
M_2	(4um/1um) • 4
M_3	(1um/1um)
M_4	(1um/2um)
M_5	(8um/1um)
M_6	(8um/1um)
M_7	(4um/1um)
M_8	(0.5um/20um)
M_9	(1um/1um)
R_b	6kΩ
Polyphase filter	
M_1	(0.5um/0.5um) • 4
M_2	(2.5um/0.5um) • 4
M_3	(2.5um/0.5um) • 8
M_4	(2.5um/0.5um) • 4
M_5	(0.5um/0.5um) • 4
M_6	(0.5um/0.5um) • 4
M_7, M_8	(2.5um/0.6um) • 4
M_b	(5um/1um) • 4
M_L	(2.5um/0.5um) • 8
C_H	4 stages: 3.5pF, 5.5pF, 10pF, 16pF
C_C	C_H/2

variations in the temperature between 0° and 80°, respectively. The performance of a one-stage polyphase filter that incorporates the constant-gm bias circuit with $\omega_P = 25$ MHz is verified. The $\mathrm{IRR_{PPF}}$ at 25 MHz can exceed -42 dB and -49.3 dB, respectively. Accordingly, the desired $\mathrm{IRR_{PPF}}$ can be achieved under process and temperature variations.

As seen from (7) and (8), the $\mathrm{IRR_{PPF}}(\omega = \omega_P)$ is degraded if the gain and pole frequencies of $H_1(s)$ and $H_2(s)$ are not identical. Since the pole frequencies of $H_1(s)$ and $H_2(s)$ shown in (14) and (15) are identically determined by gm_L and C_H, the pole frequencies mismatch can be avoided. The gain mismatch between $\mid H_1(s = \omega_P) \mid$ and $\mid H_2(s = \omega_P) \mid$ can be reduced to the balance between K_L/gm_7 and K_H/gm_8. K_L and K_H are current ratios and the mismatch can be kept small. To reduce the mismatch of gm_7 and gm_8, the layout of M_7 and M_8 can be put in common centroid. Moreover, minimum channel

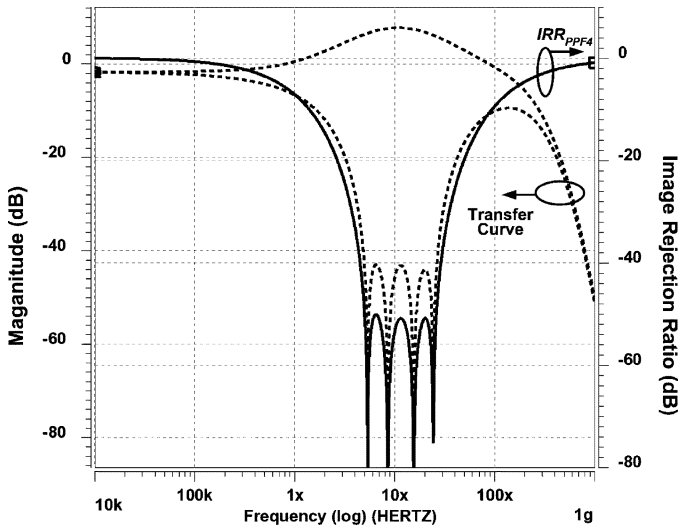

Fig. 8. HSPICE simulated transfer curve and $\mathrm{IRR_{PPF4}}$ of the 2.5-V four-stage CMOS polyphase filter.

length is not used in this design to further reduce the gain mismatch. In the passive *RC* polyphase filter, the gain mismatch depends on not only the matching in *RC* values and transconductances of buffers in I/Q paths, but also parasitic capacitors of resisters. In comparison with the mismatch effects of current ratio and tansconductance in the proposed active polyphase filter, the $\mathrm{IRR_{PPF}}$ will not be worse than the one in passive *RC* polyphase filter.

With the random variations among components, the one-stage polyphase filter ($\omega_P = 25$ MHz) biased with a constant-gm circuit is verified by 30-times of Monte Carlo simulations. Except $C_C = 3.4$ pF, all other device dimensions are the same as the values listed in Table I. The variations of transistor parameters ΔW(channel width), ΔL(channel length) and $\Delta V_{\mathrm{th}(p,n)}$(threshold voltage) are randomly distributed according to the values provided by the corner parameters of the MOS device model, such that $\Delta W = \pm 0.03$ μm, $\Delta L = \pm 0.02$ μm, $\Delta V_{\mathrm{thp}} = \pm 0.05$ V and $\Delta V_{\mathrm{thn}} = \pm 0.06$ V. The relative variations of capacitance and resistances are 10%. The results of the simulation show that the worst $\mathrm{IRR_{PPF}}$ at 25 MHz still exceeds -40 dB.

A wide bandwidth polyphase filter with an IRR of -50 dB is realized in 0.25-μm 1P5M CMOS technology with a power supply of 2.5 V. Four one-stage polyphase filters are cascaded in this design to expand the bandwidth and enhance the tolerance of bandwidth variations. The capacitors C_H in the four one-stage polyphase filters are 3.5, 5.5, 10, and 16 pF, respectively. The resultant rejected frequencies are 24.5, 15.5, 8.5, and 5.4 MHz, respectively. Fig. 8 plots the simulated transfer curves at positive and negative frequencies and the IRR $\mathrm{IRR_{PPF4}}$ of the designed polyphase filter. It is shown that the $\mathrm{IRR_{PPF4}}$ can exceed -50 dB by the four-stage polyphase filter over the bandwidth 4.5 MHz $\sim$ 27.5 MHz. The total power consumption is 11 mW at a power supply of 2.5 V. The simulated common-mode-rejection ratio (CMRR) within the bandwidth in each one-stage polyphase filter is 41 dB.

HSPICE simulations are performed to verify the effects of process and temperature variations. The results in Fig. 9 show

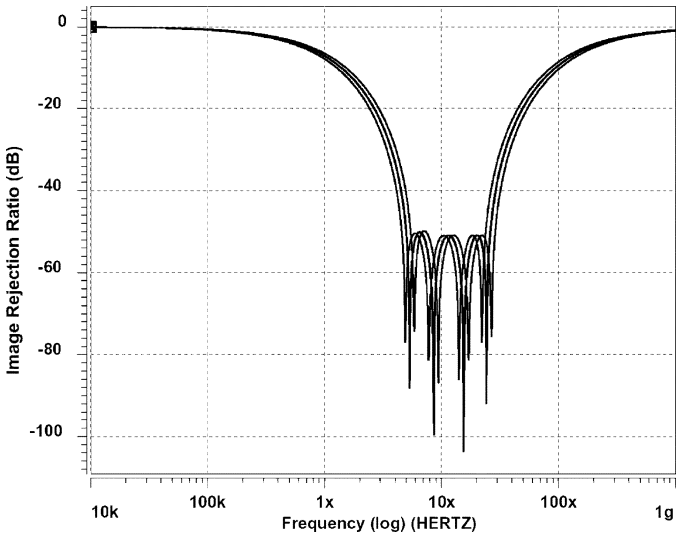

Fig. 9. HSPICE simulated IRR variations of the four-stage CMOS polyphase filter with four corners (FF, FS, SF, and SS) of MOS device models.

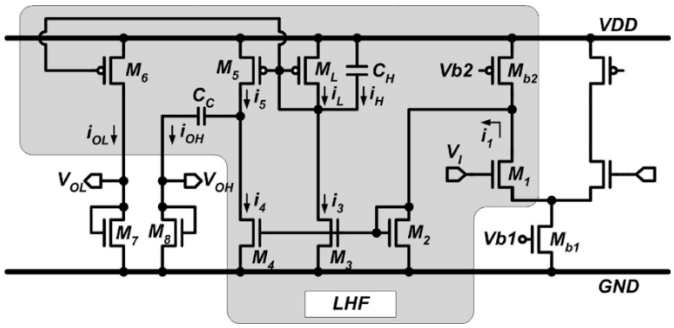

Fig. 10. Low-voltage version of LHF.

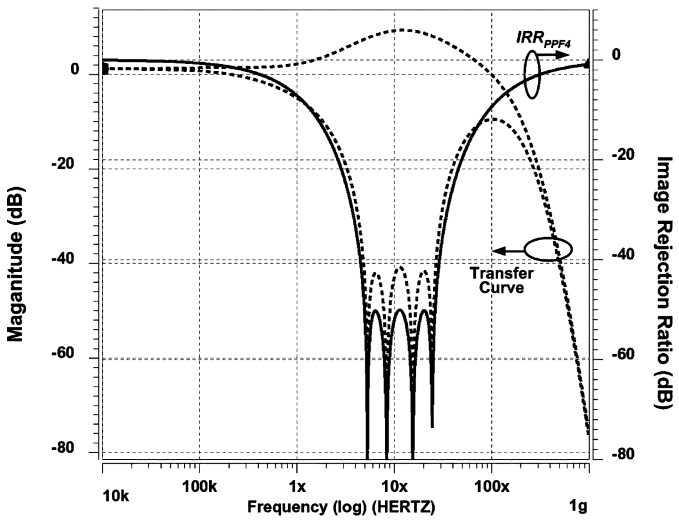

Fig. 11. HSPICE simulated transfer curve and $\mathrm{IRR}_{\mathrm{PPF4}}$ of the low-voltage four-stage CMOS polyphase filter.

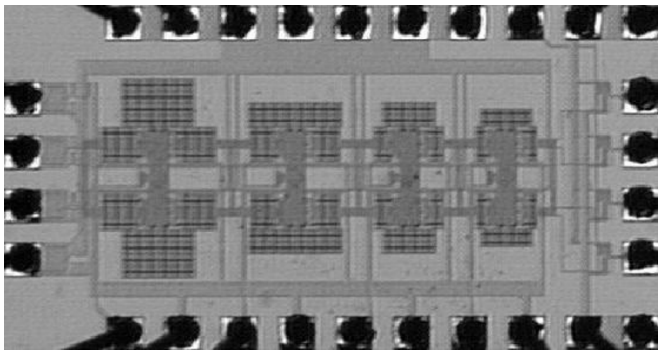

Fig. 12. Die micrograph of fabricated four-stage polyphase filter in 0.25-μm CMOS technology.

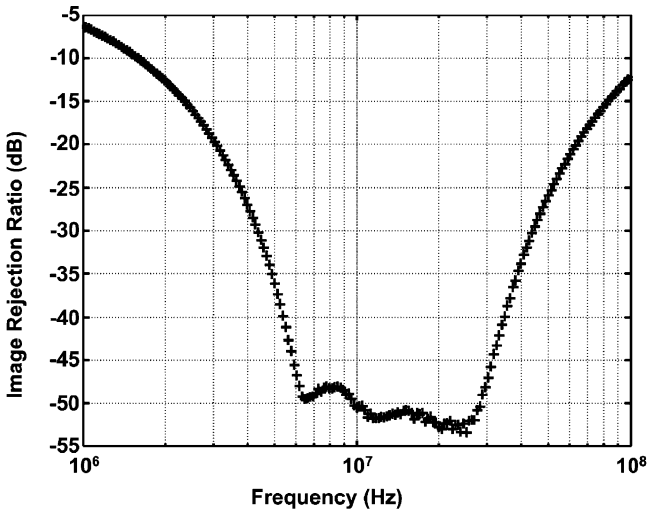

Fig. 13. Measured $\mathrm{IRR}_{\mathrm{PPF4}}$ of fabricated four-stage polyphase filter in 0.25-μm CMOS technology.

that the $\mathrm{IRR}_{\mathrm{PPF4}}$ exceeds -50 dB over the range of 5 MHz $\sim$ 26.5 MHz under the four corners of the MOS device models. As the temperature varies from 0° to 80°, an $\mathrm{IRR}_{\mathrm{PPF4}}$ of -50 dB can also be achieved within 4.75 to 27 MHz. Thus, the performance of the proposed polyphase filter can be well controlled as the process and temperature are varied.

B. 1-V Polyphase Filter

With the advantage of currents operation, the proposed active polyphase filters can be modified to operate at a low supplied voltage. Fig. 10 shows the low-voltage version of LHF where the transistor M_2 is connected in a folded structure. Therefore, the required power supply can be as low as the threshold voltage $V_{\mathrm{th}2}$ of M_2 plus the drain–source voltage $V_{\mathrm{DS}b2}$ of M_{b2}. M_{b2} works as a current source, which provides a constant dc current to M_1. Because of the high impedance at the drain of M_{b2}, the current i_1, which is generated from the input voltage signal V_I by M_1, flows to M_2 and then mirrored to i_3. The functions of other transistors are similar to those of the corresponding transistors in Fig. 6(a). With a supplied voltage of 1-V and 0.25-μm 1P5M CMOS technology, the transfer curves and the $\mathrm{IRR}_{\mathrm{PPF4}}$ of a low-voltage four-stage polyphase filter are shown in Fig. 11. Fig. 11 shows that an $\mathrm{IRR}_{\mathrm{PPF4}}$ of -50 dB can be achieved within the frequency range 4.9 MHz $\sim$ 27 MHz. The simulated CMRR within this bandwidth is 40 dB. The 1-V polyphase filter consumes 5.5 mW, which is only about 50% of the power consumption in the 2.5-V version.

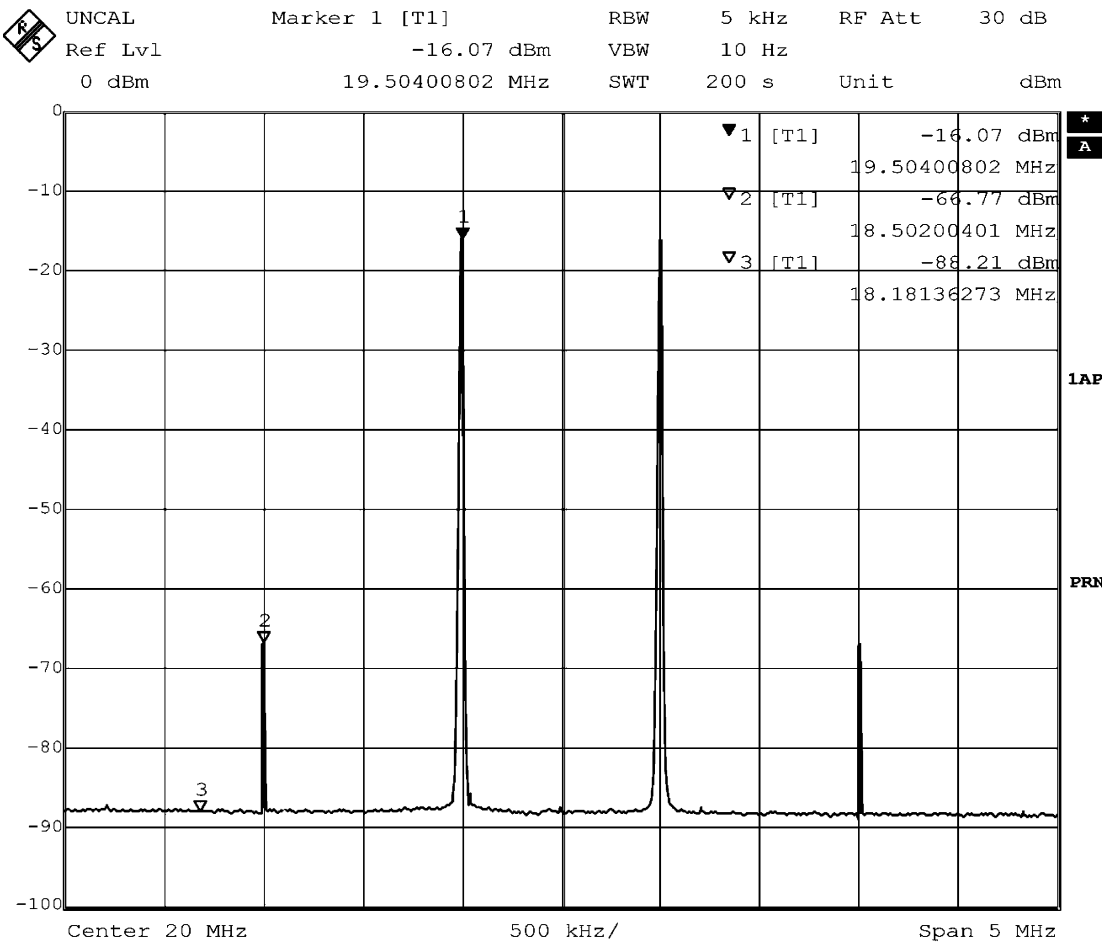

Fig. 14. Two-tone test for $f_1 = 19.5$ MHz and $f_2 = 20.5$ MHz.

IV. Experimental Results

Fig. 12 shows the die micrograph of a four-stage polyphase filter, which is designed and fabricated in 0.25-μm 1P5M CMOS technology. The four-stage polyphase filter consumes 11 mW at a supplied voltage of 2.5 V and occupies a die area of 1162×813 μm^2. All of the capacitors are implemented by metal-insulator-metal (MIM) capacitors.

For measurement purposes, on-chip test buffers are placed after the polyphase filter to analyze the output signals. In the measurement set-up, a splitter converts a single-ended signal into differential signals, which are then sent to a six-stage off-chip *RC* polyphase filter to generate the required input quadrature signals. The off-chip *RC* network can provide an IRR of more than -55 dB in the frequency range 4 MHz $\sim$ 35 MHz. After the gain loss of the off-chip *RC* network has been compensated for, the measured voltage gain of the fabricated four-stage polyphase filter at 20 MHz is 6.6 dB. The measured $\mathrm{IRR}_{\mathrm{PPF4}}$ is shown in Fig. 13, an IRR of -48 dB can be achieved in the frequency range 6.1 MHz $\sim$ 30 MHz. A two-tone test is performed to measure spurious-free dynamic range (SFDR). As shown in Fig. 14, when the input signals are at 19.5 and 20.5 MHz, the differences between noise floor to fundamental and third-order intermodulation signals are 72.2 and 21.5 dB, respectively. Thus, a 65 dB in-band SFDR can be achieved by the polyphase filter. Fig. 15 shows that the measured input third intercept point (IIP3) is 8 dBm. The measured CMRR is 41 dB and the input referred noise is 78.1 μV, which includes the noise contributed by output buffers.

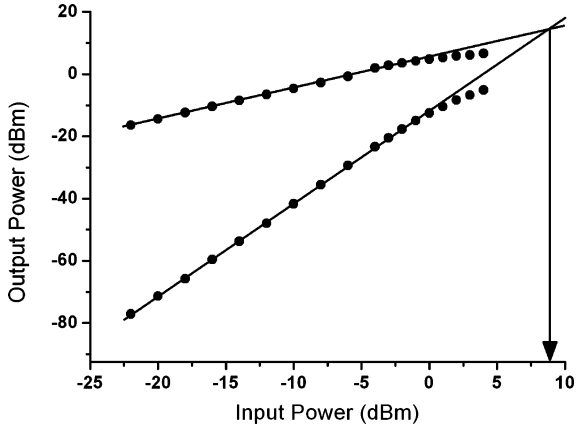

Fig. 15. Measured IIP3 of fabricated four-stage polyphase filter in 0.25-μm CMOS technology.

The performance comparison between the proposed polyphase filter and the passive *RC* polyphase filter [7] is given in Table II. As seen from Table II, the proposed polyphase filter has much lower average power dissipation per stage for the same power supply and higher passband gain while maintaining the same IRR per stage. In the passive *RC*

TABLE II
COMPARISON BETWEEN PROPOSED POLYPHASE FILTER AND PASSIVE *RC* POLYPHASE FILTER [7]

	This Work	[7]
CMOS Process	0.25 um	0.6 um
Number of stage	4	5
Power supply	2.5 V	3.3 V
Total power dissipation	11 mW	62.7 mW
Average power dissipation per stage for 2.5V	2.75 mW/stage	9.5 mW/stage
Bandwidth	23.9 MHz	16.5 MHz
Total image rejection ratio	-48 dB	-60 dB
Average image rejection ratio per stage	-12 dB/stage	-12 dB/stage
Passband gain	6.6 dB	-1 dB
In-band SFDR	65 dB	N/A
Input referred noise	78.1 uV	N/A

polyphase filter, large power is needed in interstage buffers. In the proposed four-stage polyphase filter, the power dissipation can be reduced further to 1.375 mW/stage at 1-V power supply.

V. CONCLUSION

A wide-band and low-power active polyphase filter has been proposed and analyzed. The wide-band performance is achieved by simple CMOS single-stage filter circuit and directly cascaded multistage structure. Without inter-stage buffer, the power dissipation is kept low. The simulations have shown that by biasing with a constant-gm circuit, the variations in process and temperature are effectively reduced. Due to the advantage of current-mode operation, the proposed active polyphase filter has been successfully modified to fit the operation of 1-V power supply. The performance of the filter has been verified through measurement on the fabricated chip in 0.25-μm 1P5M CMOS technology. The measured IRR of four-stage polyphase filter is higher than -48 dB over the frequency range of 6.1 MHz $\sim$ 30 MHz. The power consumption is 11 mW with 2.5-V power supply. It has been shown from measurement results that the proposed active polyphase filter is suitable in wireless communication applications.

ACKNOWLEDGMENT

The authors would like to thank the Chip Implementation Center (CIC), National Science Council, Taiwan. R.O.C., for the fabrication of the testing chip.

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