A Portable Digitally Controlled Oscillator Using Novel Varactors

Pao-Lung Chen, Ching-Che Chung, and Chen-Yi Lee

***Abstract*—This work presents a portable digitally controlled oscillator (DCO) by using two-input NOR gates as a digitally controlled varactor (DCV) in fine-tuning delay cell design. This novel varactor uses the gate capacitance difference of NOR gates under different digital control inputs to establish a DCV. Thus proposed DCO can improve delay resolution 256 times better than a single buffer design. This study also examines different types of NOR/NAND gates (2-input or 3-input) for DCV. The proposed DCO with novel DCV can be implemented with standard cells, and thus it can be ported to different processes in short time. Furthermore, the final circuit layout can be generated using an auto placement and routing (APR) tools. A test chip demonstrates that LSB resolution of the DCO can be improved to 1.55 ps with standard 0.35-μm 2P4M CMOS digital cell library. The proposed DCO has good performance in terms of fine resolution, high portability, and short design turnaround cycle compared with conventional DCO designs.**

***Index Terms*—All-digital phase-locked loop (ADPLL), cell-based hardware-description language, digitally controlled oscillator (DCO), digitally controlled varactor (DCV), PLL.**

I. Introduction

PHASE-LOCKED loops (PLLs) are widely used in many communication systems to clock and data recovery or frequency synthesis. Traditional analog circuit design such as PLL shifts the design paradigm toward more digitally intensive techniques, easier testability and less parameter variability because of process migration. A digitally controlled oscillator (DCO) based architecture for RF frequency synthesizer was reported in [1]. The *LC* tank DCO achieves very fine frequency resolution (23 kHz) by using advanced 0.13-μm CMOS process. The switchable capacitance of the finest pMOS varactor is 38 attofarads. However, this DCO suffers from one fundamental drawback. Due to the extremely small size of varactor, it requires intensive circuit layout and needs advanced lithography technology. A long design cycle will occur as product design transfers to different processes or the design specifications are changed. Thus, this work attempts to propose a high resolution DCO by using NOR/NAND gates as novel varactor.

Basically, two main techniques exist for designing a fine resolution in DCO. One technique changes the MOS driving strength dynamically using a fixed capacitance loading and achieves a fine resolution [2]. Meanwhile, the other uses the shunt capacitor technique to fine-tune the capacitance loadings and achieves high resolution [1], [3]. Fig. 1 shows the conventional control mechanism with the shunt capacitor circuit. In Fig. 1, M_C serves as a capacitor. The gate of transistor $M_{\rm ctrl}$ (that is, $D_{\rm ctrl}$) controls the discharge/charge current. Consequently, $D_{\rm ctrl}$ can control the delay resolution from In to Out.

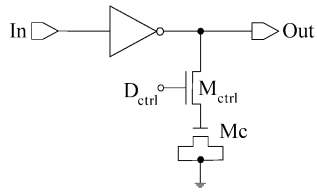

Fig. 1. Conventional digitally controlled mechanism with shunt capacitor.

A standard cell description of the DCO simplifies the design and can be easily ported to different processes. A simple DCO that directly uses an inverter ring is presented in [4], but has insufficient resolution for most applications. Another DCO example consists of a bank of tri-state inverter buffers [5]. The delay resolution in this case can be controlled by the number of enabled buffers. However, [5] has the disadvantages of large silicon area and high power consumption. Another means of fine resolution enhancement, implemented by an or-and-inverter (OAI) cell shunted with two tri-state inverters to enhance driving capability, was proposed in [6]. The proposed DCO in [6] has less area and power consumption than [5]. However, the resolution step of the proposed DCO is nonuniform and sensitive to power-supply variation because it uses OAI cell to change the delay resolution. Additionally, this technique also requires an additional decoder for mapping OAI cell control input.

The proposed DCO, like most voltage-controlled oscillators, employs a frequency control mechanism located inside an oscillator block. Two parameters are used to modulate the output frequency of a ring oscillator, namely the propagation delay time of each delay cell, and the total number of delay cells in the closed loop. Generally, delay time resolution is more difficult to achieve than total delay time, because the transistor width/length (W/L) is fixed in a cell-based design. To deal with this problem, we developed a novel DCV using NOR/NAND gate in the fine-tuning cell design of DCO. The proposed DCO improves delay resolution and demonstrates monotonic delay behavior with respect to digital control codes. The proposed technique has been successfully verified on a test chip fabricated in a 0.35-μm 2P4M CMOS process.

The remainder of this paper is organized as follows. Section II describes the proposed digitally controlled oscillator. Different types of digitally controlled varactors (DCVs) are also addressed

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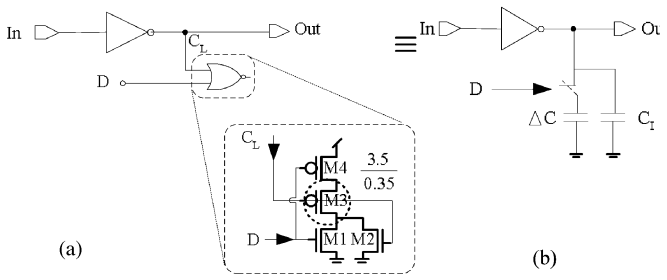

Fig. 2. Proposed DCV with two-input NOR gate. (a) Circuit with digital control. (b) Equivalent circuit with ΔC capacitance.

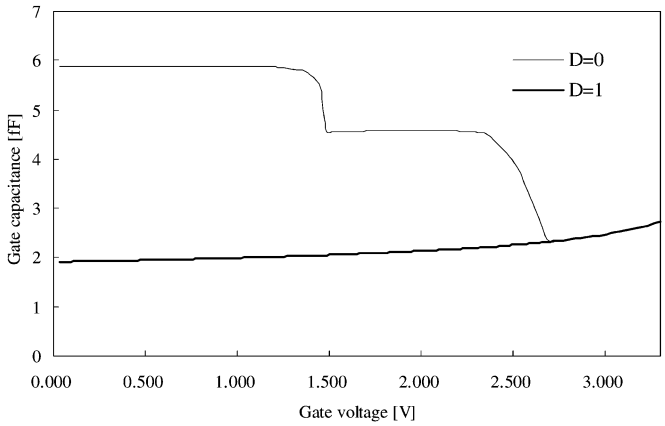

Fig. 3. Variation of two-input NOR gate's capacitance when $D = 0$ and $D = 1$.

in this section. Section III then describes the implementation and experimental results. Conclusions are finally made in Section IV.

II. Proposed Digitally Controlled Oscillator

A. Digitally Controlled Varactors

Fig. 2(a) illustrates a novel varactor cell using a two-input NOR gate. As described in [7], the gate-to-channel capacitance contributes to total gate capacitance. The proposed method controls the capacitance between gate and source or between gate and drain. In Fig. 2(a), the NOR gate capacitance at node C_L depends on control node D's value. The total gate capacitance of transistors M2 and M3 varies with D input states.

Fig. 2(b) shows the equivalent circuit of Fig. 2(a), an initial capacitance (C_I) parallels with a capacitance difference (ΔC). The D input controls the capacitance (ΔC) in the output (Out) node. Fig. 3 shows the gate capacitance difference characteristic which is simulated using the HSPICE circuit simulator. The swing-averaged capacitance $C_{\text{average}}(D)$, as D-node is in the 0 state or in the 1 state, is given by

$$C_{\text{average}}(D) = \frac{1}{Vdd}\int_0^{Vdd} C(V_{\text{gate}}, D)dV_{\text{gate}} \qquad (1)$$

where $C(V_{\text{gate}}, D)$ denotes the simulated gate capacitance shown in Fig. 3. Based on (1), ΔC denotes the capacitance difference between $C_{\text{average}}(0)$ and $C_{\text{average}}(1)$. Consequently, the variable delay (ΔT) of the proposed DCV in different D states can be calculated easily using the following linear equation:

$$\Delta T = K_{\text{load}} \times \Delta C \qquad (2)$$

where K_{load} denotes the delay factor of driving inverter. The K_{load} value of the driving inverter is 0.509 (ns/pF) in target 0.35-μm 2P4M CMOS cell library. The ΔC of Fig. 3 is estimated to be around 2.8 fF. Therefore, ΔT of 1.425 ps $(= 0.509{*}2.8)$ is easily obtained. If N NOR gates are attached to the C_L node, the max delay time variation becomes $N{*}\Delta T$. Moreover, different ΔT can be achieved as needed by changing the cell type of the driving inverter (i.e., change the K_{load}).

A NAND gate can also be applied to DCV design. Fig. 4 illustrates three different DCVs: (a) two-input NAND gate; (b) three-input NOR gate; (c) three-input NAND gate. For the three-input NOR and three-input NAND gate, an extra input pin is fixed to 1 and 0, respectively. The marked transistors (M5, M6, M7) produce a large capacitance difference under different D states.

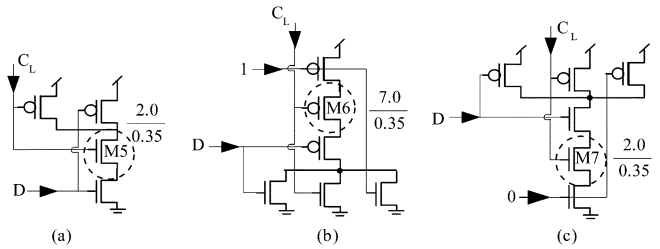

Fig. 4. Three different types of DCV cells. (a) Two-input NAND. (b) Three-input NOR. (c) Three-input NAND.

TABLE I
Comparisons Among Different Types of Proposed DCV Cells

Items \ Types	Two-input NOR	Two-input NAND	Three-input NOR	Three-input NAND
Transistors	4	4	6	6
Size of transistor (W/L) unit: μm	3.5 / 0.35	2.0 / 0.35	7.0 / 0.35	2.0 / 0.35
Delay resolution	1.43 ps	0.80 ps	3.2 ps	0.80 ps
Power consumption	15.5 μw/MHz	18.1 μw/MHz	14.5 μw/MHz	14.3 μw/MHz

Table I lists the comparisons among these DCVs. The three-input NAND/NOR gate varactor consumes less power than the 2-input NAND/NOR gate varactor, but it costs more area. Generally, the finer delay resolution can be obtained by decreasing MOS width of (M5, M6, M7).

B. Performance of the Digitally Controlled Varactors

HSPICE circuit simulation is performed for estimating the performance of different type fine-tuning delay cell including the proposed DCV, pass transistor [3], and OAI cell [6] on a standard 0.35-μm CMOS 2P4M process. In this simulation, a series of 97 inverters are used in the coarse-tuning stage of the ring oscillator, and the proposed DCV and serves as the fine-tuning delay cell. Totally, 32 DCVs are used in the fine-tuning delay cell $(N = 32)$. Fig. 5 shows the delay resolution of the fine-tuning stage and the proposed delay cell has finer resolution (about 1.43 ps) than other circuits [3], [6].

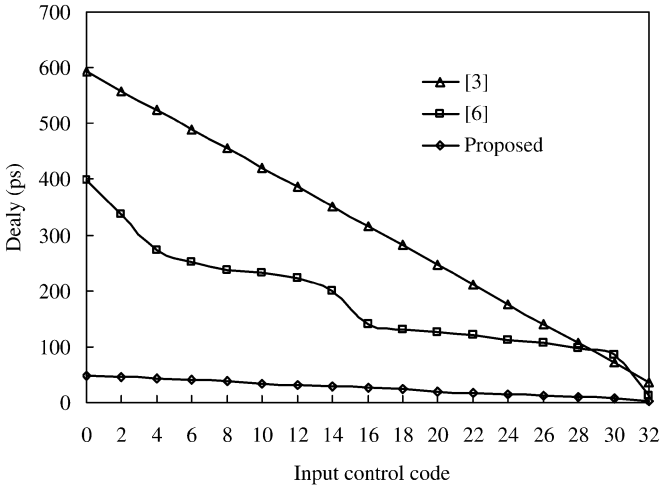

Fig. 5. Comparisons among the proposed DCV and other approaches.

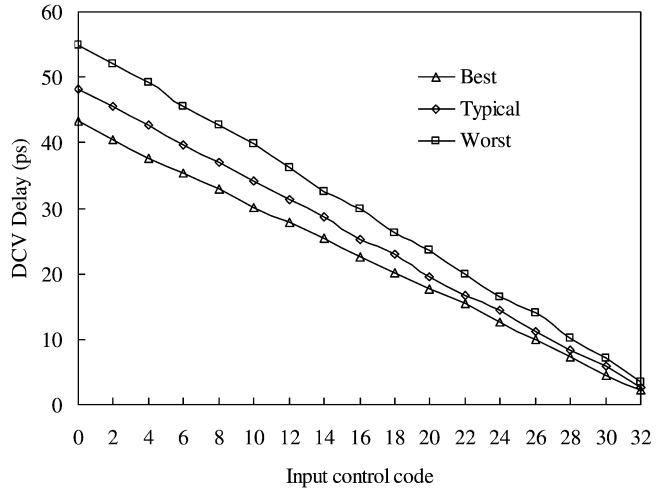

Fig. 6. Proposed DCV using two-input NOR under different PVT conditions.

The delay cell proposed by [3] has very good linearity but poor resolution and it also has large transistor counts. Oppositely, OAI cell [6] has less transistor counts and less power consumption, but it has nonuniform linearity. Fig. 6 shows the proposed DCV under different process, voltage, temperature (PVT) conditions: (Best: FF, 3.6 V, 0 °C), (Typical: TT, 3.3 V, 25 °C), and (Worst: SS, 3.0 V, 125 °C). The delay resolution of the proposed DCV ranges from 1.28 ps in the best case to 1.61 ps in the worst case. It demonstrates the effectiveness of the proposed DCV to overcome PVT variations.

C. Structure of the Proposed DCO

Fig. 7 illustrates the structure of the proposed cell-based DCO with 15 bits binary weighted control $(0000_{16} \sim 7FFF_{16})$. The proposed DCO structure is separated into two stages: the coarse-tuning stage and the fine-tuning stage. The higher seven bits of the control code are for coarse-tuning stage, and lower eight bits are for the fine-tuning stage. The coarse-tuning stage uses a 128-to-1 path selector for delay-chain selection. This selector is implemented by multistage tristate buffers to reduce the loading effects of coarse-tuning buffers. The coarse decoder of the DCO decodes the $7(=\log_2(128))$ bits control code into 128 control signals. This architecture has the advantage that operating frequency of DCO can be easily modified according to different specifications. The $T_{\rm PHL}+T_{\rm PLH}(=T_{\rm buffer})$ of one coarse delay cell is about 385 ps in target 0.35-μm 2P4M CMOS standard cell library.

To increase the frequency resolution of the DCO, the fine-tuning stage is divided into fine1 and fine2 stages which are added after the coarse-tuning stage. The fine1 stage consists of 32 DCVs with capacitance difference ΔC. 32 identical NOR gates with ΔC are used to build one $\Delta C2$ DCV. The total capacitance difference equals to 256 ΔC DCVs. The proposed NOR gate varactors for fine-tuning stage thus can improve delay resolution by 256 times compared to a simple buffer design.

The period of DCOs output signals equals

$$T_{\rm period}=T_{\rm coarse}+T_{\rm fine}+T_{\rm constant} \tag{3}$$

where $T_{\rm coarse}$ denotes the propagation delay time of coarse buffers, $T_{\rm fine}$ represents the fine-tuning delay time, and $T_{\rm constant}$ is the constant factor for delay time because of one extra NAND gate, a multistage tri-state buffer and the intrinsic delay caused by capacitance (C_I) of fine-tuning cells in the DCO ring. Equation (3) can be rewritten as follows:

$$T_{\rm period}=M\times T_{\rm buffer}+N_2\times\Delta T_2+N_1\times\Delta T_1+T_{\rm constant} \tag{4}$$

where M denotes the number of selected coarse buffers. N_1 and N_2 represent the number of turned on DCVs in fine1 and fine2 stages, respectively. Meanwhile, ΔT_1 and ΔT_2 are variable delay which can be calculated from (2). Therefore, (4) provides an easy method of calculating the timing period of DCO output.

III. Implementation and Experimental Results

A. Implementation Overview

The proposed DCO with novel DCVs is applied to all-digital PLL (ADPLL) design. The test chip is fabricated using a standard 0.35-μm 2P4M CMOS process. The designed DCO consists of two major functional blocks as illustrated in Fig. 7, namely the ring structure and decoder. Moreover, the decoder part is described by Verilog-HDL. The ring structure with DCVs is described at the gate level. A Verilog-HDL model of DCVs is first built from HSPICE simulation results for co-simulation with other digital blocks. Next, source codes are synthesized to gate-level netlists and schematics for further simulation and verifications. Once the functions have been correctly verified, an automatic placement and routing (APR) tool is used to complete the physical layout.

In APR process, the designed DCO must be grouped in a restricted region to minimize the induced capacitance and the ring structure of DCO had to be placed regularly rather than randomly. Furthermore, the post-layout simulation is performed to ensure the monotonic response of DCO and timing resolution. The APR process will be refined until the target specification is achieved.

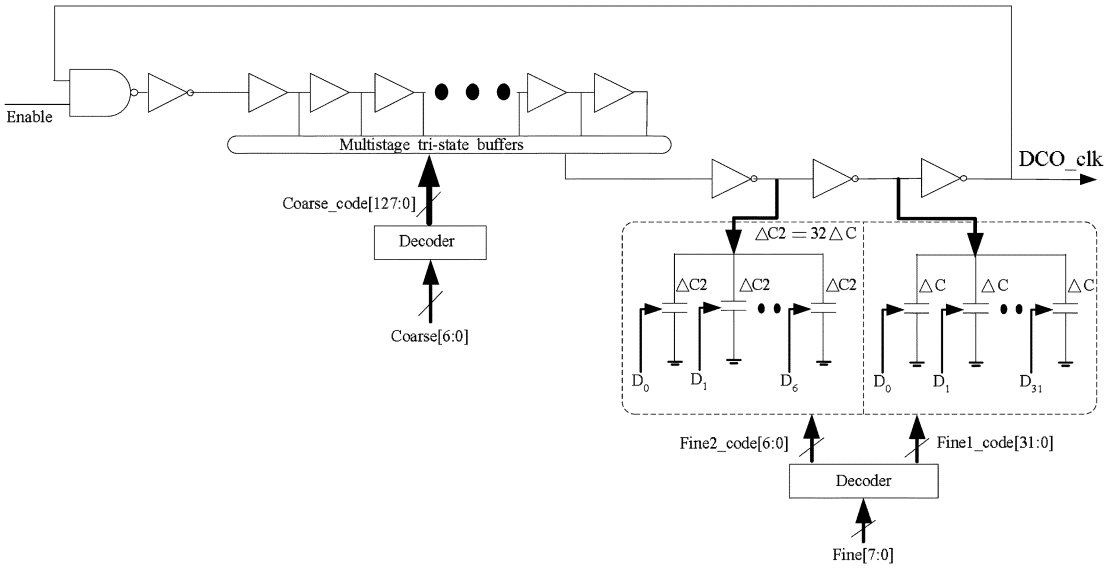

Fig. 7. Proposed digitally controlled oscillator with DCV in the fine-tuning stage.

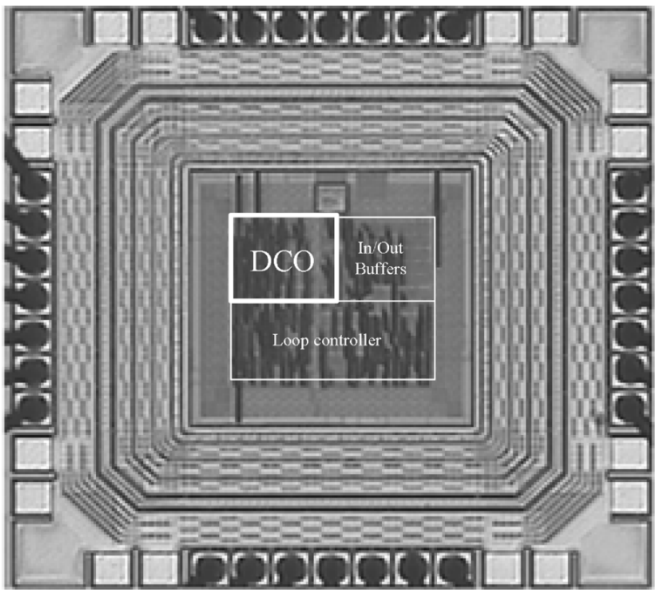

Fig. 8. Microphotograph of DCO test chip.

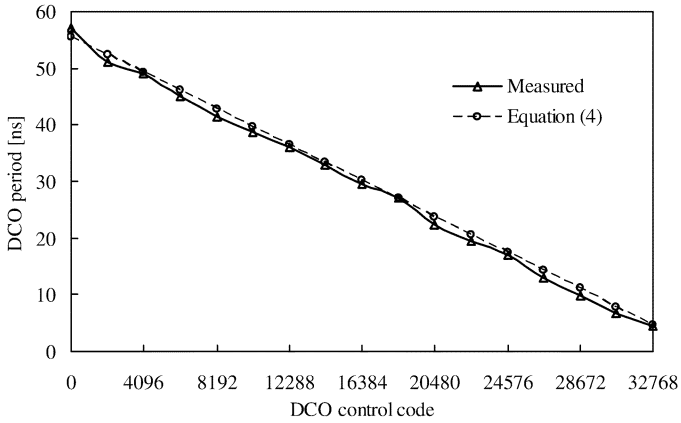

Fig. 9. Chip measured results compared to linear (4) under 3.3 V/25 °C.

B. Laboratory Test Result

Fig. 8 is a microphotograph of the ADPLL. The proposed DCO is located in the upper left corner of the test chip and occupies 0.04 mm^2 of chip area (i.e., 200 μm$\times$ 200 μm). This DCO has been measured for different settings. Initially, the DCO output frequency is directly measured using LeCory LC584A at 3.3 V/25 °C, and the measured results demonstrate that the operating frequency of the DCO ranges from 18 to 214 MHz (i.e., 55.555 ns to 4.673 ns). Moreover, the average step resolution is 1.55 ps. In Fig. 9, the measured results are compared to linear delay (4). Fig. 9 also reveals that linear delay (4) can be used to estimate DCO timing period.

Table II lists the chip measurement results compared with conventional approaches [3], [5], [6]. The proposed DCO with 15 bits control codes achieves the finest LSB resolution and best portability. Additionally, the proposed DCO also consumes less power as compared with [5] and [6].

TABLE II
COMPARISON WITH EXISTING DCOS

Items / Function	Proposed	ISQED'02 [3]	ISSCC'03 [5]	JSSC'03 [6]
Process	0.35 μm@3.3V	0.13 μm@1.65V	0.6 μm@5V	0.35 μm@3.3V
DCO control word length	15 bits	8 bits	10 bits	12 bits
LSB Resolution	1.55 ps	40 ps	10 ps	5 ps
DCO output frequency	18 ~ 214 (MHz)	150 (MHz)	10 ~ 12.5 (MHz)	45 ~ 450 (MHz)
Power consumption	18 mW @ 200 MHz	1 mW @ 150 MHz	164 mW @100 MHz	100 mW @ 450 MHz
Portability	Yes	No	Yes	Yes

IV. CONCLUSION

A portable digitally controlled oscillator using two-input NOR gates as digitally controlled varctors has been presented. Different configurations based on NOR/NAND gates have also been

investigated using HSPICE circuit simulator. The delay resolution of the proposed DCO can be determined using a simple linear equation. Test chip measurement results show the average delay resolution of the proposed DCO is 1.55 ps. Therefore, the proposed digitally controlled oscillator reduces the circuit complexity and also improves testability. Compared to conventional approaches, design time can also be reduced significantly by using Verilog hardware-description language and APR CAD tools. Furthermore, the proposed DCO is suitable for intellectual property (IP)-based design, and has an excellent probability of first-time silicon success.

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