THE FABRICATION AND THE CHARACTERISTICS OF METAL-OXIDE SEMICONDUCTOR TRANSISTORS

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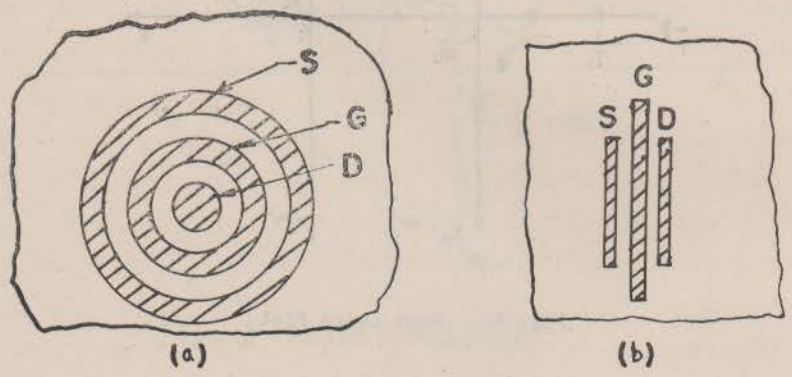
Abstract-The theory of MOS transistors is introduced in brief and the design and the fabrication of MOS transistors are discussed in detail. The experimental MOS transistor characteristics show the effects of the surface states and can be determined by the gate capacitance versus gate voltage characteristics by a specially designed automatic curve tracer.

I. INTRODUCTION

The idea of modulating the conduction current by the electric field in solid, was proposed early in 1940's. Shockley [1] gave a complete theoretieal analysis in 1952, but due to the lack of controllability and the stability of the semiconductor surface, not until recent years were the actual feasible devices fabricated by using the modern semiconductor fabrication technology. The method of fabrication is discussed in detail, especially the treatments of the oxide layer. Since the gate capacitance versus the gate voltage characteristics are very important in the determination of the surface states, here is introduced a convenient method which can display the C-V characteristics directly on the oscilloscope screen to replace the usual point-by-point measurements.

II. PHYSICAL STRUCTURES

The surface geometry of MOS transistors is generally in two forms,



circular and rectangular, as shown in Fig. 1(a) and (b), respectively.

Fig. 1. The MOS transistor structures (a) Circular, (b) Rectangular.

The cross sectional view of MOS transistors is shown in Fig. 2, using a P-type substrate as an example. The two N^+ islands are obtained by the

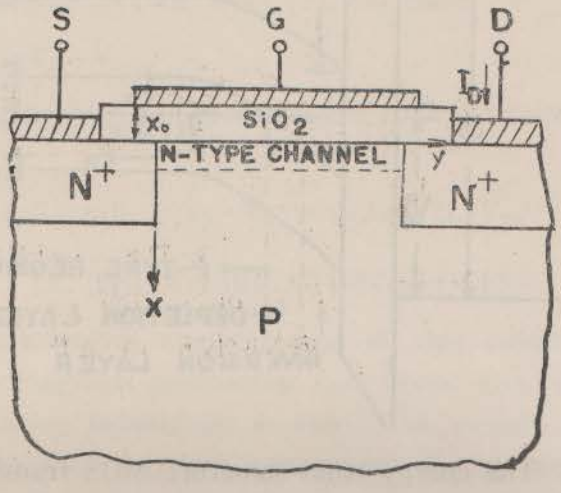


Fig. 2. The sectional view of an N-channel, p-type substrate MOS transistor, the coordinate system used is also shown in this figure.

seiective diffusion of phosphorus, a thin oxide layer of 1000Å to 8000Å is thermally grown on the semiconductor surface in dry oxygen or in de-ionized water vapor or in mixture of the two, and a metal film is obtained by evaporation of aluminium in high vacuum. The island labeled S is the input electrode, the source, the island labeled D is the output electrode, the drain, and the electrode labeled G is the control electrode, the gate. The "Three-Terminal Connections" is commonly used in device application, i. e., the source is connected directly to the substrate. Sometimes, the substrate may be connected as an independent electrode.

The energy band structure of the MOS transistors is showh in Fig. 3, which shows the band bending due to the surface states. The work function difference between the metal and the semiconductor is also indicated in tis figure. 3.

From this diagram, the semiconductor surface is inverted to N type due to the applied gate voltage, called the inversion layer. The layer next to the inversion layer is a layer of depleted charges, called the depletion

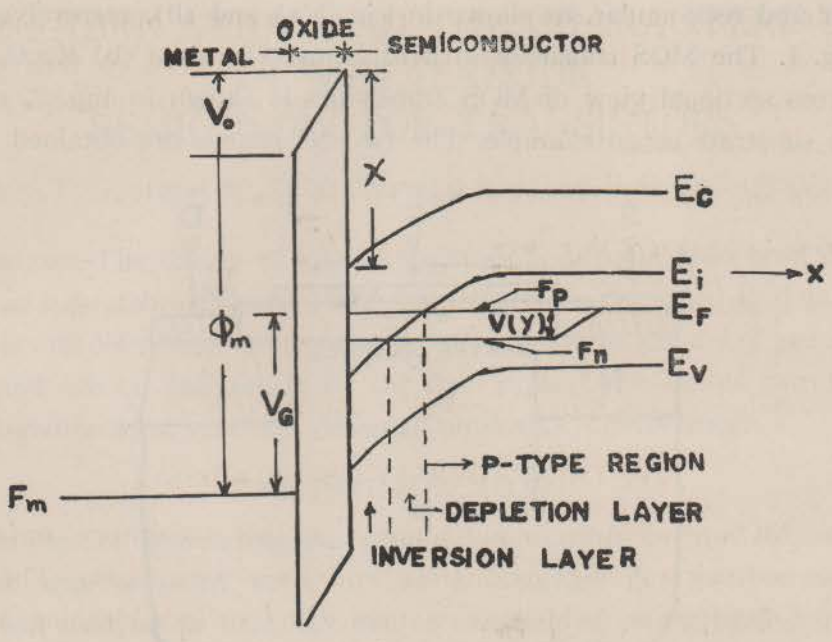


Fig. 3. The energy band structure MOS transistors.

layer. The region next to the depletion layer is p-type region, which is the semiconductor bulk.

III. THE CHARACTERISTIC THEORY

If the conducting channel of the MOS transistors is fairly uniform along its length, the electric field is almost perpendicular to the silicon-silicon dioxide interface. The surface states are also lumped into a fixed charge with total charge given by Q_{ss} per unit area of surface. By the two assumptions, Sah [2] derived an important drain charateristic equation:

$$I_D=(\bar{\mu}_n\ CoZ/L)\ (V_G-V_T)V_D-V_D{}^2/2 \tag{1}$$

where $\bar{\mu}_n$ is the effective mobility and is given by

$$\bar{\mu}_n=\int \mu_n n dx/\int n dx \tag{2}$$

Co is the oxide capacitance per unit area

V_T is the threshold voltage and is defined as

$$V_T=-(Q_{ss}+Q_B)/Co \tag{3}$$

where Q_B is the charge qer unit area in the bulk.

Physically, if $Q_{ss}+Q_B<0$, V_T is the minimun gate voltage to turn on

the drain current and corresponds to the enhancement mode of operation. If $Q_{ss}+Q_s>0$, V_T is the minimun gate voltage required to turn off the drain current and this is the case for P-type substrate which exists an N-channel even when $V_G=0$.

At saturation, $(\partial I_D/\partial V_D)V_G=0$, from (1), one have

$$V_D=V_{DS}=V_D-V_T \tag{4}$$

This is also the pinch-off condition, the drain current at this condition is given by

$$I_D=I_{DS}=(\bar{\mu}_n Coz/2L)\ (V_G-V_T)^2=(\bar{\mu}_n Coz/2L)V_{DS}^2 \tag{5}$$

IV. THE FABRICATION PROCESS

The MOS transistors manufactured at this laboratory have both circular and rectangular geometries and have two sizes. The usual transistor fabrication technology is used. The surface cleaning and the oxidation are the two important procedures in the fabrication of MOS transistors, a good surface cleaning can reduce the surface states to minimun and very pure chemicals must be used during the oxidation process to reduce the impurities in the oxidation layer. The process is listed in Table I using p-type substrate, N-channel transistors as an example the mask used are shown in Fig. 4.

Table I. MOS transistor fabrication process.

Step	Operation	Instruction	Step	Operation	Insttuction
1	Cleaning		15	Cleaning	
2	Oxidation	1050°C,45′	16	Oxidation	1000°C,3hrs, O_2
3	Baking	1050°C,45′	17	Baking	900°C,10′
4	KPR(1)		18	KPR(3)	
5	Baking	135°C,45′	19	Baking	135°C,45′
6	Etching		20	Etching	
7	Cleaning		21	Cleaning	
8	Phosphorus Diffusion		22	Evaporation	
9	Cleaning		23	KPR(4)	
10	Oxidation	1050°C,45′	24	Etching	

11	Baking	900°C,10′	25	Cleaning	
12	KPR(2)		26	Sintering	
13	Baking		27	Probing	
14	Etching				

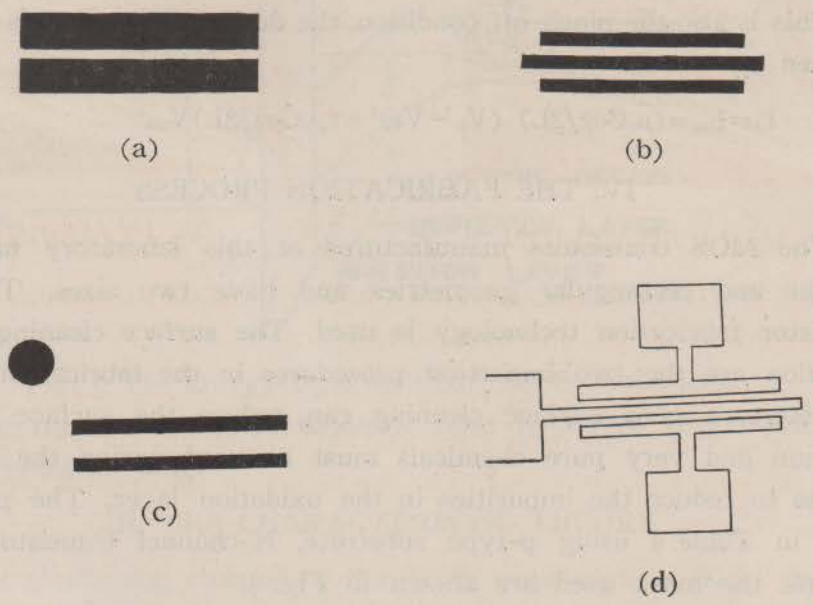


Fig. 4. The masks used in fabrication.

V. EXPERIMENTAL RESULTS

As an illustrating example, we use an N-channel MOS transistor with rectangular structure, channel length $L=40\mu$, an channel width $Z=550\mu$, the effective gate area is $A_G=ZL=2.2\times10^4\mu^2$. The oxide thickness is 1300Å, the measured oxide capacitance is $Co=4.14$pF, or 1.88×10^4pF/cm^2.

The drain characteristics are shown in Fig. 5. These curves were obtained from a Tektronix 575 Transistor Curve Tracer by connecting the source to E terminal, the gate to B terminal and the drain to C terminal and connecting a resistor of 100 KΩ across the B and the E terminals to convert the step currents generated from the step generator into the step voltages.

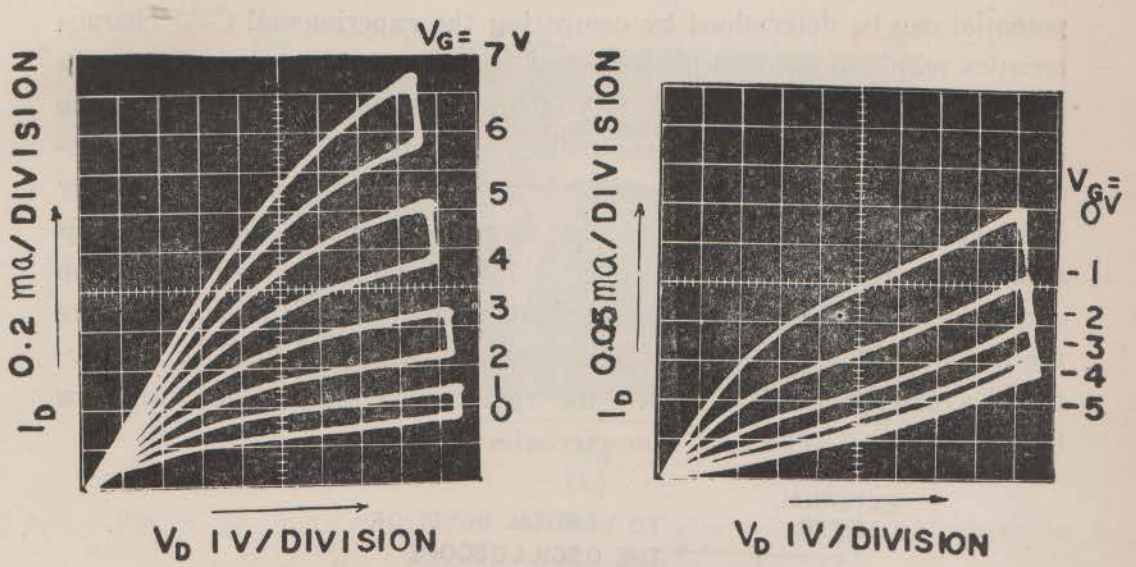


Fig. 5. The drain characteristics of an N-channel transistor
(a) Forward bias, (b) Reverse bias.

In Fig. 5(a), the lowest curve is the drain characteristic with zero gate voltae, this is the depletion mode since the drain current exists even when the gate voltage is zero. The drain current saturates when the gate voltage is large since the electrons in the channel suffer more surface scattering when the channel current is large and the electron mobility decreases. The mobility also decreases when the channel is heated due to large drain current

There is still increasing drain current after pinch-off since the gradual channel approximation is not valid if the channel length is not very long to compare with the channel thickness and the leakage current also increases when the drain voltage is large.

In Fig. 5 (b), one sees that the drain current exists even when the gate voltage is negative, this is the reason that an N-channel MOS transistor can operate without bias. The turn-off voltage of the transistor, from the figure, is about 6.5 volts.

The characteristics of the gate capacitance versus the applied gate voltage are discussed here since they contain important information about the surface states which reside in the oxide layer and the oxidesemiconductor interface, the distribution of surface states versus the surface

potential can be determined by comparing the experimental C-∇ characteristics with the theoretical calculated curves [3]. Here is introduced a method which can display the C-V characteristics automatically on the oscilloscope screen to instead the tedious point-by-point balancing procedures. This method is more convenient than the method proposed by Zaininger [4]. The schematic circuit diagram is shown in Fig. 7. This makes use of a Boonton Electronics 75D Gapacitance Bridge and an oscilloscope. Let the bridge be in LINEAR mode of operation and calibrate the output with the internal standard capacitance, then the C-V characteristics can be displayed with the required voltage range with slow horizontal sweep. The C-V characteristics

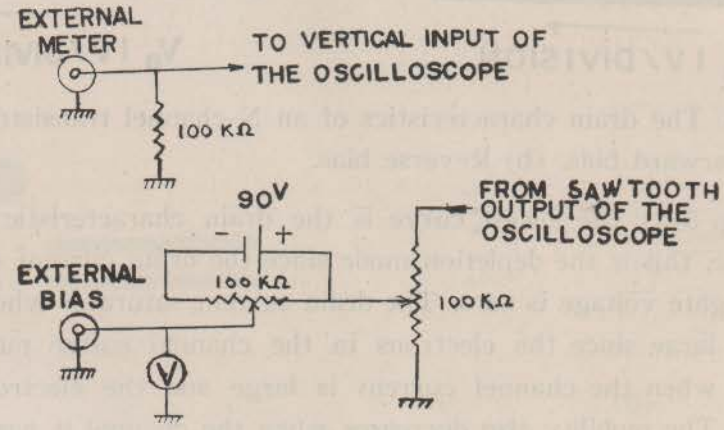
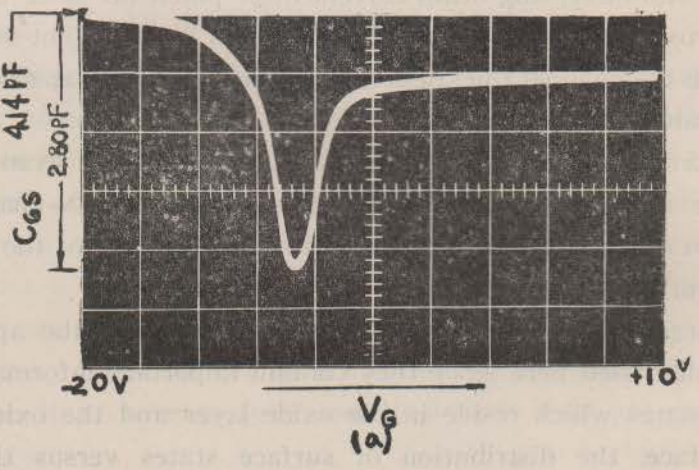


Fig. 7. The automatic capacitance versus voltage characteristic curve tracer.



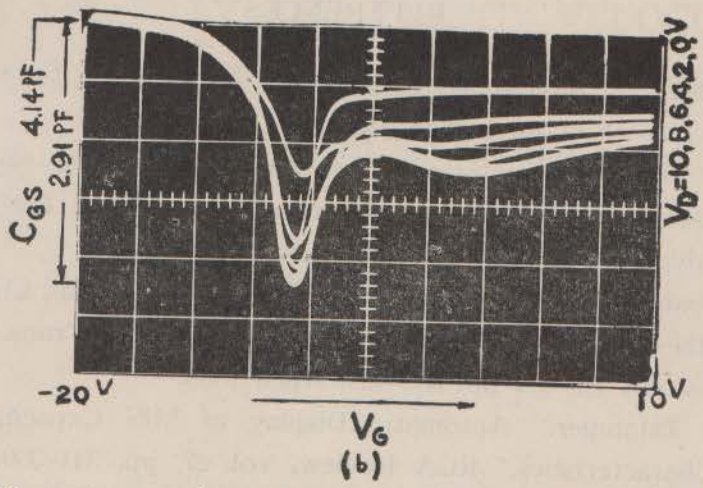


Fig. 8. The gate capacitance versus the gate voltage at (a) zero drain voltage, (b) Different drain voltage.

obtained are shown in Fig. 8(a) and (b), the channel acceptor concentration can be calculated from the capacitance difference $\triangle C$ in Fig. 8(a), this curve is shifted to the left of the ideal C-V curve because of the voltage contributed by the surface states. Fig. 8(b) shows the effects of the different drain voltages, the capacitance decreases when the drain voltage increases at large gate bias region.

VI. CONCLUSION

The approximate analysis of MOS transistor can be modified by taking the fixed bulk charge and surface states which actually depend upon the applied gate voltage into consideration. This can be solved by the study of the gate capacitance versus the gate voltage characteristics which give the actual surface state distribution with recpect to the surface potential.

VII. ACKNOWLEDGMENT

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