Zinc Dopping Effects On MOS Structure

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1. Introduction:

It has been investigated that gold dopping into bulk of silicon can be used to controlling MOS transistor characteristics [1]. However. zinc dopping into silicon, silicon dioxide as well as silicon dioxide-silicon interface has not yet been investigated.

First of all, it was indicated by Carlson and Tyler et al [2,3] that there are multi-zinc acceptor levels in silicon, one is located at 0.55 ev from bottom of conduction band and the others are located at 0.126 ev, 0.092 ev, 0.078 ev, and 0.31 ev from top of valance band respectively as is shown in Fig. 1.

(1). $N<10^{16}cm^{-3}$

n type 0.31 eV (A)

p type 0.55 eV (A)
0.31 eV (A)

(2). $N>10^{16}cm^{-3}$

Boron doped 0.126 eV (A)
0.092 eV (A)

Al doped 0.078 eV (A)

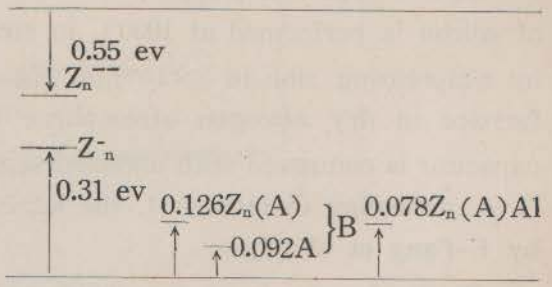

Fig. 1 Zinc levels in silicon

Obviously the recombination process will be dominanted by 0.55 eV level whereas carrier generation machanism will be dominanted by 0.078 eV level and 0.126 eV level. A very interesting result is obtained due to Z_n^{--} level as a S_i-S_iO_2 interace state which will shift the C-V curve of silicon MOS Structure. That is a very powerful method to controlling MOS transistor characteristics as well.

It will be further indicated here that 0.126 eV acceptor level and 0.078 eV acceptor level will affect the carrier concentration in the bulk of silicon.

However, due to this mult-lvel process, the machanism will be very complicated, therefore, the isolation of these machanism for the study of zinc effect on MOS structure has been devoted.

Z_n diffusion in silicon dioxide is interstitial type [5] therefore, low temperature diffusion process through S_iO_2 is applied in order to preventing from diffusion into the bulk of silicon.

The next step is rising the temperature and then investigation of zinc dopping effect on carrier concentration is obtained dy means of measuring MOST channal conductance [6] which will be compared with the interface state effect obtained formerly.

Further study on segregation coefficient is also in progress.

This report is a brief introduction of our research work on this problem.

2. Experimental results and discussion.

Both n type and p type wafer with ⟨lll⟩ direction are tested. oxidation of silicon is performed at 1000°C in steam vapor. zinc doping is obtained by evaporating zinc in 2×10^{-6}mm Hg vacuum and then put in drive-in furnace in dry nitrogen atmosphere for 30 minutes. zinc doped MOS capacitor is compared with undoped sample with the same drive-in process (i. e. annealing in nitrogen). the annealing effect has been investigated by F-Fang et al [7].

Obviously, zinc is an acceptor levyel, therefore the shift of C-V curve is toward the right. as shown in Fig. 3 and Fig. 4 for n type wafer and p type wafer respectively.

References

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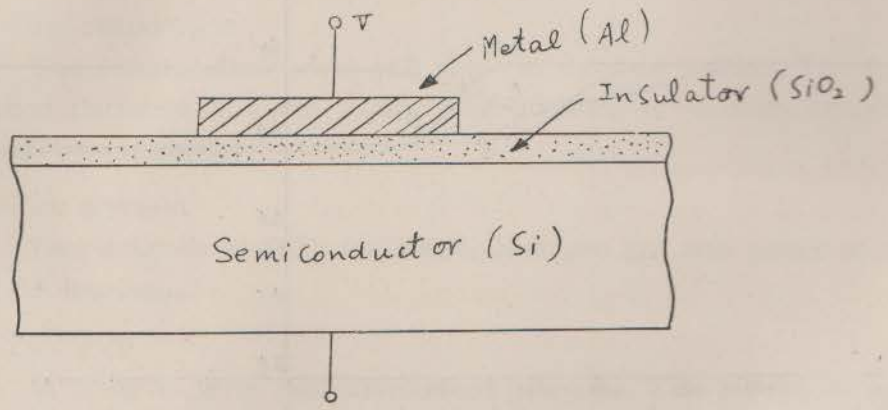

Fig 2. MOS structure

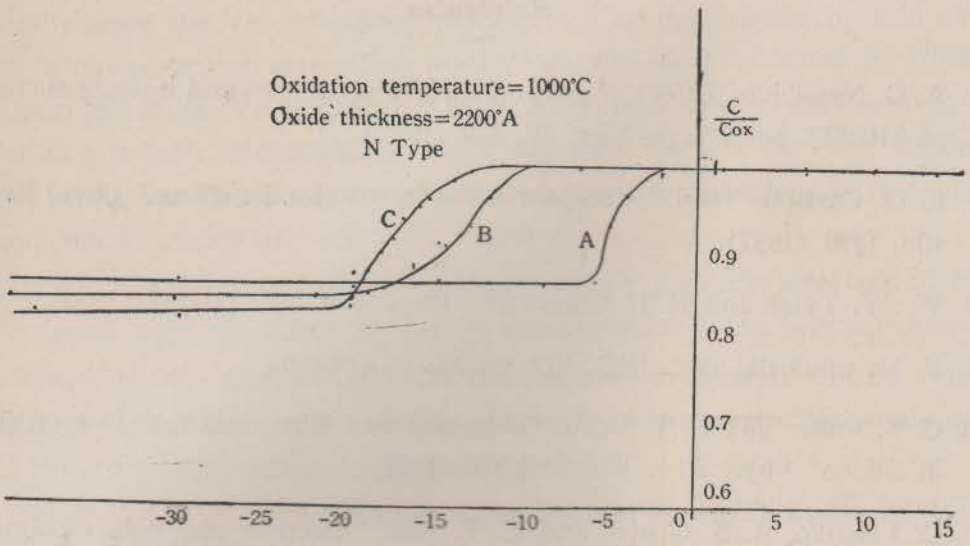

Fig. 3 Curve A Zinc doping (800°C, 30 min in N_2)
Curve B (heat treatment in N_2 800°C 30 min)
Curve C After Oxidation

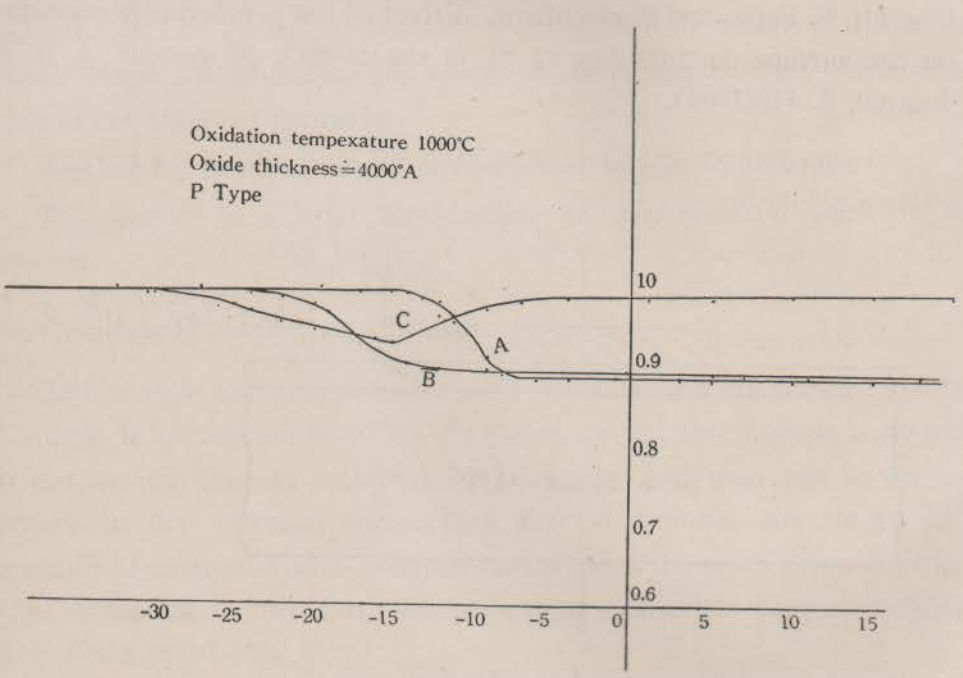

Fig. 4 Curve A Zinc doping (800°C 30 min in N_2)
Curve B (heat treatment in N_2 800°C 30 min)
Curve C (afteroxidation)

Appendix

Experimental set up

The materials used for making MOS structure were p type (3×10^{16}) and n type (5×10^{16}) silicon. Both are (III) orientation.

a. Procedure:

1. Cleaning

The wafers were cleaned by trichloroethylene, rinsed with distilled water, ultrasonic ally cleaned in acetone, followed by etching with a solution composed of distilled water 30cc, HF 10cc, and Ammonium Fluoride 20g. then qurther rinseag with distilled water, and was immersed ten min. in nitric acid, quenched the wafers in distilled water. Fianlly the wafers were dreied on bibulus paper.

2. Oxidation

The wafers were thermally oxidized at 1000°c, 17 min. wet O_2, How oxide thickness is 2200 Å.

3. Baking

Baking tempcrature is 1000°c, time 10 min. nitrogen gas Hows at a rate of 1 liter/min.

4. Zinc evaporation

The detailed description will show in the next section. The evaporation thickness is about 1000Å. The pressure of vacuum chamber is 5×10^{-5} torr(mmHg).

5. Zinc drive-in

Zinc drive-in at 800°c for 30min. Nitrogen gas was passed at a rate of 0.5 liter/min.

6. Zinc etch

In order to form a predetermined gate area, Zinc on the surface of the wafers were removed by a solution composed of Acetic acid 15cc, Nitric acid 3cc, and phosphoric acid 75cc, distilled water 14cc.

7. Aluminum evaporation

Use aluminum for the contact.

8. KPR

For dividing the aluminum film into small areas. (Use planar transistor emitter mask).

9. Ramove KPR

10. Dissolving the oxide layer on the back surface of silicon wafers. (Use dilute HF solution).

11. Zinc evaporation

During the evaporation of Zinc, the following difficulties are encountered· If Zinc is in powder form, it will jump out during the preliminary heating. The cause of jumping, partly due to the eddy current (A. C. source), partly due to the volatility of Zinc. In additian' Zinc films will not condense on non-metallic surfaces unless the vapour intensity is very high or the substrate temperature is very low. To conquer these difficulties we use tungsten net on the top of the titanium boat to prevent from the ejected power; aboue the tungsten net, tantalum sheet is puton the tungsten net learing a small window to pass the Zinc vapour. This will increase the vapour intensity. The cross-section view is shown Fig. 4.