A 15-b 40-MS/s CMOS Pipelined Analog-to-Digital Converter With Digital Background Calibration

Hung-Chih Liu, *Member, IEEE*, Zwei-Mei Lee, *Student Member, IEEE*, and Jieh-Tsorng Wu, *Member, IEEE*

***Abstract*—This study presents a 15-b 40-MS/s switched-capacitor CMOS pipelined analog-to-digital converter (ADC). High resolution is achieved by using a correlation-based background calibration technique that can continuously monitor the transfer characteristics of the critical pipeline stages and correct the digital output codes accordingly. The calibration can correct errors associated with capacitor mismatches and finite opamp gains. The ADC was fabricated using a 0.25-μm 1P5M CMOS technology. Operating at a 40-MS/s sampling rate, the ADC attains a maximum signal-to-noise-plus-distortion ratio of 73.5 dB and a maximum spurious-free-dynamic-range of 93.3 dB. The chip occupies an area of 3.8×3.6 mm^2, and the power consumption is 370 mW with a single 2.5-V supply.**

***Index Terms*—Analog–digital conversion, calibration, mixed analog–digital integrated circuits.**

I. Introduction

PIPELINED analog-to-digital converters (ADCs) are widely used in applications such as video imaging systems, broadband communication transceivers, and instrumentation. The subranging architecture offers a good tradeoff among power, sampling rate, and chip area for Nyquist-rate analog-to-digital (A/D) conversion.

In CMOS technologies, a pipeline stage for A/D conversion generally consists of a set of voltage-mode comparators and a switched-capacitor (SC) multiplying digital-to-analog converter (MDAC). The MDAC combines the functions of a sample-and-hold, a digital-to-analog (D/A) converter, a subtracter, and a voltage-mode amplifier [1], [2]. An SC MDAC employs an opamp with a capacitor feedback network to provide linear voltage amplification. As is well known, the dc offsets in the opamps and the comparators do not affect the overall linearity of a pipelined ADC if redundancy design and proper output encoding are adopted. The overall A/D linearity is mainly determined by the accuracy of the MDAC's conversion gain and the linearity of its D/A function.

The D/A linearity of an SC MDAC is determined by the capacitor ratio, while its gain factor is determined by both the capacitor ratio and the opamp's dc gain. Accuracy of the capacitor ratios is restricted for a given technology. Self-calibration schemes exist that can alleviate this limitation. Although the calibration can be accomplished in the analog domain [3], fully digital approaches are preferred in deep submicrometer technologies owing to the lower cost of the added digital circuitry [2], [4]–[9].

Conventional self-calibration schemes need reconfiguration of the pipeline stages, which inevitably disrupt the normal A/D operation. Thus, in applications that cannot afford idle time, the ADC's can only be calibrated in the power-on state. This power-on calibration may become insufficient for high-resolution ADCs, whose accuracy requirement for the MDACs cannot tolerate significant variation in opamp's dc gain. Furthermore, the opamp's dc gain is hard to maintain against supply-voltage and temperature variation.

To diminish this deficiency, several background calibration schemes have been developed to enable ADCs to continuously calibrate their internal pipeline stages to track environmental changes while simultaneously performing the normal A/D conversions. A good summary exists of the previous efforts [10]. In recent years, the correlation-based background calibration techniques have attracted attention since most of the calibration procedures can be undertaken in the digital domain. To calibrate a pipeline stage, most correlation-based schemes involve introducing a known random term into the stage, and then measuring the stage's transfer characteristic by extracting the random term from the ADC digital output. The schemes differ in: 1) how the problem is formulated; 2) how the random term is introduced; and 3) how the errors are corrected. Some schemes require an extra low-speed high-resolution ADC to determine the magnitude of the injected signal [11], [12]. The gain error correction plus the DAC noise cancellation (GEC+DNC) technique can only be applied to multibit pipeline stages [13]–[16], and it also doubles the required opamp's output range. A random signal can also be injected into the pipeline stage by randomly switching the thresholds of the stage's internal comparators [10]. However, the scheme also requires the input to often appear near the thresholds of the comparators. Another technique also involves switching the thresholds, but also switches the D/A configurations [17]. Both the conversion gain and nonlinear terms of the transfer characteristic of a pipeline stage can be statistically extracted from code distances at the same input location between two randomly switching circuit configurations. However, to collect sufficient information, the scheme requires that the input appears often in certain locations. The original design also cannot correct D/A nonlinearity [17].

The ADC described in this study employs a robust correlation-based background calibration scheme to correct the static A/D conversion errors [18], [19]. Random analog signals are sequentially injected into the critical pipeline stages through the

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The authors are with the Department of Electronics Engineering, National Chiao-Tung University, Hsin-Chu, Taiwan, R.O.C. (e-mail: jtwu@mail.nctu.edu.tw).

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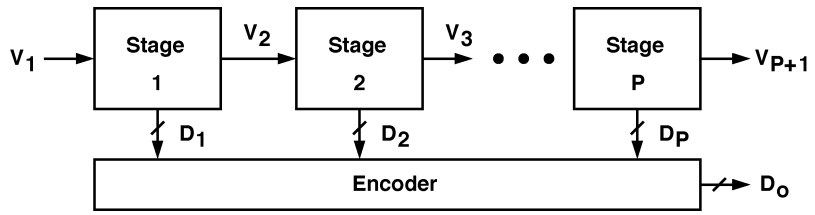

Fig. 1. Pipelined ADC.

split capacitors for measuring the stages's transfer characteristics. All static errors due to component mismatches and finite opamp gains are corrected in the digital domain. This calibration scheme requires only slight modifications to the standard pipeline stages. No additional high-resolution ADC is needed. For the critical analog signal path, no extra capacitive loading is added, thus its operating speed is not degraded. This calibration scheme is also robust since its effectiveness does not rely on the input's amplitude distribution. The measurement results of this 15-b 40-MS/s ADC chip fabricated in a 0.25-μm CMOS technology demonstrate the feasibility of this calibration scheme.

The rest of this paper is organized as follows. Section II gives a brief overview of the pipelined A/D architecture. Section III reviews the theory of digital self-calibration. Section IV introduces the proposed background calibration scheme. Section V describes the design of the ADC prototype. Section VI presents the experimental results of this ADC prototype. Finally, Section VII draws conclusions.

II. Overview of Pipelined ADCs

Fig. 1 shows the general form of a pipelined ADC. Although each pipeline stage can be different, it has a basic configuration shown in Fig. 2. At the jth stage, the analog input V_j is quantized with a sub-ADC. The resultant digital code D_j represents an estimate of V_j and is fed to a sub-DAC to generate a corresponding analog signal $V_j^{\rm da}(D_j)$. The output V_{j+1} can then be expressed as

$$V_{j+1} = G_j \times \left[V_j - V_j^{\rm da}(D_j)\right]. \tag{1}$$

In the above equation, V_{j+1} is the residue of the jth-stage A/D conversion amplified by a factor of G_j. By applying (1) recursively, the input of the entire pipelined ADC can be expressed as

$$V_1 = V_1^{\rm da} + \frac{V_2^{\rm da}}{G_1} + \frac{V_3^{\rm da}}{G_1 G_2} + \cdots + \frac{V_P^{\rm da}}{G_1 G_2 \cdots G_{P-1}} + Q \tag{2}$$

where $Q = V_{P+1}/(G_1 G_2 \ldots G_P)$ represents the quantization error of the entire A/D conversion. The ADC's digital output D_o is calculated from D_j, for $j = 1, \cdots, P$, by applying (2) and letting $D_o = V_1 - Q$. Both $V_j^{\rm da}$ and G_j, for $j = 1, \cdots, P$, are design parameters. Furthermore, the sub-ADC's conversion characteristics are well known to have no influence on D_o as long as the redundancy design for the pipeline stages can keep V_{j+1}, for all j, within the designed ranges.

Fig. 3 shows a radix-2 1.5-b switched-capacitor pipeline stage. The corresponding conversion characteristic is shown in Fig. 4. The sub-ADC is composed of two comparators with thresholds at $+0.25V_r$ and $-0.25V_r$, respectively. The opamp

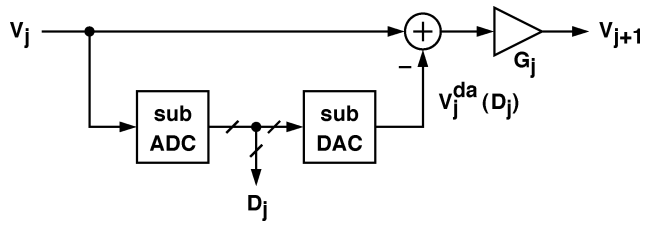

Fig. 2. Block diagram of a pipeline stage.

and the two capacitors, C_f and C_s, form a multiplying digital-to-analog (D/A) converter, which performs the functions of sample-and-hold, D/A conversion, subtraction, and voltage amplification. When clock ϕ_1 is high, V_j is sampled onto capacitor C_f and C_s. The digital code, $D_j \in \{-1, 0, +1\}$, is obtained by comparing V_j with $+0.25V_r$ and $-0.25V_r$. When clock ϕ_2 is high, the output V_{j+1} can be written as

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\rm da}(D_j) - V_j^{\rm os}\right] \tag{3}$$

with

$$\hat{G}_j = \frac{C_s + C_f}{C_f} \times \frac{1}{1 + \frac{1}{A_0} \cdot \frac{C_s + C_f + C_p}{C_f}} \tag{4}$$

$$\hat{V}_j^{\rm da}(D_j) = V_r \cdot \frac{C_s}{C_s + C_f} \times D_j \tag{5}$$

where C_p denotes the parasitic capacitance associated with the opamp's negative input. The realized jth stage gain factor $\hat{G}_j$ is a function of capacitor ratios and the opamp's dc gain A_0. The $V_j^{\rm os}$ term accounts for the offset effect of the jth stage, including the opamp's input-referred offset voltage and charge injection from analog switches. Letting $A_0 = \infty$ and $C_s = C_f$, an ideal transfer characteristic is obtained with $G_j = 2$ and $V_j^{\rm da}(D_j) = 0.5V_r \times D_j$.

III. Theory of Digital Calibration

With pipeline stages' behavior governed by (3) rather than (1), for $j = 1, \cdots, P$, the overall A/D characteristic also deviates from the ideal one if (2) is still employed to compute the ADC's output code. It can be shown that the offset terms $V_j^{\rm os}$, for $j = 1, \cdots, P$, contribute only to the overall A/D offset. Conversely, nonlinear A/D conversion occurs if $\hat{G}_j \neq G_j$ and $\hat{V}_j^{\rm da}(D_j) \neq V_j^{\rm da}(D_j)$. To achieve high resolution, values of both $\hat{G}_j$ and $\hat{V}_j^{\rm da}(D_j)$ must be obtained to replace G_j and $V_j^{\rm da}(D_j)$ in (2).

Normally, in pipelined ADCs, a z-ADC is employed to calibrate $\hat{G}_j$ and $\hat{V}_j^{\rm da}(D_j)$ of the jth pipeline stage as demonstrated in Fig. 5, with z-ADC being the backend stages comprising of the $(j+1)^{\rm th}$, $(j+2)^{\rm th}$, ..., and Pth pipeline stages. The z-ADC

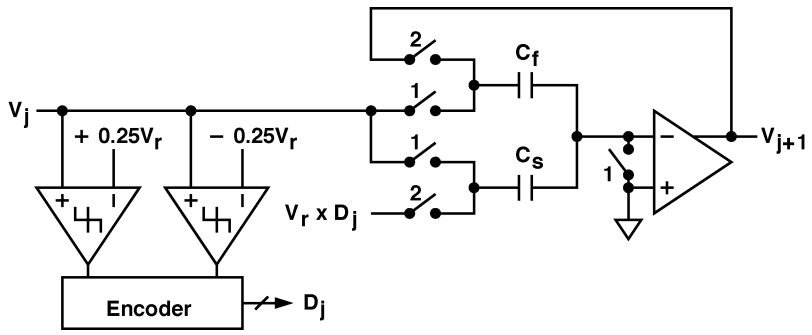

Fig. 3. Radix-2 1.5-b SC pipeline stage.

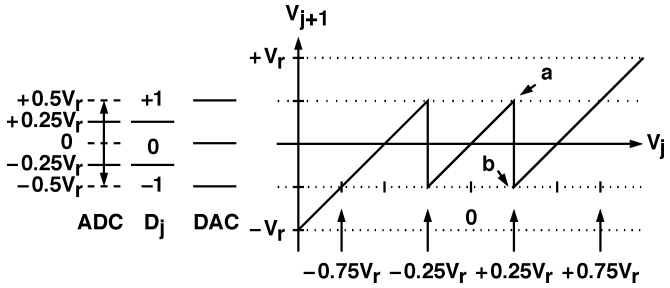

Fig. 4. Conversion characteristic of the SC pipeline stage in Fig. 3.

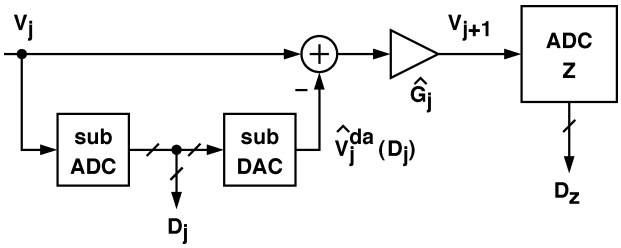

Fig. 5. Digital calibration of the jth pipeline stage.

quantizes the output of the jth stage, V_{j+1}, and generates a corresponding digital code D_z. If the z-ADC has a linear transfer characteristic, then V_{j+1} can be denoted as

$$V_{j+1} = \frac{G_z}{\hat{G}_z} \cdot D_z + O_z + Q_z. \tag{6}$$

This A/D conversion has a gain error of $G_z/\hat{G}_z$, an offset of Q_z, and a quantization error of Q_z. Here, G_z represents the specified gain factor and $\hat{G}_z$ is the realized gain factor.

To calibrate the jth stage, the height of every vertical transition in the V_{j+1} versus V_j transfer curve of Fig. 6 is measured and quantized by the z-ADC. The procedures include setting the jth stage's input, V_j and its sub-DAC output, $\hat{V}_j^{\rm da}(D_c)$. The V_{j+1} values at points a, b, c, and d are measured separately [4], [6]–[9]. The measured digital data are then manipulated to obtain $D_z(D_c)$, which in turn represents $R_j(D_c)$ as

$$R_j(D_c) = \hat{G}_j \times \hat{V}_j^{\rm da}(D_c) = \frac{G_z}{\hat{G}_z} \cdot D_z(D_c). \tag{7}$$

The transition height in Fig. 6 is the step size of $R_j(D_c)$ when the digital code D_c is changed by 1. Notably, the offset terms, $V_j^{\rm os}$ in (3) and Q_z in (6), can be removed during computation of $D_z(D_c)$. The quantization error term, Q_z in (6), is ignored in (7), since it is of no consequence in the background calibration

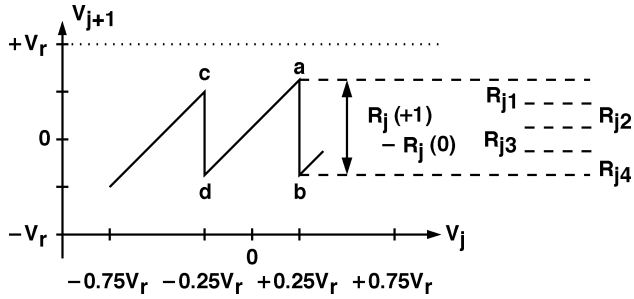

Fig. 6. Conversion characteristic of the SC pipeline stage in Fig. 3 under calibration.

scheme described in the following section. The value for $V_j^{\rm os}$ can be chosen so that $\hat{V}_j^{\rm da}(0) = 0$. Equation (7) can be rearranged as

$$\hat{V}_j^{\rm da}(D_c) = \frac{G_j G_z}{\hat{G}_j \hat{G}_z} \cdot T_j(D_c) \tag{8}$$

where $T_j(D_c)$ is defined as

$$T_j(D_c) = \frac{D_z(D_c)}{G_j}. \tag{9}$$

The digital values of $T_j(D_c)$ are stored and used to generate the ADC's output codes.

During normal A/D conversion operation, the combined A/D conversion for the jth stage followed by the z-ADC can be expressed as

$$V_j = \hat{V}_j^{\rm da}(D_j) + V_j^{\rm os} + \frac{V_{j+1}}{\hat{G}_j}. \tag{10}$$

Combining (10), (6), and (8) gives

$$V_j = \frac{G_{jz}}{\hat{G}_{jz}} \cdot D_{jz} + O_{jz} + Q_{jz} \tag{11}$$

where

$$\text{Digital Output} = D_{jz} = T_j(D_j) + \frac{D_z}{G_j} \tag{12}$$

$$\text{Gain Error} = \frac{G_{jz}}{\hat{G}_{jz}} = \frac{G_j G_z}{\hat{G}_j \hat{G}_z} \tag{13}$$

$$\text{Offset} = O_{jz} = V_j^{\rm os} + \frac{O_z}{\hat{G}_j} \tag{14}$$

$$\text{Quantization Error} = Q_{jz} = \frac{Q_z}{\hat{G}_j}. \tag{15}$$

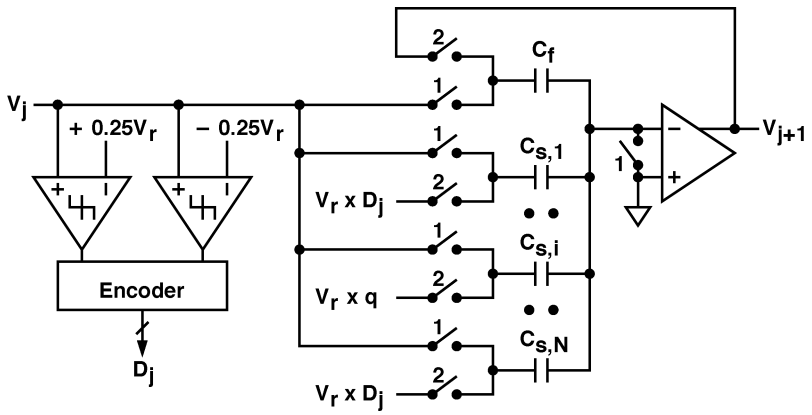

Fig. 7. Radix-2 1.5-b SC pipeline stage for background calibration.

Thus, the combined jth stage and z-ADC has a linear A/D conversion characteristic if D_{jz} of (12) is used as the combined digital output. The conversion carries a new gain error of $G_{jz}/\hat{G}_{jz}$ and a new offset of O_{jz}. The combined quantization error Q_{jz} is reduced by a factor of the stage gain $\hat{G}_j$. The similarity between (11) and (6) indicates that $j+z$ ADC with the linear conversion characteristic of (11) can then be used to calibrate the preceding $(j-1)$th stage.

IV. A Background Calibration Technique

As depicted in (4), the realized gain $\hat{G}_j$ is a function of capacitor ratios as well as the opamp's dc voltage gain A_0. Since A_0 is sensitive to temperature and supply-voltage variations, $\hat{G}_j$ needs to be constantly calibrated in high-resolution ADCs.

The proposed background calibration scheme measures and quantizes $R_j(D_c)$ in (7) without interrupting the normal A/D operation. To achieve this, a modified SC pipeline stage as shown in Fig. 7 is used. The existing capacitor C_s is split into N fragments such that

$$C_s = C_{s,1} + C_{s,2} + \cdots + C_{s,N}. \tag{16}$$

When the clock ϕ_1 is high, all capacitors C_s and C_f are connected together to sample the input signal V_j. When the clock ϕ_2 is high, all of the C_s capacitors are connected to $D_j \cdot V_r$, except for the $C_{s,i}$ capacitor, which is connected to $q \cdot V_r$. The q signal is a digital binary-valued sequence generated from a pseudorandom generator. To measure $R_j(+1)$, the value of q alternates between $+1$ and 0. To measure $R_j(-1)$, q alternates between -1 and 0. Fig. 8 shows the model for this modified pipeline stage. The model has the following transfer characteristic:

$$V_{j+1} = \hat{G}_j \times \left[V_j - \hat{V}_j^{\mathrm{da}}(D_j) - V_j^{\mathrm{os}}\right] + R_{ji}(D_c)\cdot D_j - R_{ji}(D_c)\cdot q \tag{17}$$

where

$$R_{ji}(D_c) = \hat{G}_j \times D_c \times V_r \cdot \frac{C_{s,i}}{C_s + C_f}. \tag{18}$$

The digital code D_c is either $+1$ or -1, depending on the polarity of q. The gain factor $\hat{G}_j$ is defined in (4). As depicted in Fig. 6, $R_{ji}(D_c)$ is a subsection of the transition step height in

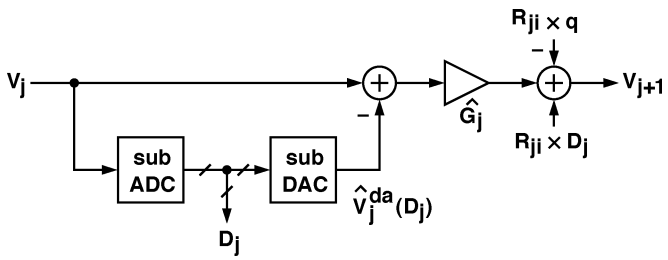

Fig. 8. Model for the modified pipeline stage in Fig. 7.

the V_{j+1} versus V_j transfer function. The relationship between $R_{ji}(D_c)$ and $R_j(D_c)$ can be expressed as

$$R_j(D_c) = \hat{G}_j \times \hat{V}_j^{\mathrm{da}}(D_c) = R_j(D_c - 1) + \sum_{i=1}^{N} R_{ji}(D_c). \tag{19}$$

Thus, $R_j(D_c)$ can be reconstructed from $R_{ji}(D_c)$ and used for digital output correction.

Fig. 9 shows the scheme for extracting $R_{ji}(D_c)$ in the background during normal A/D operation. The value of $R_{ji}(D_c)$ is estimated by quantizing V_{j+1} to obtain D_z using the succeeding z-ADC and then low-pass filtering the $q' \times D_z$ product in the digital domain, where q' has the same waveform pattern as q but alternates between $+1$ and -1. By multiplying both (6) and (17) with q' and applying time-domain averaging, an expression is obtained for the output of the low-pass filter (LPF), D_y. Suppose that q' has a mean value of 0 and is uncorrelated with V_j, then

$$\frac{G_z}{\hat{G}_z} \cdot D_y = -\overline{q'q} \times R_{ji}(D_c) = -\frac{1}{2} \times R_{ji}(D_c). \tag{20}$$

The value of $T_j(D_c)$ can be computed by applying (20), (19), and (9). For normal A/D operation, the digital output D_o is derived from D_k, for $k = 1, \cdots, (j-1)$, and the D_{jz} of (12). Notably, the raw D_z digital output from the z-ADC contains the last two terms of (17) which must be subtracted from D_z before calculating D_{jz}. Once D_y of (20) is found, these two extra terms can be entirely removed from D_z. During the extraction of $R_{ji}(D_c)$, the time-domain averaging process also eliminates the effects of the z-ADC's offset O_z and quantization error Q_z, as long as q and V_j remain uncorrelated.

The above procedures for calibration and A/D conversion can be conducted simultaneously without interrupting each other. The errors due to capacitor mismatches and finite opamp gains

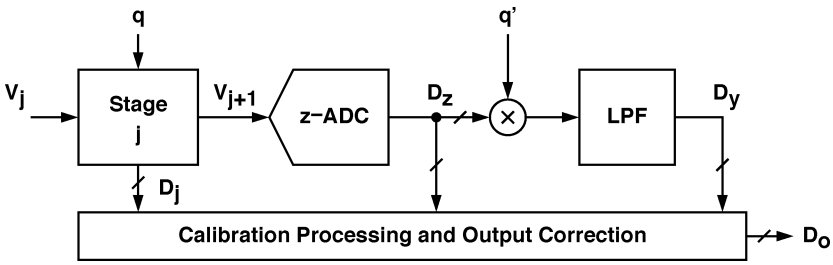

Fig. 9. Block diagram of the background calibration scheme.

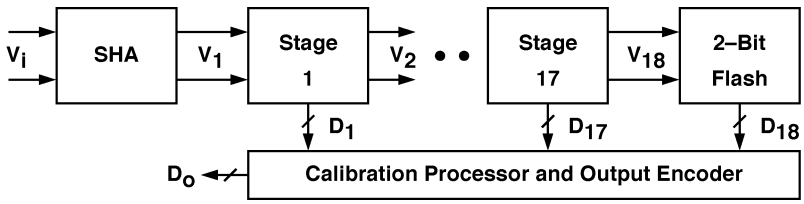

Fig. 10. Block diagram of the ADC prototype.

can all be corrected. As shown in Fig. 7, the only modification to a pipeline stage required by this calibration scheme is splitting the existing C_s capacitor. This modification does not increase the capacitance seen by the opamp's input, and thus it does not degrade the operating speed of the original pipeline stage.

The injection of random sequence R_{ji} into the jth stage also increases its required operating output range. As shown in Fig. 4, if V_j is limited to the range $\pm 0.5V_r$, then the additional output range is

$$\Delta V_{j+1} = \pm \hat{G}_j \times V_r \cdot \frac{C_{s,i}}{C_s + C_f}. \tag{21}$$

For a given opamp's output voltage range, the R_{ji} injection reduces the available signal range for the normal A/D operation and hence decreases the achievable dynamic range of the ADC. This adverse impact can be mitigated by choosing a smaller value for C_s to reduce $\hat{G}_j$. Another approach is to split C_s into more capacitors, i.e., increasing N and resulting in smaller $C_{s,i}$, for $i = 1, \cdots, N$.

V. Prototype Implementation

To demonstrate the calibration technique described in the previous section, an experimental ADC prototype was fabricated in a 0.25-μm 1P5M 2.5-V CMOS technology with MIM capacitors. This section describes the design details.

A. Architecture

Fig. 10 shows the block diagram of the prototype, which consists of a front-end sample-and-hold amplifier (SHA), 17 radix-2 1.5-b SC pipeline stages, and a final 2-b flash stage. The entire analog signal path is fully differential so as to minimize the effects of common-mode noises and to suppress even-order distortions.

Only the first five pipeline stages, i.e. from the first to fifth stage, were designed to employ the proposed background calibration scheme. In each of these stages, hereafter called "the calibrated stage," its C_s capacitor is split into four equal parts, i.e., $N = 4$ in (16). The remaining uncalibrated pipeline stages, from the sixth stage to the 18th stage, constitute a 14-b ADC with approximately 11-b resolution. The resolution is limited mainly by the matching accuracy of the MIM capacitors.

All voltage references are externally applied. The system clock is generated by frequency-dividing an external clock by two to ensure a duty cycle of 50%.

B. Operational Amplifier

Fig. 11 shows the topology of the opamps used in the SHA and all pipeline stages. The fully differential two-stage configuration consists of a telescopic first stage followed by a common-source second stage [20], [21]. The overall dc voltage gain is more than 90 dB. Although the calibration technique described in the previous section eliminates the adverse impact of the opamp's finite voltage gain, nonlinear properties in the opamp's dc transfer function are error sources that cannot be removed. Thus, the opamp is preferred to have a large gain.

With a 2.5-V supply, the opamp can provide a differential output voltage range as large as 2.8 V_{pp}. The opamp's output range must be large enough to cover the entire range of V_{j+1} in (3), plus the extra residue caused by the offsets of the comparators, plus the additional range for the R_{ji} injection. From (21), the required output range in this design with $N = 4$ is 25% more than that of a conventional design.

The opamp's signal path consists of only n-channel devices to maximize the operating speed [22]. The two capacitors C_{c1} and C_{c2} serve as cascoded Miller compensation [23], [24]. However, this compensation scheme may suffer from insufficient gain margin due to the peaking of the magnitude response beyond the unity-gain bandwidth, caused by the nondominant poles [24]. The addition of C_{c3} and C_{c4} generates a left-half-plane zero that can be placed to avoid the peaking [25], [26]. The entire compensation method is similar to the nested cascoded Miller compensation [27]. In the first pipeline stage, the opamp dissipates 22.5 mW of power and achieves a unity-gain frequency of 650 MHz with $C_s = C_f = 2$ pF and an external load of 4 pF.

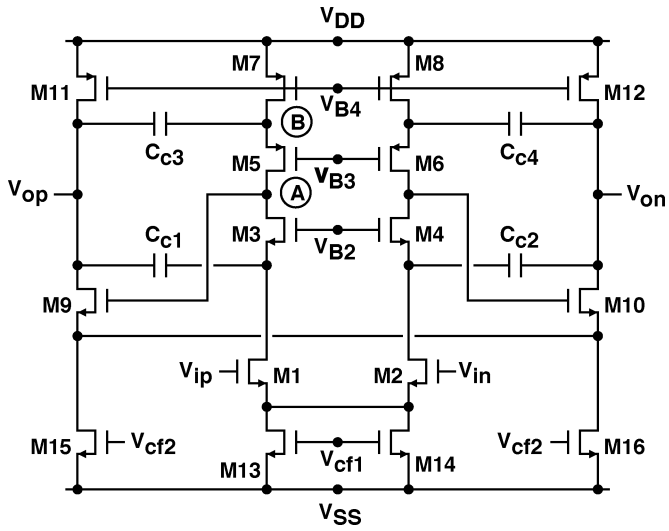

Fig. 11. Simplified circuit schematic of the operational amplifiers.

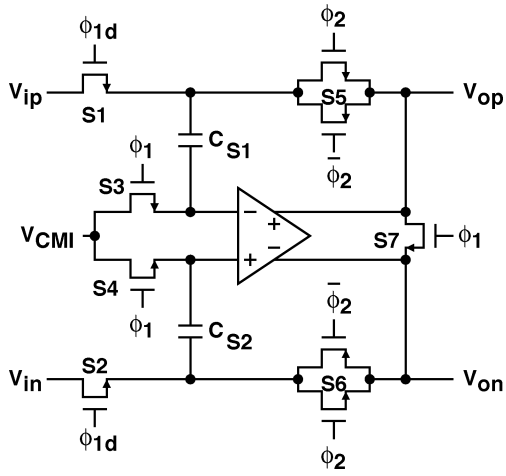

Fig. 12. Simplified circuit schematic of the SHA.

Two separate SC common-mode feedback circuits are used to generate control voltage V_{cf1} and V_{cf2} for the first and second stages of the opamp [22], [28]. The input common-mode voltage is set to 0.95 V, and the output common-mode voltage is set to 1.35 V.

To reduce power dissipation, device scaling along the pipeline has been adopted. However, due to the limited design time, the scaling strategy used is far from optimal. In this prototype, the SHA and the first five pipeline stages use identical opamps. The opamps and capacitors are reduced by half in the next six stages. Another scaling by half is applied to the remaining stages.

C. Sample-and-Hold Amplifier

The SHA adopts a conventional flip-around configuration, as shown in Fig. 12 [22]. It has a fast settling behavior due to a large feedback factor. To employ the bottom-plate sampling technique, S1 and S2 switches are turned off after S3 and S4 have been turned off. The gate-controlling clocks for S1 and S2 are generated from two constant-V_{GS} bootstrapped clock generators [29], [30]. The use of constant-V_{GS} clocks helps reduce the device sizes of S1 and S2 and decrease the distortion caused by charge injection from the switches. The values of the input sampling capacitors C_{S1} and C_{S2} are both 4 pF.

D. Comparator

Fig. 13 shows the schematic diagram of comparators used in all pipeline stages. The comparator consists of a differential-difference preamplifier with a voltage gain of 9, followed by a regenerative latch. In Fig. 7, the threshold voltages for the two comparators are $\pm 0.25V_r$. In this design, the differential V_r is 1.4 V, and its common-mode voltage is 1.35 V. Thus, the corresponding reference voltages for V_{RP} and V_{RN} in Fig. 13 are 1.525 and 1.175 V, respectively.

E. Digital Circuits

Digital functional blocks, such as calibration processor and output encoder, are also integrated in the same chip. Fig. 14 shows the block diagram of the R_{ji} extractor. The LPF in Fig. 9 is realized with a simple accumulator. The digital output from the z-ADC, D_z, is first correlated with the random sequence q' before being integrated by the accumulator. The resulting output D_y is taken only after M cycles of integration, where M is the period of the random sequence q.

Referring to Fig. 9, the quantization step size for a Z-bit z-ADC can be assumed to be $V_r/2^Z$. Furthermore, the analog signal embedded in V_{j+1} for nominal A/D conversion can be assumed to be uniformly distributed between $+0.5V_r$ and $-0.5V_r$. This V_{j+1} causes a fluctuation in D_y, resulting in a varying R_{ji}. The variance of R_j can be expressed as

$$\sigma^2(R_j) = N \times \sigma^2(R_{ji}) = N \times \frac{1}{M}\sigma^2(V_{j+1}) = \frac{N}{M} \times \frac{V_r^2}{12} \quad (22)$$

where N is the number of C_s fragments as defined in (16). By letting $\sigma(R_j)$ be smaller than one half of the z-ADC's quantization step size, the following is obtained:

$$M \geq \frac{N}{3} \times 2^{2Z}. \quad (23)$$

Obviously, large M is required for high resolution, but it also leads to slow calibration process. Equation (23) demonstrates that, to attain a 15-b ADC using the pipeline stage shown in Fig. 7 with $N = 4$, one can choose $M_1 = 2^{28}$ for the first stage, $M_2 = 2^{26}$ for the second stage, $M_3 = 2^{24}$ for the third stage, and $M_n = 2^{30-2n}$ where n is the stage number. However, simulation reveals that the resulting ADC does not reach 15-b resolution due to the accumulation of R_j errors from the cascaded stages. A better choice is to have $M_1 = 2^{28}$, $M_2 = 2^{27}$, $M_3 = 2^{26}$, and $M_n = 2^{29-n}$ where n is the stage number. To simplify the design of this ADC prototype, $M = 2^{28}$ is chosen for all calibrated stages.

For this ADC prototype, only the first five pipeline stages are calibrated. For one calibration cycle, the calibration proceeds backward and sequentially, i.e., from the fifth stage toward the first stage. When calibrating the fifth stage, the z-ADC is the pipeline from the sixth stage to the 18th stage. When calibrating the fourth stage, the z-ADC is the pipeline from the calibrated fifth stage to the 18th stage. When the jth stage is under calibration, the $R_{ji}(D_c)$ values are measured sequentially for $i = 1, 2, 3, 4$, and $D_c = -1, +1$. A total of eight R_{ji} values have to be measured for each calibrated stage. These values are

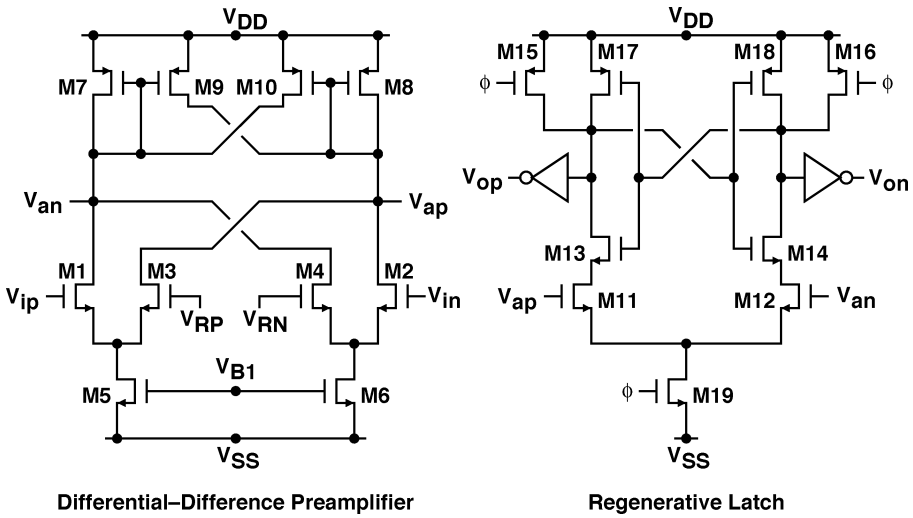

Fig. 13. Circuit schematic of the comparators.

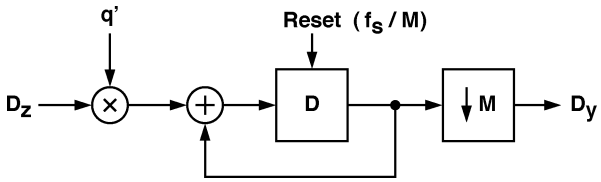

Fig. 14. Block diagram of the R_{ji} extractor.

used to compute $R_j(-1)$ and $R_j(+1)$. The value for $R_j(0)$ is preset to 0. A total of 40×2^{28} sampling periods are required to complete one calibration cycle, which corresponds to 4.5 min for a sampling rate of 40 MS/s. During the initial power-up, the full-cycle calibration time is reduced to 0.065 s by shorting the SHA's inputs to zero and setting $M = 2^{16}$. By shorting the inputs, the $\sigma^2(V_{j+1})$ term in (22) becomes zero, and M can be reduced to speed up the calibration process.

All digital circuits are synthesized with standard cells by commercial CAD tools. The total gate count is approximately 27 000. The biggest adder is the 48-b accumulator used in the R_{ji} extractor. This ADC prototype does not require a multibit multiplier.

VI. Experimental Results

Fig. 15 shows the chip microphotograph of the fabricated ADC. The chip dimensions are 3.8×3.6 mm^2. Digital circuits occupy 12% of the total area. The digital and analog blocks use separate power lines. The analog block is surrounded by analog V_{DD} and V_{SS} power lines. Decoupling capacitors formed by PMOS and NMOS devices are buried underneath the analog power lines. This guard-ring structure shields noise coupled from the digital block via the substrate. Operating at a 40-MS/s sampling rate under a single 2.5-V supply, the analog block consumes a total of 350 mW of power while the digital block consumes only 20 mW.

Figs. 16 and 17 show the ADC's differential nonlinearity (DNL) and integral nonlinearity (INL) characteristics obtained from code-density measurements. Notably, the LSB is normalized to 16-b resolution in those figures. The number of registered output codes is approximately $3/4 \times 2^{16}$. Fig. 16 shows

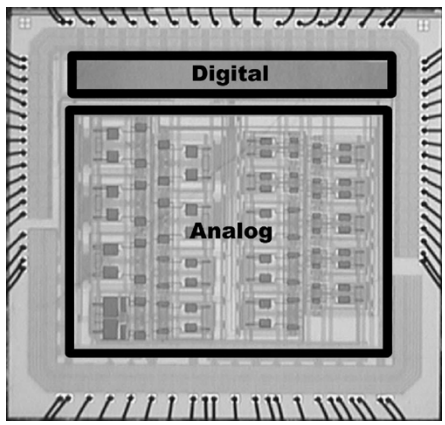

Fig. 15. ADC chip microphotograph.

the ADC's native DNL and INL before activating the calibration processor. The DNL is $+1.2/-0.6$ LSB and the INL is $+15/-15$ LSB. Fig. 17 shows the ADC's DNL and INL after the background calibration is activated. The DNL is reduced to $+0.34/-0.25$ LSB, and the INL is reduced to $+3.4/-4.0$ LSB.

Fig. 18 shows the ADC's output fast Fourier transform (FFT) spectra at a 40-MS/s sampling rate. The input is a differential 2.0 V_{pp} 8.30-MHz sinusoidal signal. Without calibration, the third-order harmonic is the dominant distortion term, which is -76 dB below the fundamental signal. The signal-to-distortion-plus-noise ratio (SNDR) is 68 dB and the spurious-free dynamic range (SFDR) is 76 dB. After the background calibration is activated, the SNDR is improved by 5.5 dB to 73.5 dB and the SFDR is improved by 17.3 to 93.3 dB. Notably, the ADC's signal-to-noise ratio (SNR) remains almost the same before and after calibration. The SNDR/SFDR improvement after calibration comes from the elimination of harmonic tones.

Fig. 19 shows the ADC's measured SNDR and SFDR versus input frequencies at a 40-MS/s sampling rate. The SNDR and SFDR change little up to the Nyquist frequency. Generally, the calibration can improve the SNDR by 5.5 dB and the SFDR by 17 dB. Fig. 20 shows the ADC's SNDR versus input signal level with calibration on and off respectively. The 1 MHz sinusoidal

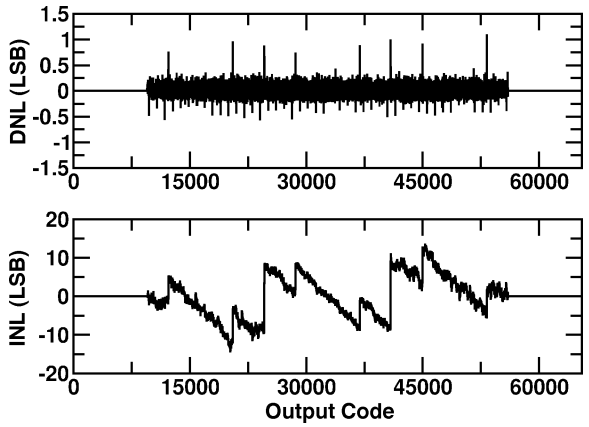

Fig. 16. Measured DNL and INL at 40 MS/s with calibration off.

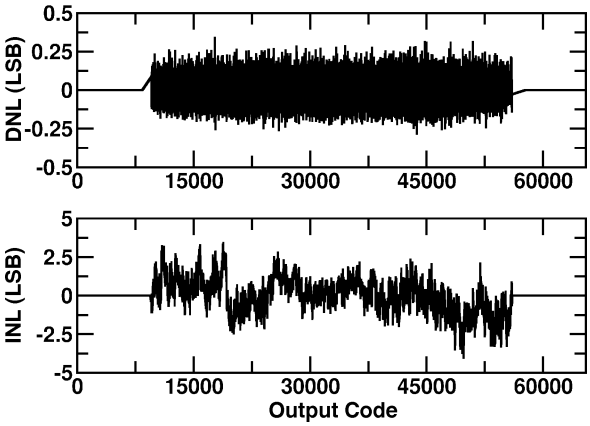

Fig. 17. Measured DNL and INL at 40 MS/s with calibration on.

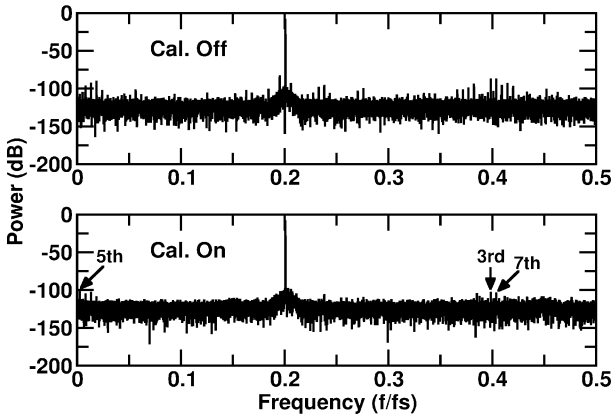

Fig. 18. Measured output FFT spectra. The 2.0-V_{pp} 8.30-MHz differential sinusoidal input is sampled at 40 MS/s.

input is sampled at 40 MS/s. The data reveal that the total noise power, excluding distortions, is not affected by the input level. The noise power does not increase when the calibration is on. Thus, the random term R_{ji} injected into the analog signal path is fully removed in the digital output. The measured dynamic range is approximately 78.5 dB.

Table I summarizes the measured performance of the ADC prototype at room temperature.

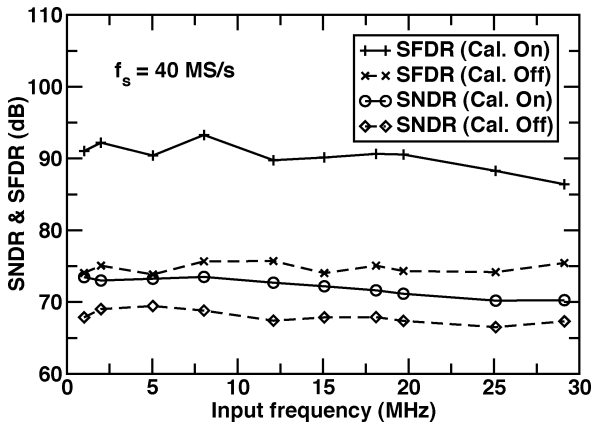

Fig. 19. Measured SNDR and SFDR versus input frequency at 40-MS/s sampling rate.

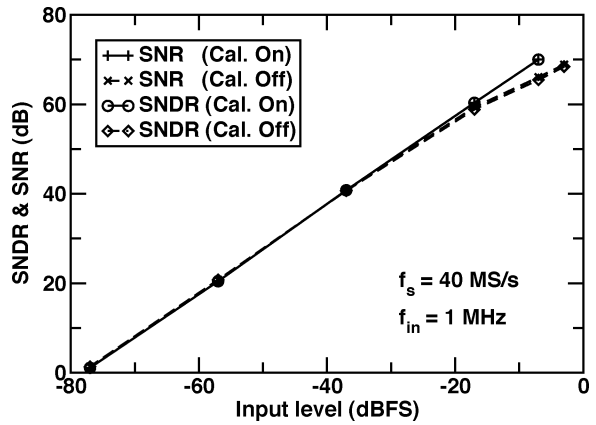

Fig. 20. Measured SNDR and SNR versus input level. The 1-MHz differential sinusoidal input is sampled at 40 MS/s.

TABLE I
ADC PERFORMANCE SUMMARY

Technology	0.25 μm CMOS
Chip Area	3.8×3.6 mm^2
Supply, V_{AA}/V_{DD}	2.5/2.5 V
Power, P_{AA}/P_{DD}	350/20 mW
Max. Sampling Rate	40 MS/s
Differential Input Range	2.1 V_{pp}
Number of Output Codes	$(3/4) \times 2^{16}$
DNL, normalized to 16 bits	$-0.25/+0.34$ LSB
INL, normalized to 16 bits	$-4.00/+3.40$ LSB
SFDR, f_s = 40 MS/s, f_{in}=8.03MHz	93.3 dB
SNDR. f_s = 40 MS/s, f_{in}=8.03MHz	73.5 dB

VII. CONCLUSION

A high-resolution CMOS pipelined ADC consisting of 17 radix-2 1.5-b SC pipeline stages and a final 2-b flash stage has been realized to demonstrate the feasibility of a proposed digital background calibration technique. A pipeline stage can be calibrated without interrupting its normal A/D operation by injecting a random sequence into its MDAC through the split $C_{s,i}$ capacitor. The calibration can correct the errors resulting from capacitor mismatches and finite opamp gains. All calibration procedures are conducted in the digital domain. The required

modification to the analog signal path is minimal and is not crucial to the circuit's performance. This calibration scheme is also robust since its effectiveness does not rely on the input's amplitude distribution. Ultimately, the linearity of the calibrated ADCs is constrained by the opamps' nonlinear characteristics, the capacitors' voltage coefficients and the transient behavior of the circuitry.

The 15-b 40-MS/s CMOS pipelined ADC was fabricated in a 0.25-μm CMOS technology. This chip occupies 3.8×3.6 mm^2 and dissipates 370 mW from a single 2.5-V supply. It achieves an SFDR of more than 90 dB and an SNDR of more than 73 dB. The calibration can improve SFDR by 17 dB and SNDR by 5.5 dB. The SNDR is limited by coupling noises. The maximum sampling rate is limited by the speed of the opamps.

Although only a radix-2 1.5-b switched-capacitor pipeline stage is demonstrated herein, the principle of the proposed calibration technique is applicable to multibit pipeline stages and circuit configurations other than the SC circuit.

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Hung-Chih Liu (M'96) received the B.S. degree in electrical engineering from the National University of Marine and Technology, Keelung, Taiwan, in 1987 and the M.S. degree in electrical engineering from National Taiwan University, Taipei, in 1989. He is currently working toward the Ph.D. degree in electronics engineering at National Chiao-Tung University, Hsin-Chu, Taiwan, R.O.C.

In 1993, he joined Silicon Integrated Systems Corporation as a Group Leader developing analog and mixed-signal integrated circuits, including self-calibrating A/D and D/A converters, sigma-delta A/D and D/A converters, PLLs, and high-speed serial links for USB2.0, SATA, DVI, and PCI-Express.

Zwei-Mei Lee (S'03) received the B.S. degree in electronics engineering from National Central University, Chung-Li, Taiwan, R.O.C., in 1997. She is currently working toward the Ph.D. degree in electronics engineering at National Chiao-Tung University, Hsin-Chu, Taiwan.

Her current research interest is high-speed high-resolution A/D converter design.

Jieh-Tsorng Wu (S'83–M'87) was born in Taipei, Taiwan, on August 31, 1958. He received the B.S. degree in electronics engineering from National Chiao-Tung University, Hsin-Chu, Taiwan, R.O.C., in 1980, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1983 and 1988, respectively.

From 1980 to 1982, he served in the Chinese Army as a Radar Technical Officer. From 1982 to 1988, at Stanford University, he focused his research on high-speed analog-to-digital conversion in CMOS VLSI. From 1988 to 1992, he was a Member of Technical Staff at Hewlett-Packard Microwave Semiconductor Division, San Jose, CA, where he was responsible for several linear and digital gigahertz IC designs. Since 1992, he has been with the Department of Electronics Engineering, National Chiao-Tung University, where he is now a Professor. His current research interests are high-performance mixed-signal integrated circuits.

Dr. Wu is a member of Phi Tau Phi.