SCR Device Fabricated With Dummy-Gate Structure to Improve Turn-On Speed for Effective ESD Protection in CMOS Technology

Ming-Dou Ker, *Senior Member, IEEE* and Kuo-Chun Hsu, *Member, IEEE*

***Abstract*—Turn-on speed is the main concern for an on-chip electrostatic discharge (ESD) protection device, especially in the nanoscale CMOS processes with ultrathin gate oxide. A novel dummy-gate-blocking silicon-controlled rectifier (SCR) device employing a substrate-triggered technique is proposed to improve the turn-on speed of an SCR device for using in an on-chip ESD protection circuit to effectively protect the much thinner gate oxide. The fabrication of the proposed SCR device with dummy-gate structure is fully process-compatible with general CMOS process, without using an extra mask layer or adding process steps. From the experimental results in a 0.25-μm CMOS process with a gate–oxide thickness of $\sim$ 50 Å, the switching voltage, turn-on speed, turn-on resistance, and charged-device-model ESD levels of the SCR device with dummy-gate structure have been greatly improved, as compared to the normal SCR with shallow trench isolation structure.**

***Index Terms*—Charged device model (CDM), dummy gate, electrostatic discharge (ESD), silicon-controlled rectifier (SCR).**

I. Introduction

ELECTROSTATIC discharge (ESD) is a transient process of high energy transfer from outside an integrated circuit (IC) to the internal chip, when the IC is floated. The total discharge process of a human-body-model (HBM) [1] ESD event spans only about 100 ns. Several hundred volts, or even several thousand volts, are transferred during ESD stress. For deep-submicron CMOS technologies, the gate oxide thickness has been scaled down to increase circuit operating speed. However, its time-to-breakdown ($t_{\rm BD}$) or charge-to-breakdown ($Q_{\rm BD}$) will also decrease. The ultrathin gate oxide cannot survive if the overstressed ESD pulse duration is too long. ESD events can cause latent damage [2]–[4] or failure to core circuits, if the ESD protection circuits do not work in time. A superior ESD protection device must have high enough ESD robustness and fast enough turn-on speed to effectively protect the thinner gate oxide of the input stage from ESD overstress. With the best area efficiency, a silicon-controlled rectifier (SCR) can sustain the highest ESD level in the smallest layout area, as compared with other ESD protection devices. Thus, the SCR had been used as on-chip ESD protection for a long time [5], [6]. But, SCR still has a higher switching voltage ($\sim$ 22 V) in 0.25-μm CMOS technology, which is generally greater than the gate–oxide breakdown voltage of the input stage. So, it is imperative to reduce the switching voltage of the SCR and to enhance the turn-on speed of SCR for efficiently protecting the ultrathin gate oxide from latent damage or rupture, especially against the faster charged-device-model (CDM) [7] ESD events. Some reports had presented solutions (such as modified device structures and advanced trigger-assist circuit techniques) to overcome this issue [8]–[10], including a substrate-triggered SCR (STSCR) device [11].

In this work, a novel dummy-gate structure is used to block the shallow trench isolation (STI) and silicide between the diffusion regions in the SCR device, and therefore to further enhance its turn-on speed and CDM ESD levels [12], [13]. The fully silicided STSCR with dummy-gate structure has the advantages of lower switching voltage, lower clamping voltage, smaller turn-on resistance, and faster turn-on speed, as compared to the STSCR with STI. With suitable ESD-detection circuit, the STSCR with dummy-gate structure is designed to be kept off during normal circuit operating conditions, and to be quickly triggered on during the ESD-zapping conditions. Therefore, the ultrathin gate oxide in deep-submicron CMOS processes can be effectively protected by the STSCR with a dummy-gate structure. In the future, nanoscale CMOS process with VDD below 1.2 V, concern for latchup will be eliminated, because the holding voltage of the SCR device is greater than the maximum voltage level of the power supply voltage VDD.

II. SCR Device With Dummy-Gate Structure

The normal fully silicided STSCR device with STI structure [11] is shown in Fig. 1(a). In a typical 130-nm CMOS process, the depth of STI is about $\sim$ 0.4 μm, but the junction depth of P^+/N^+ diffusion is only about $\sim$ 0.15 μm. The deeper STI region in the SCR device creates a longer current path from the anode to the cathode, which also leads to a slower turn-on speed of the SCR. In order to further enhance the turn-on speed of the STSCR device, the STI structure must be blocked. In nanoscale CMOS processes, the STI region is defined by the active area (thin oxide) mask. Then, the P^+/N^+ diffusions regions will be formed through the definition of implantation masks. In such a typical process flow, the STI regions between diffusions in the active area can be blocked. But, the extra silicide-blocking mask must be used to block the silicide between diffusions in

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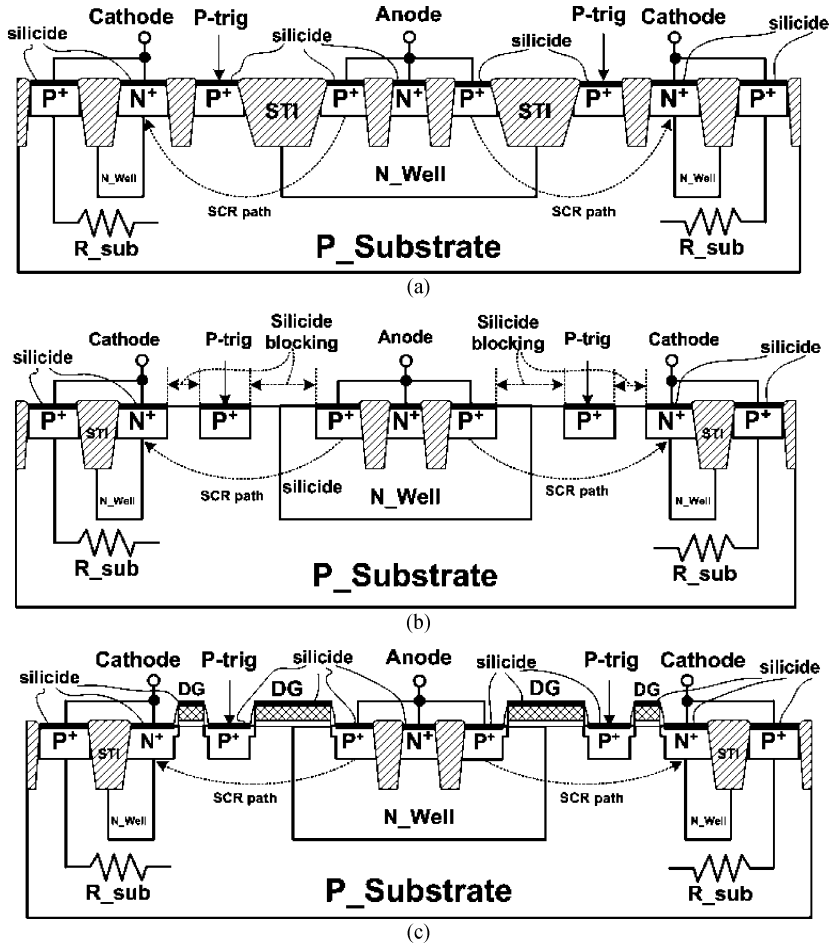

Fig. 1. Device structures of (a) the STSCR device with STI, (b) the STSCR device with extra silicide-blocking mask, and (c) the proposed STSCR device with dummy-gate structure.

the fully silicided CMOS processes, otherwise the anode and the cathode of SCR device will become a short circuit. The STSCR with silicide-blocking structure is shown in Fig. 1(b). To achieve higher performance circuit operation, some advanced circuit designs did not use the silicide-blocking mask in the input/output (I/O) circuits. To increase the ESD robustness of I/O circuits but avoid using the silicide-blocking mask, some layout techniques had been invented to improve ESD levels of nMOS device [14]–[16]. Moreover, with the extra silicide-blocking mask, the process flows and total fabrication costs will be increased. In this work, a dummy-gate structure is proposed to block the silicide and STI between the diffusion regions in the SCR device without adding extra process masks and increasing the fabrication costs.

The proposed STSCR device with dummy-gate structure is shown in Fig. 1(c). The ESD current paths in these STSCR devices are indicated by the dashed lines in Fig. 1(a)–(c). The ESD current path in Fig. 1(c) is the shortest, because the spacing between the diffusion regions isolated by the dummy-gate structure is the smallest design rule in the typical CMOS process, and the deeper STI regions do not exist in the ESD current path in Fig. 1(c). The turn-on speed of STSCR with dummy-gate structure will have greater benefits than that of STSCR with STI or silicide-blocking structure. Thus, in this paper, the device characteristics and ESD performance of the STSCR with dummy-gate structure will be investigated in detail. As compared with the traditional LSCR device structure [5], the extra P^+ diffusions are inserted into the STSCR device structure. The inserted P^+ diffusions are connected out as the p-trigger node of the STSCR. When a trigger current is applied into the trigger node, the base voltage of the NPN transistor will be raised due to the substrate resistor ($R_{\rm sub}$). As long as the base voltage of the NPN transistor is greater than 0.7 V, the NPN bipolar transistor in the SCR structure is active. The collector current of the NPN is generated to trigger on the PNP bipolar transistor. When the PNP transistor is turned on, the collector current of the PNP is in turn generated to further bias the NPN transistor. The positive feedback regeneration mechanism of the SCR latching process [17], [18] is initiated by the substrate-triggered current. Finally, the STSCR will be successfully triggered into its latching state to discharge the ESD current.

For on-chip ESD protection purposes, the corresponding ESD-detection circuit [11] has to be designed to control the turn-on of this STSCR with the dummy-gate structure. The ESD-detection circuits can be designed according to the principle of RC delay (used to distinguish ESD-zapping events from the normal circuit operating conditions) or the gate-coupled circuit technique (used to generate the trigger

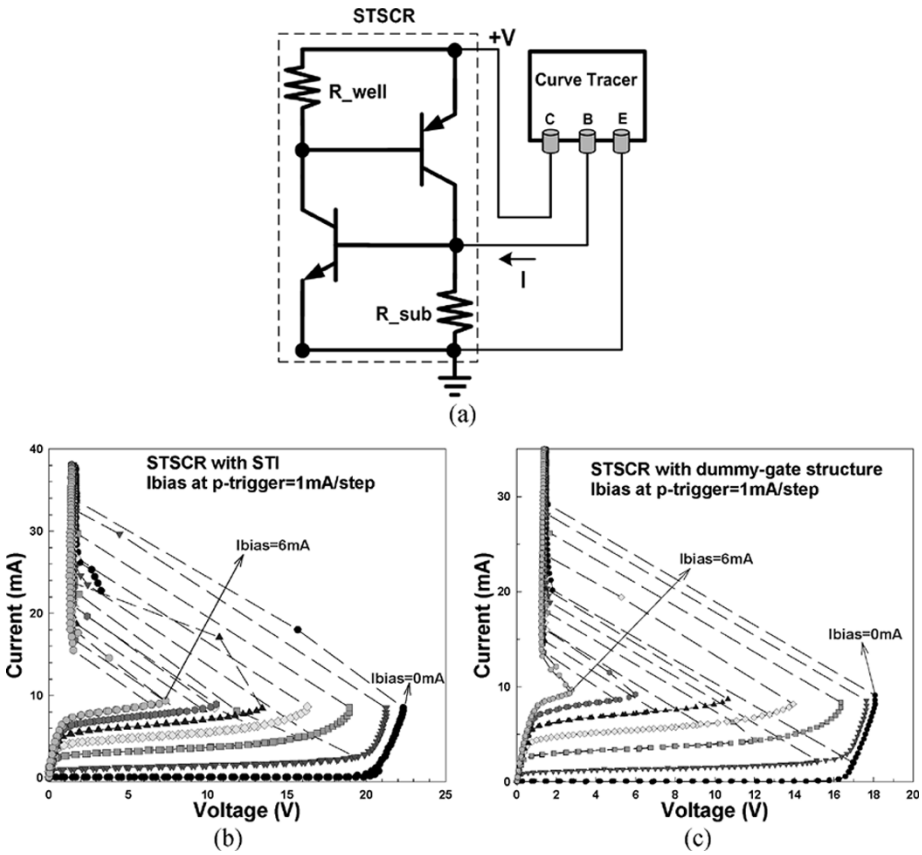

Fig. 2. (a) Measurement setup to find the dc I–V curves of STSCR devices. The dc I–V curves of STSCR with (b) STI and (c) dummy-gate structures under different substrate-triggered currents.

current) to turn on this STSCR device during ESD-zapping conditions. With the suitable ESD-detection circuit, the STSCR with dummy-gate structure is designed to be kept off without interfering the I/O signals during normal circuit operating conditions, and to be quickly triggered on to discharge ESD current during the ESD-zapping conditions. So, the STSCR with dummy-gate structure can be successfully used in the input, output, and power-rail ESD protection circuits. To avoid the latchup issue in the STSCR device, the voltage drop elements (such as diodes or STSCR devices) can be stacked with the dummy-gate blocking STSCR device to elevate its total holding voltage in the bulk CMOS process. As long as the total holding voltage of ESD protection device (including the STSCR and the voltage drop elements) is greater than the maximum voltage level of VDD, the latchup concern inherent in SCR structure can be eliminated during normal circuit operating conditions.

III. Experimental Results

A. Device Characteristics

Two fully silicided STSCR devices with STI and dummy-gate structures have been fabricated with the same layout area in a 0.25-μm CMOS process. The active areas (without including the guard rings) of these two STSCR devices in the test chip are 20 μm$\times$ 20 μm. The measurement setup to plot the dc current–voltage (I–V) curves of the fabricated SCR devices under substrate-triggering technique is shown in Fig. 2(a). The dc I–V curves of the STSCR with STI and dummy-gate structures under different substrate-triggered currents are shown in Fig. 2(b) and (c), respectively. When the substrate-triggered current applied at the p-trigger node is increased from 0 to 6 mA, the switching voltage of STSCR with STI is reduced from $\sim$ 22 to $\sim$ 7 V, whereas that of STSCR with dummy-gate structure is reduced from $\sim$ 18 to $\sim$ 3 V. With the substrate-triggered current, both the STSCR with STI and dummy-gate structures can be triggered into the latching state without involving the avalanche breakdown mechanism [19]. The dependences of the switching voltage of STSCR devices with STI and dummy-gate structures on the substrate-triggered current are compared in Fig. 3. If

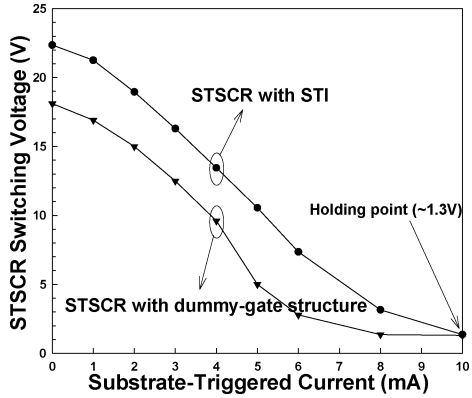

Fig. 3. Dependences of the switching voltages of STSCR devices with STI or dummy-gate structure on the substrate-triggered current.

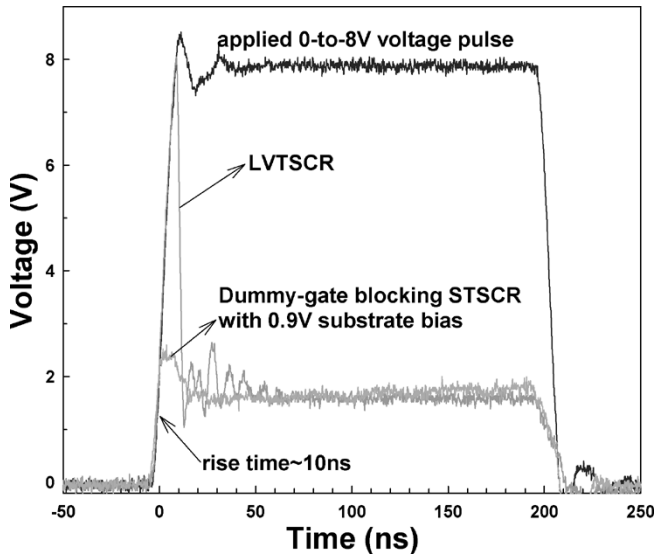

Fig. 4. Comparison of turn-on speed between the LVTSCR and the dummy-gate blocking STSCR with 0.9-V substrate bias under an applied 0–8 V voltage pulse.

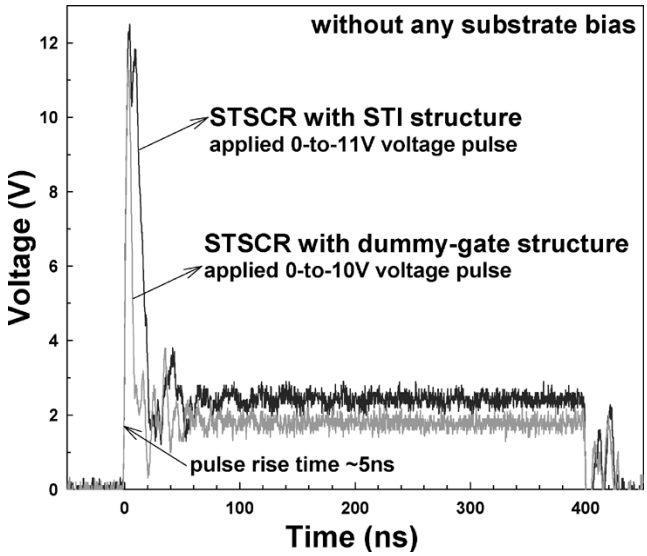

Fig. 5. Comparison of turn-on speed between the STSCR with STI and dummy-gate structures without any substrate bias applied at p-trigger node.

the trigger current is continually increased, the switching voltages of both STSCR devices will be reduced to a value close to their holding voltages ($\sim$ 1.3 V). Moreover, the switching voltage of the STSCR with the dummy-gate structure can be further reduced below that of the STSCR with STI under the same trigger current. This is related to the current gain (β) of the parasitic bipolar transistor in SCR structure, which will be discussed later. The SCR device with the lower switching voltage can clamp the ESD overstresses more quickly to effectively protect the thinner gate oxide of the core device.

B. Turn-On Speed

The comparison of turn-on speed between a traditional low-voltage-triggering SCR (LVTSCR) [8] and the new STSCR with the dummy-gate structure under an applied 0–8 V voltage pulse is shown in Fig. 4. The dummy-gate blocking STSCR with 0.9-V substrate bias is initially triggered on at $\sim$ 2.5 V through the positive feedback regeneration mechanism, but the LVTSCR is initially triggered on at a higher voltage level of 8 V through the drain avalanche breakdown of the inserted short-channel nMOS device. The 8-V voltage pulse is more quickly clamped to a stable low-voltage level ($\sim$ 1.7 V) by the dummy-gate blocking STSCR with a 0.9-V substrate bias than by the traditional LVTSCR. The STSCR with the dummy-gate structure has a lower switching voltage and faster turn-on speed than the LVTSCR device, if enough substrate bias is applied to the STSCR device. Therefore, the new STSCR with dummy-gate structure is more suitable to protect the ultrathin gate oxide of input stages against ESD overstresses.

In addition, the comparison of turn-on speed between the STSCR devices with STI and dummy-gate structures without any substrate bias applied at the p-trigger node is shown in Fig. 5. When a 0–10 V voltage pulse with 5-ns rise time is applied, the STSCR with dummy-gate structure can be triggered on to clamp the voltage pulse to a low voltage level, but the STSCR with STI cannot be triggered on until a 0–11 V voltage pulse with 5-ns rise time is applied. Due to the $\mathrm{dV/dt}$ transient current, the dynamic switching voltages of STSCR devices are smaller than the static switching voltage of STSCR devices, as shown in Fig. 2. But, the dynamic switching voltage of STSCR with dummy-gate structure is still smaller than that of STSCR with STI. The STSCR with dummy-gate structure also has a lower clamping voltage level ($\sim$ 1.9 V) than that ($\sim$ 2.4 V) of STSCR with STI. Moreover, the ESD-like voltage pulse can be more quickly clamped to a stable low-voltage level by the STSCR with dummy-gate structure than by the STSCR with STI. This proves that the turn-on speed of STSCR with dummy-gate structure is faster than that of STSCR with STI.

In order to further investigate the dependence of turn-on efficiency of the STSCR devices with STI and dummy-gate structures on substrate bias, the experimental setup to measure the required turn-on times of the STSCR devices is illustrated in Fig. 6(a). A 5-V voltage bias is connected to the anode of the STSCR device through a resistance of 10 Ω, which is used to limit the sudden large transient current from power supply when the STSCR is turned on. The turn-on time of STSCR is defined as the time for STSCR to enter its latched state. The measured turn-on times for STSCR devices with STI and dummy-gate structure are shown in Fig. 6(b) and (c), respectively. The V_{anode} is the voltage waveform on the anode of STSCR shown in Fig. 6(a). From Fig. 6(b), the turn-on time of STSCR with STI is reduced from 35, 20, to 11.2 ns, while the STSCR is triggering by the voltage pulse of 1.5, 2, and 4 V with 10-ns rise time into the p-trigger node, respectively. Moreover, from Fig. 6(c), the turn-on time of STSCR with the dummy-gate structure is further reduced from 25.4, 13.6, to 9.8 ns under the same measurement conditions as those of Fig. 6(b). The comparison of the turn-on time between STSCR with STI and dummy-gate structures under different voltage pulses with 10-ns rise time applied at the p-trigger node is summarized in

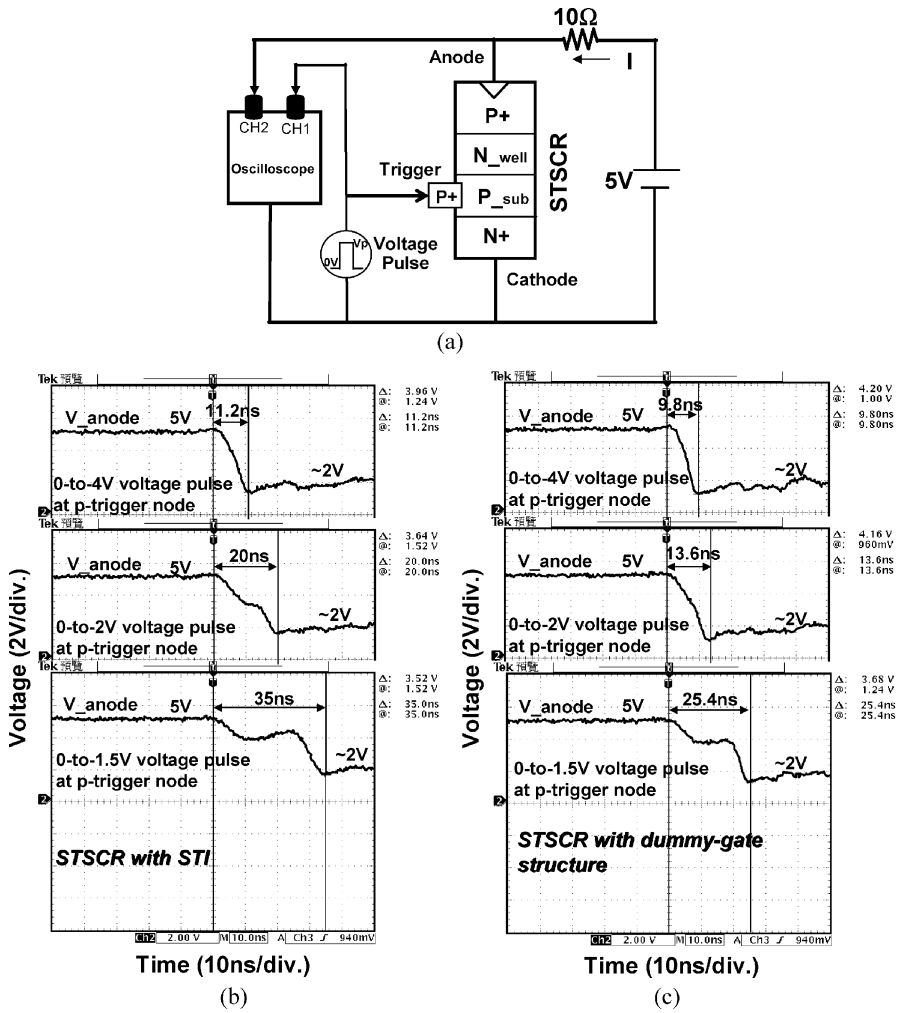

Fig. 6. Measurement on the turn-on time of STSCR with STI and dummy-gate structures under different voltage pulses. (a) The measurement setup. The measured voltage waveforms on the anode of the STSCR with (b) STI and (c) dummy-gate structure, while the STSCR is triggering by the voltage pulse of 1.5, 2, and 4 V into the trigger node.

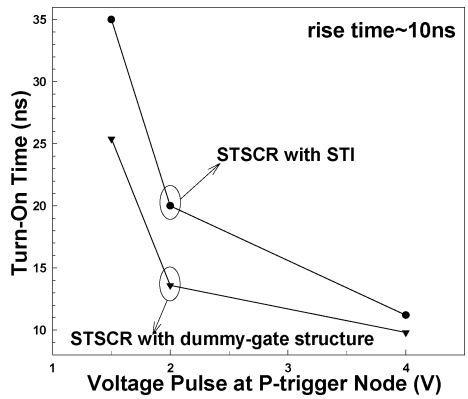

Fig. 7. Comparison of the turn-on time between STSCR with STI and dummy-gate structures under different voltage pulses with 10-ns rise time applied at the p-trigger node.

Fig. 7. With the increased pulse voltage applied at the p-trigger node, the turn-on time of both STSCR devices with STI and dummy-gate structures will be reduced. Moreover, the turn-on time of the STSCR with dummy-gate structure is shorter than that of the STSCR with STI under the same substrate voltage pulse. The dependence of turn-on time of the STSCR with the

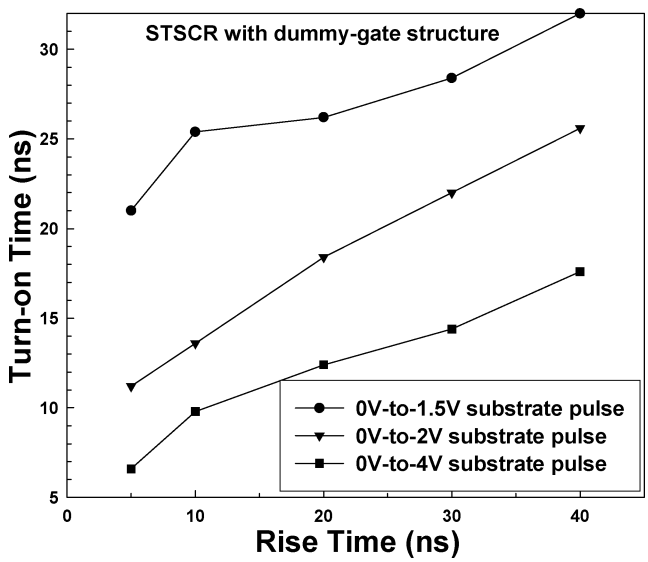

Fig. 8. Dependence of the turn-on time of STSCR with dummy-gate structure on the rise time of voltage pulse under different substrate bias conditions.

dummy-gate structure on different rise times of voltage pulse under different substrate pulse conditions is shown in Fig. 8.

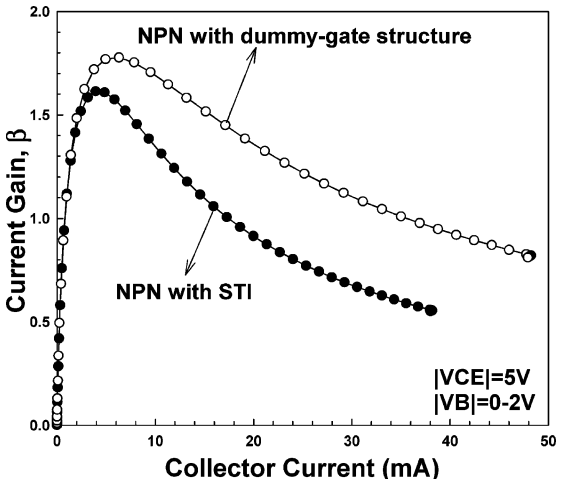

Fig. 9. Dependence of current gains of the NPN bipolar transistors in the STSCR devices with STI or dummy-gate structures on its collector current.

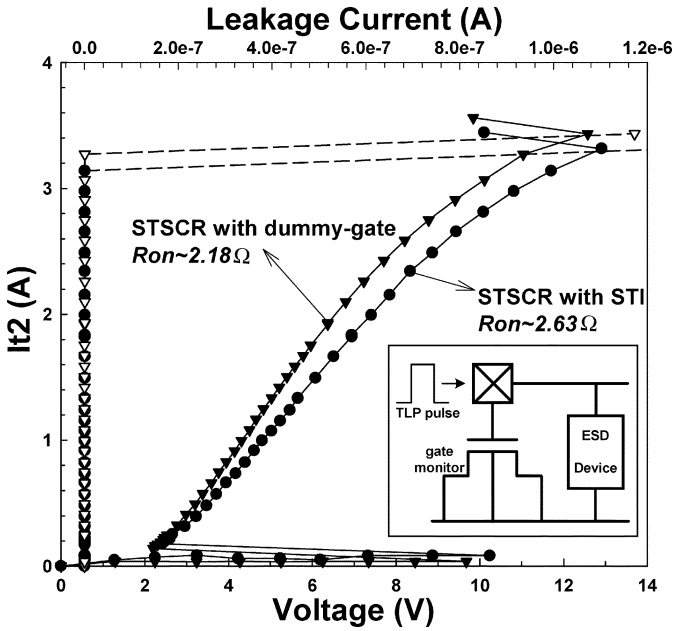

Fig. 10. TLP-measured I–V curves of the STSCR with STI and dummy-gate structures.

With the reduction of pulse rise time, the turn-on time of the STSCR with the dummy-gate structure will be also shortened under the same substrate pulse voltage. When a 4-V substrate pulse with rise time of 5 ns is applied to the p-trigger node, the turn-on time of the STSCR with the dummy-gate structure can be shortened to only 6.6 ns. So, the turn-on time of such STSCR with dummy-gate structure can trace the rise time of ESD event (even the CDM stress) to efficiently protect the ultrathin gate oxide, if a high enough voltage pulse has been applied to the STSCR device. For CMOS IC applications with ultrathin gate oxide, the dummy-gate blocking STSCR device with faster turn-on speed can be designed to protect the core circuits from latent damage more efficiently than the STSCR with STI.

The dependence of current gains of NPN bipolar transistors in the STSCR with STI and dummy-gate structures on the collector current under the measured conditions of $|\mathrm{VCE}| = 5$ V and $|\mathrm{VB}| = 0 - 2$ V is shown in Fig. 9. The current gain of the NPN in the STSCR with dummy-gate structure is higher than that of NPN in the STSCR with STI due to the shorter current path. The switching voltage of STSCR device is in inverse proportion to the current gain [20], so the STSCR with dummy-gate structure has a lower switching voltage. In addition, the substrate bias used to trigger the NPN transistor in the STSCR device has significant effect to further reduce the switching voltage and the turn-on time of STSCR with the dummy-gate structure, as compared with the STSCR with STI.

C. ESD Robustness

The secondary breakdown current (I_{t2}) is the index for the HBM ESD robustness, which is indicated by the sudden increase of the leakage current under the voltage bias of 1.2 V in this work. The relation between secondary breakdown current (I_{t2}) and HBM ESD level (V_{ESD}) can be approximated as $V_{\mathrm{ESD}} \cong I_{t2} \times 1.5\ \mathrm{k}\Omega$, where 1.5 k$\Omega$ is the equivalent resistance of human body. The I–V curves of STSCR with STI and dummy-gate structures measured by the transmission line pulsing (TLP) system are shown in Fig. 10 with the measurement setup. The gate monitor device is a nMOS capacitor to verify the effectiveness of the ESD protection device. The leakage currents of the gate monitor device are the same before and after the TLP measurements. This implies that the thin gate oxide of nMOS can be fully protected by the STSCR with the dummy-gate structure. The I_{t2} of both STSCR devices are almost the same, but the turn-on resistance ($\sim$ 2.18 Ω) of STSCR with the dummy-gate structure is smaller than that ($\sim$ 2.63 Ω) of STSCR with STI. The STSCR devices with STI and dummy-gate structures are designed with the same layout spacing to study the STI-blocked effect in this paper. In fact, the layout spacing of STSCR with the dummy-gate structure can be further reduced, so the current path and turn-on resistance of STSCR with the dummy-gate structure can be also reduced. Under the breakdown limitation of the ultrathin gate oxide of input stage, the STSCR with the dummy-gate structure with a smaller turn-on resistance can sustain more ESD current than that of STSCR with STI with a larger turn-on resistance.

The human-body-model (HBM) [1], machine-model (MM) [21], and charged-device-model (CDM) [7] ESD tests are used to verify the ESD levels of STSCR devices with STI and dummy-gate structures. The comparison of the ESD robustness between the STSCR with STI and dummy-gate structures is shown in Table I. In this ESD verification, the failure criterion is defined as the measured voltage after ESD zapping at the current level of 1 μA is shifted 30% from its original value. The HBM (MM) ESD levels of both STSCR devices with STI and dummy-gate structures are almost the same and equal to $\sim$ 7 kV ($\sim$ 600 V). The comparison of leakage current between the STSCR with STI and the dummy-gate structures before and after the 4-kV HBM ESD zapping is shown in Fig. 11. Although the proposed STSCR with the dummy-gate structure has a larger leakage current (originating from the dummy-gate structures) than the STSCR with STI, the leakage current of STSCR with the dummy-gate structure is still smaller than

TABLE I
COMPARISON OF THE ESD ROBUSTNESS BETWEEN THE STSCR WITH STI AND DUMMY-GATE STRUCTURES

ESD stress / Device	HBM (kV)	MM (V)	CDM (+) (V)	CDM (-) (V)
STSCR with STI	~7	600	800	-650
STSCR with dummy-gate	~7	650	***1500***	***-900***

Active area: STSCR with STI or dummy-gate is drawn as 20 μm×20 μm.

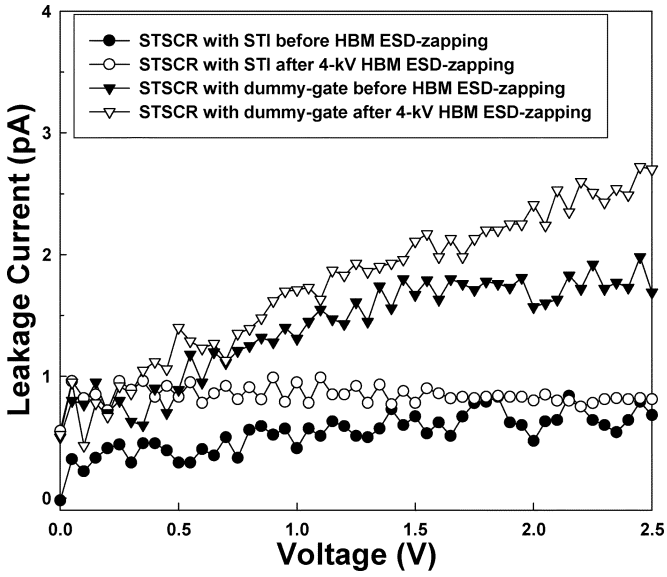

Fig. 11. Comparison of leakage current between the STSCR with STI and dummy-gate structures before and after 4-kV HBM ESD zapping.

3 pA at 2.5-V normal circuit operating condition even after 4-kV HBM ESD zapping. For reference, a gate-grounded nMOS (GGNMOS) device with $(W/L) = 200\ \mu\text{m}/0.5\ \mu\text{m}$ has been fabricated in the same CMOS process with extra silicide-blocking mask. This GGNMOS which occupied a large active layout area of 25.8 μm$\times$ 50 μm can only sustain the HBM ESD level of 3.5 kV. This verifies the area efficiency of the STSCR device with dummy-gate structure (17.5 V/μm^2 for STSCR with dummy-gate structure, but only 2.71 V/μm^2 for GGNMOS).

Under the socket-mode CDM ESD test, the CDM ESD level of the STSCR with the dummy-gate structure is significantly higher than that of STSCR with STI structure. The dummy-gate blocking STSCR device with gate monitor device can sustain the positive (negative) CDM ESD level of 1500 (−900) V, but the STI STSCR device with gate monitor device can only sustain that of 800 (−650) V in the same 0.25-μm CMOS process. The gate monitor device is the nMOS capacitor in these CDM ESD-zapping tests. The gate of the nMOS capacitor is connected to a pad, which is protected by the STSCR with STI or dummy-gate structures. The leakage currents of the gate monitor device are the same before and after the ESD zapping. From the CDM-zapping results, the STSCR with the dummy-gate structure can be indeed triggered on faster to protect the ultrathin gate oxide of input stage and to sustain higher CDM ESD robustness, as compared to the STSCR with STI. Therefore, blocking the STI region in the STSCR device structure can reduce the switching voltage, enhance the turn-on speed, and increase the CDM ESD level of the SCR device.

IV. CONCLUSION

The novel dummy-gate structure to block the STI region in the SCR device with substrate-triggered design has been successfully investigated in a 0.25-μm salicided CMOS process. The proposed STSCR device with the dummy-gate structure is fully process-compatible to the general silicided CMOS processes without using an extra silicide-blocking mask. As compared to the STSCR with STI structure, the STSCR with the dummy-gate structure has a lower switching voltage, smaller turn-on resistance, lower clamping voltage, higher bipolar current gain, faster turn-on speed, and higher CDM ESD level to effectively protect the ultrathin gate oxide against ESD stresses. The STSCR with the dummy-gate structure can sustain the positive (negative) CDM ESD level of 1500 (−900) V, but the STSCR with STI can only sustain that of 800 (−650) V in the same 0.25-μm CMOS process. With a faster turn-on speed, the proposed STSCR with dummy-gate structure can effectively protect the ultrathin gate oxide against ESD damage in future nanoscale CMOS integrated circuits without latchup issue.

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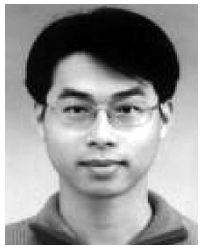

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