ESD Implantations for On-Chip ESD Protection With Layout Consideration in 0.18-μm Salicided CMOS Technology

Ming-Dou Ker, *Senior Member, IEEE*, Che-Hao Chuang, and Wen-Yu Lo

***Abstract*—One method to enhance electrostatic discharge (ESD) robustness of the on-chip ESD protection devices is through process design by adding an extra "ESD implantation" mask. In this work, ESD robustness of nMOS devices and diodes with different ESD implantation solutions in a 0.18-μm salicided CMOS process is investigated by experimental testchips. The second breakdown current (I_{t2}) of the nMOS devices with these different ESD implantation solutions for on-chip ESD protection are measured by a transmission line pulse generator (TLPG). The human-body-model (HBM) and machine-model (MM) ESD levels of these devices are also investigated and compared. A significant improvement in ESD robustness is observed when an nMOS device is fabricated with both boron and arsenic ESD implantations. The ESD robustness of the N-type diode under the reverse-biased stress condition can also be improved by the boron ESD implantation. The layout consideration in multifinger MOSFETs and diodes for better ESD robustness is also investigated.**

***Index Terms*—CMOS, diode, electrostatic discharge (ESD) implantation, ESD protection, snapback breakdown.**

I. Introduction

WITH the migration toward shallower junctions, much thinner gate oxides, salicided (self-aligned silicide) diffusions, Cu-interconnections, and lightly doped drain (LDD) structures, electrostatic discharge (ESD) has become a main reliability concern for integrated circuits (ICs) in sub-quarter-micron CMOS technology [1]–[5]. To withstand a reasonable ESD stress (typically, ±2 kV in the human-body-model [6] ESD event) for safe production, on-chip ESD protection circuits have to be added into the IC products. A typical whole-chip ESD protection design had been developed, which is redrawn in Fig. 1 [7]. The MOSFETs and diodes are usually used as the ESD clamp devices to discharge ESD current, so the ESD protection capability is decided by the ESD robustness of these clamp devices.

In order to enhance the ESD robustness of these clamp devices, some ESD implantations had been reported for inclusion into the process flow to modify device structures for ESD protection [8]–[13]. The N-type ESD implantation was used to cover the LDD peak structure and to make a deeper junction in nMOS devices for ESD protection [8], [9]. The P-type ESD implantation, located under the drain junction of the nMOS devices, was used to reduce the reverse junction breakdown voltage and to allow earlier turn-on of the parasitic lateral bipolar transistor of nMOS [10], [11]. With higher doping concentrations, the P-type ESD implantation can also be used to reduce the reverse junction breakdown voltage of the diode or field-oxide device and to promote a higher ESD robustness under reverse-biased conditions [12]. Moreover, both of the N-type and P-type ESD implantations were used in nMOS devices to yield a higher ESD robustness [13]. Although there were some U.S. patents issued that claim these process methods for producing such different ESD implantations, the experimental comparison among these different ESD implantations for ESD protection in the same CMOS process was never reported in the literature before.

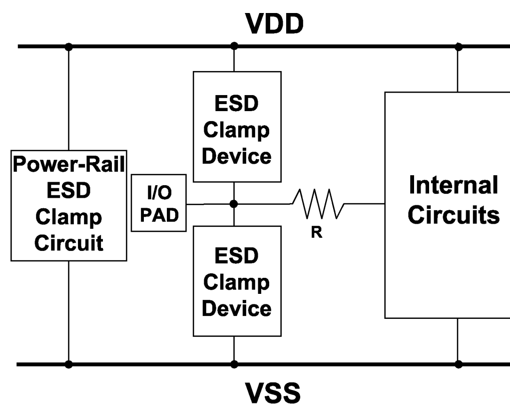

Fig. 1. Typical on-chip ESD protection design for input/output (I/O) pad with power rail ESD clamp circuit.

In this work, the ESD robustness of nMOS devices and diodes with different ESD implantation solutions in a 0.18-μm 1.8 V/3.3 V salicided CMOS process is investigated [14]. The layout dependence on nMOS devices and diodes with these ESD implantations is also investigated for optimizing on-chip ESD protection design.

II. MOSFET With Different ESD Implantations

For general ESD protection design in integrated circuits, the nMOS device drawn with multiple fingers is usually used as the ESD clamp device. In this section, four types of multifinger gate-grounded nMOS (GGNMOS) in a 0.18-μm salicided CMOS process with different ESD implantations are

Manuscript received April 9, 2003; revised December 30, 2004.

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Digital Object Identifier 10.1109/TSM.2005.845100

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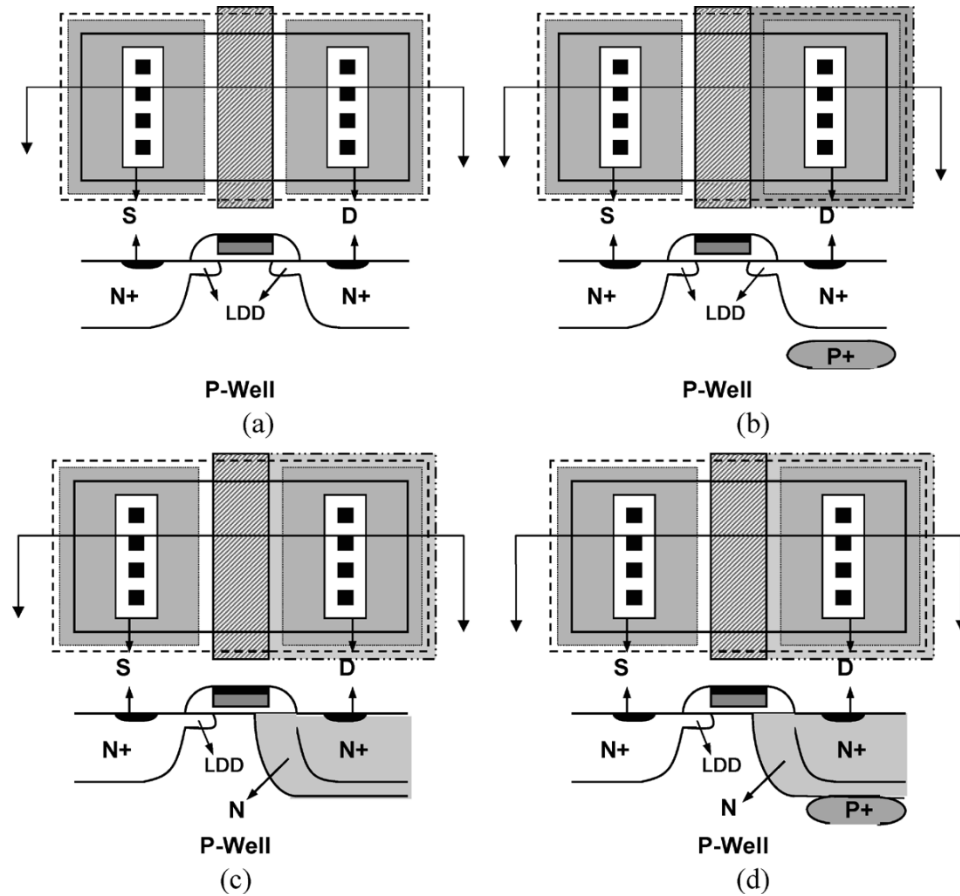

Fig. 2. Layout top view and the device cross-sectional view of (a) device A (normal nMOS without ESD implantation), (b) device B (nMOS with boron ESD implantation), (c) device C (nMOS with arsenic ESD implantation), and (d) device D (nMOS with both boron and arsenic ESD implantations).

studied. The dependences of ESD robustness of GGNMOS and gate-VDD pMOS on the device dimensions are also studied.

A. Device Structures With Different ESD Implantations

The layout top view and device cross-sectional view of four types of multifinger gate-grounded nMOS structures with different ESD implantations are shown in Fig. 2, where the additional silicide-blocking mask is used to remove $CoSi_2$ at both source and drain regions to enhance ESD robustness of GGNMOS. The device A in Fig. 2(a) is the normal nMOS device without ESD implantation. In the device B in Fig. 2(b), the boron (B) is used for the P-type ESD implantation under the drain of the nMOS device. The P-type ESD implantation located under the drain junction of nMOS is used to reduce the reverse junction breakdown voltage, and for earlier activation of the parasitic lateral BJT of the nMOS for ESD protection. In the device C in Fig. 2(c), the arsenic (As) is used for the N-type ESD implantation at the drain of the nMOS device. The N-type ESD implantation is used to cover the LDD peak structure, and to make a deeper junction in the nMOS device for ESD protection. The previous study had shown that the nMOS device with As-implanted N-type LDD has a higher ESD robustness than that with phosphorus (P)-implanted N-type LDD [15]. Therefore, arsenic is chosen for N-type ESD implantation in this study to get a better ESD level. In the device D in Fig. 2(d), the N-type arsenic ESD implantation and the P-type boron ESD implantation are both used at the drain of the nMOS device to promote a higher ESD robustness. The channel width (W) and channel length (L) of the four types of GGNMOS devices in this study are 480 and 0.5 μm, respectively. The process features of this 0.18-μm 1.8 V/3.3 V salicided bulk CMOS technology with different ESD implantations are summarized in Table I. The doping dose of the boron ESD implantation is 5E13 atoms/cm^2 and the implant energy is 80 keV. The doping dose of the arsenic ESD implantation is 1E15 atoms/cm^2 and the implant energy is 60 keV.

B. Experimental Results

A curve tracer (Tektronix Model TEK370) is used to measure the dc current–voltage (I–V) curves of devices for investigating the p/n junction breakdown voltage (V_b), the trigger voltage (V_{t1}) of the parasitic lateral bipolar transistor, and the holding voltage (V_h) of the snapback breakdown. The second breakdown current (I_{t2}) and voltage (V_{t2}) are measured by the transmission line pulse generator (TLPG) with a pulsewidth of 100 ns to verify the ESD robustness of devices [16]. The ESD failure criterion of devices is defined as the leakage current greater than 1 μA under the specified VDD bias. The PS-mode (positive-to-VSS) human-body-model (HBM) ESD level and machine-model (MM) ESD level are measured by an ESD simulator (*Zapmaster*) to compare the ESD robustness of these test devices under the HBM and MM ESD stresses.

The measured dc I–V curves of the four GGNMOS devices with different ESD implantations are shown in Fig. 3. The p/n

TABLE I
PROCESS FEATURES OF THE 0.18-μm SALICIDED CMOS PROCESS WITH DIFFERENT ESD IMPLANTATIONS

Gate Oxide Thickness (tox) for 3.3V N(P)MOS	68Å
Gate Oxide Thickness (tox) for 1.8V N(P)MOS	32Å
P-Type (B) ESD Implantation Concentration	5E13 atoms/cm^2
Energy of P-Type (B) ESD Implantation	80keV
N-type (As) ESD Implantation Concentration	1E15 atoms/cm^2
Energy of N-type (As) ESD Implantation	60keV
N-Well (P) Implantation	First: 700keV 3E13 atoms/cm^2 Second: 60keV 1.5E12 atoms/cm^2
P-Well (B) Implantation	First: 300keV 3E13 atoms/cm^2 Second: 60keV 8E12 atoms/cm^2
Silicide	$CoSi_2$

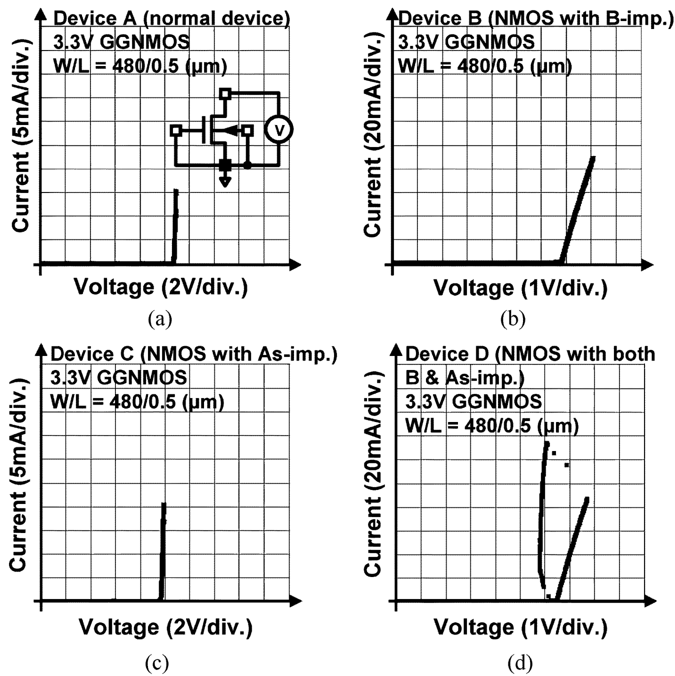

Fig. 3. Measured dc I–V curves for (a) device A, (b) device B, (c) device C, and (d) device D, under gate-grounded condition.

junction breakdown voltage (V_b) is defined as the voltage at which the current is 1 mA. The comparison of V_b among the four devices with different ESD implantations is shown in Fig. 4. The V_b is 10.4 V for device A, and can be reduced to 6.9 V for

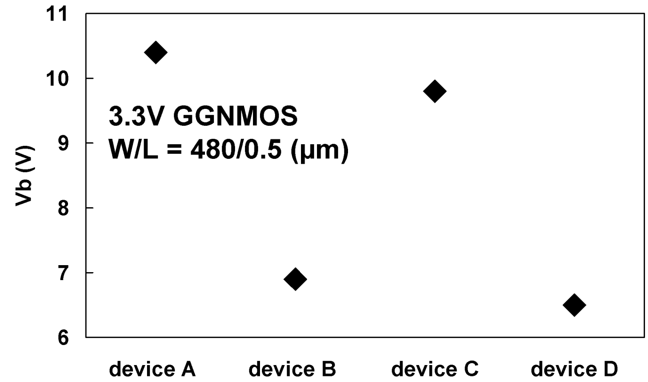

Fig. 4. Comparison of V_b (at $I = 1$ mA) among the four devices with different ESD implantations where the four devices (A, B, C, and D) have the same W/L of 480 μm/0.5 μm.

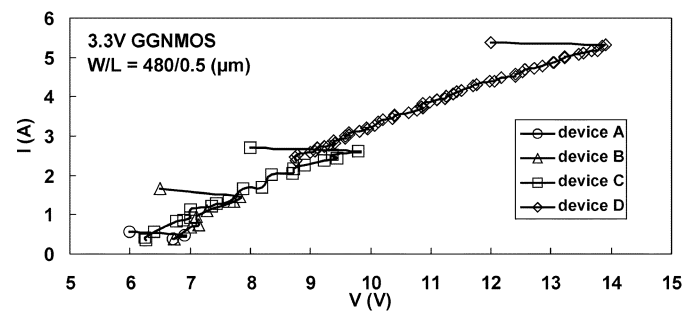

Fig. 5. TLPG-measured I–V curves of the four gate-grounded nMOS with different ESD implantations.

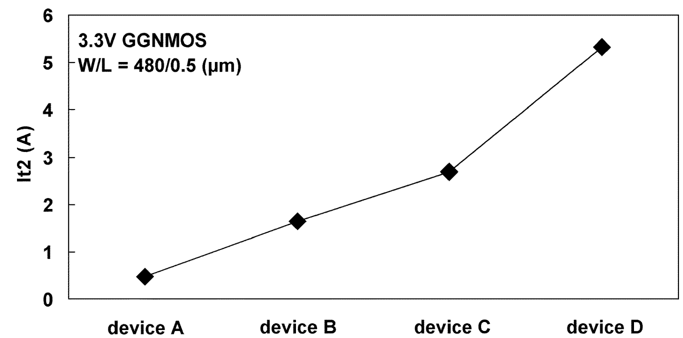

Fig. 6. Comparison of I_{t2} among the four GGNMOS devices with different ESD implantations.

device B using the boron ESD implantation and 9.8 V for device C by using the arsenic ESD implantation. The V_b and the holding voltage (V_h) of the device D with both ESD implantations are 6.5 and 5.96 V, respectively. In Fig. 3(d), the nMOS with both boron and arsenic ESD implantations shows an obvious snapback region. From the experimental results, the p/n junction breakdown voltage of the nMOS transistor can effectively be reduced by using the boron ESD implantation.

The TLPG-measured I–V curves of the four devices are shown in Fig. 5, and the I_{t2} of the four devices are compared in Fig. 6. For the GGNMOS devices without ESD implantation (device A), the I_{t2} is 0.48 A and V_{t2} is 6.68 V. For boron ESD implantation used in device B, the I_{t2} increases to 1.65 A and V_{t2} is 7.18 V. When the arsenic ESD implantation is used in device C, the I_{t2} becomes 2.7 A and V_{t2} becomes 9.33 V. When both boron and arsenic ESD implantations are used in device

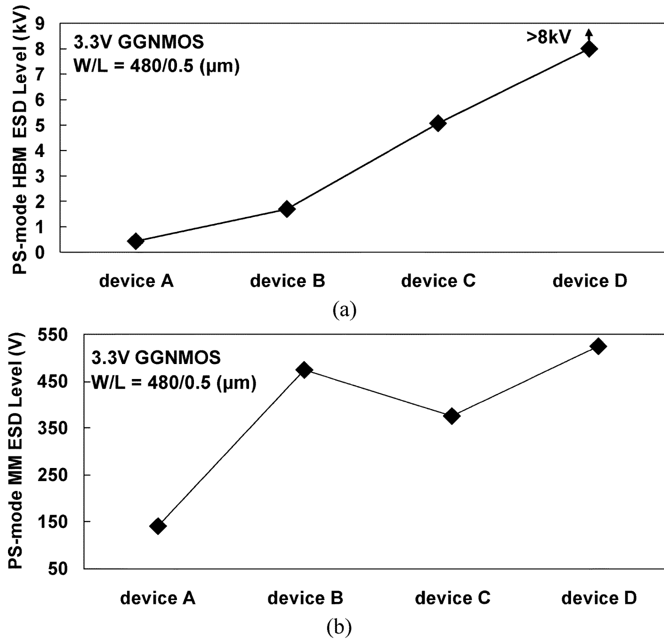

Fig. 7. PS-mode (a) HBM ESD level and (b) MM ESD level of the four GGNMOS devices with different ESD implantations.

D, the I_{t2} increases up to 5.33 A and V_{t2} is 12.76 V. This result demonstrates the effectiveness of different ESD implantations for ESD protection. Device D with both boron and arsenic ESD implantations shows an obvious improvement in second breakdown current.

Fig. 7(a) and (b) shows the HBM and MM ESD levels of the four devices under the positive-to-VSS (PS-mode) ESD stress condition. All four devices are fabricated with W/L of 480 μm/0.5 μm in the testchip. For device A without any ESD implantation, the HBM ESD level is only 0.5 kV and the MM ESD level is 120 V. When the boron ESD implantation is used in device B, the HBM ESD level increases to 2 kV and the MM ESD level increases to 500 V. When the arsenic ESD implantation is used in device C, the HBM ESD level becomes 5 kV and the MM ESD level becomes 400 V. When both boron and arsenic ESD implantations are used in device D, the HBM ESD level increases up to greater than 8 kV and the MM ESD level increases up to 550 V. From the experimental results, the ESD implantations show significant improvement in HBM and MM ESD levels of GGNMOS devices, especially for device D with both boron and arsenic ESD implantations.

C. GGNMOS and Gate-VDD pMOS Devices With Different Channel Length

In an earlier study on a 0.35-μm CMOS process [17], GGNMOS devices with short channel lengths have a higher ESD robustness. However, for the 0.25-μm CMOS process, the dependence of the ESD robustness on channel length is reversed because the melting volume of GGNMOS devices are probably too small for short channel devices [18], [19]. In order to optimize the ESD robustness of the GGNMOS and gate-VDD pMOS devices using 0.18-μm salicided CMOS technology, the dependence of ESD level on channel length is a major concern. The GGNMOS and gate-VDD pMOS devices with

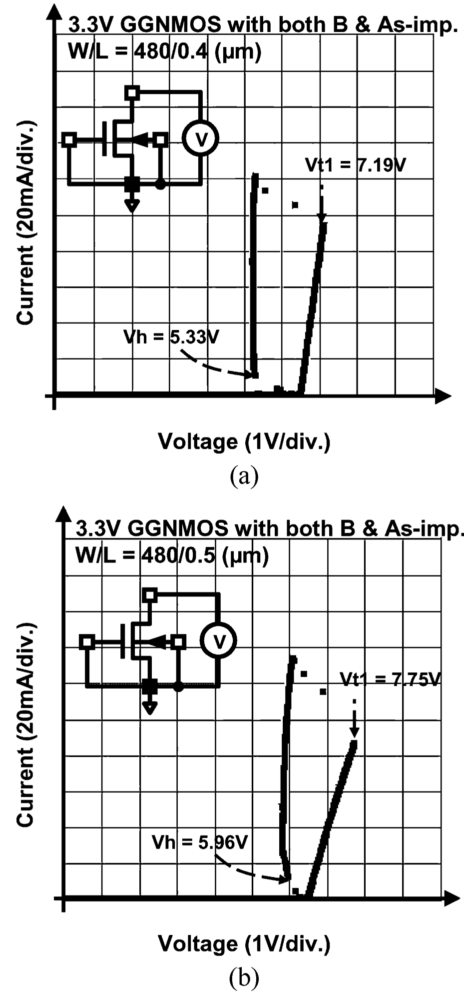

Fig. 8. Measured dc I–V curves of the fabricated 3.3-V GGNMOS with (a) $L = 0.4$ μm, and (b) $L = 0.5$ μm. The total channel width is 480 μm.

different channel lengths and different gate-oxide thickness (1.8 or 3.3 V) are fabricated in the testchip for investigation.

The dc I–V curves of the 3.3-V GGNMOS devices with channel lengths of $L = 0.4$ μm and $L = 0.5$ μm are shown in Fig. 8(a) and (b), respectively. Both GGNMOS devices are fabricated with total channel width of 480 μm in the testchip. The boron and arsenic ESD implantations are used in these two GGNMOS devices. In Fig. 8(a), the V_{t1} is 7.19 V and V_h is 5.33 V for the nMOS with $L = 0.4$ μm. In Fig. 8(b), the V_{t1} is 7.75 V and V_h is 5.96 V for the nMOS with $L = 0.5$ μm. From the dc I–V characteristics, the V_{t1} and V_h are decreased when the channel length is decreased. Therefore, the turn-on efficiency of the parasitic lateral BJT in the nMOS device can be improved when the channel length is decreased. The dc I–V curves of the 3.3-V gate-VDD pMOS device with different channel lengths of $L = 0.45$ μm and $L = 0.6$ μm are shown in Fig. 9(a) and (b), respectively. Both of the two gate-VDD pMOS devices are fabricated with the same total channel width of 480 μm in the testchip. The ESD implantation is not used in these two gate-VDD pMOS devices. Because of the poor turn-on efficiency of the parasitic lateral BJT in the pMOS device, there is no obvious snapback after drain breakdown. In Fig. 9(a), the V_b is -8.35 V for the pMOS device with $L = 0.45$ μm. In Fig. 9(b), the V_b is -8.57 V for the pMOS

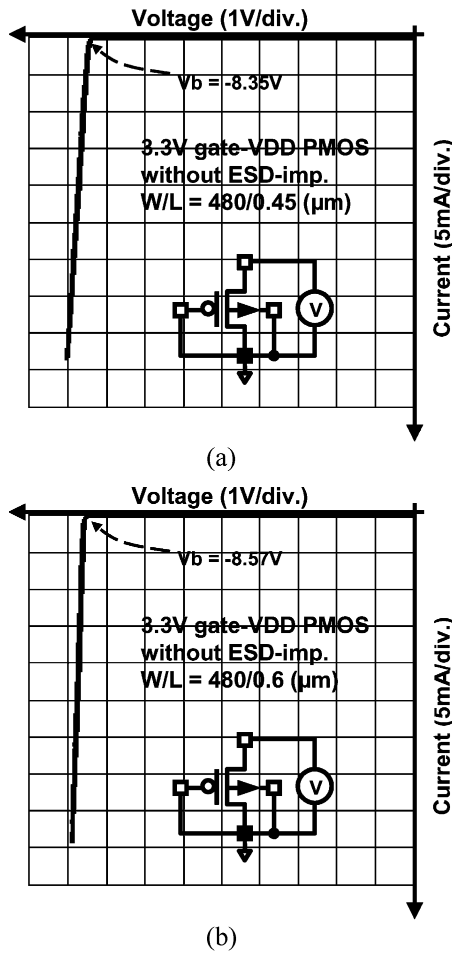

Fig. 9. Measured dc I–V curves of the fabricated 3.3-V gate-VDD pMOS with (a) $L = 0.45$ μm, and (b) $L = 0.6$ μm. The total channel width is 480 μm.

device with $L = 0.6$ μm. From the dc I–V characteristics, the V_b is decreased slightly when the channel length is decreased.

The dependence of I_{t2}, HBM ESD level, and MM ESD level on the channel length of GGNMOS and gate-VDD pMOS devices are shown in Fig. 10(a)–(c), respectively. The 3.3-V GGNMOS devices have both boron and arsenic ESD implantations but the 1.8-V GGNMOS devices have only the boron ESD implantation. There are no ESD implantation in the 1.8- and 3.3-V gate-VDD pMOS devices. The total channel width is 480 μm for each device. From the experimental results, the I_{t2} is reduced from 5.5 to 3.9 A with the channel length from 0.6 to 0.4 μm in the 3.3-V gate-grounded nMOS device. With the 1.8-V gate oxide, the GGNMOS with $L = 0.18$ μm has a higher ESD robustness than that with longer channel length because the turn-on efficiency and performance of the parasitic lateral bipolar transistor in the GGNMOS device with shorter channel length is significantly improved. For the 1.8- and 3.3-V gate-VDD pMOS devices, the HBM and MM ESD robustness have not obviously changed when the channel length is reduced from 0.33 to 0.18 μm and from 0.6 to 0.35 μm, respectively, as shown in Fig. 10(b) and (c). Therefore, the 1.8-V GGNMOS, 1.8-V gate-VDD pMOS, and 3.3-V gate-VDD pMOS devices can be drawn with minimum channel length to sustain the highest ESD robustness in this 0.18-μm salicided CMOS technology. The channel length of the 3.3-V GGNMOS device

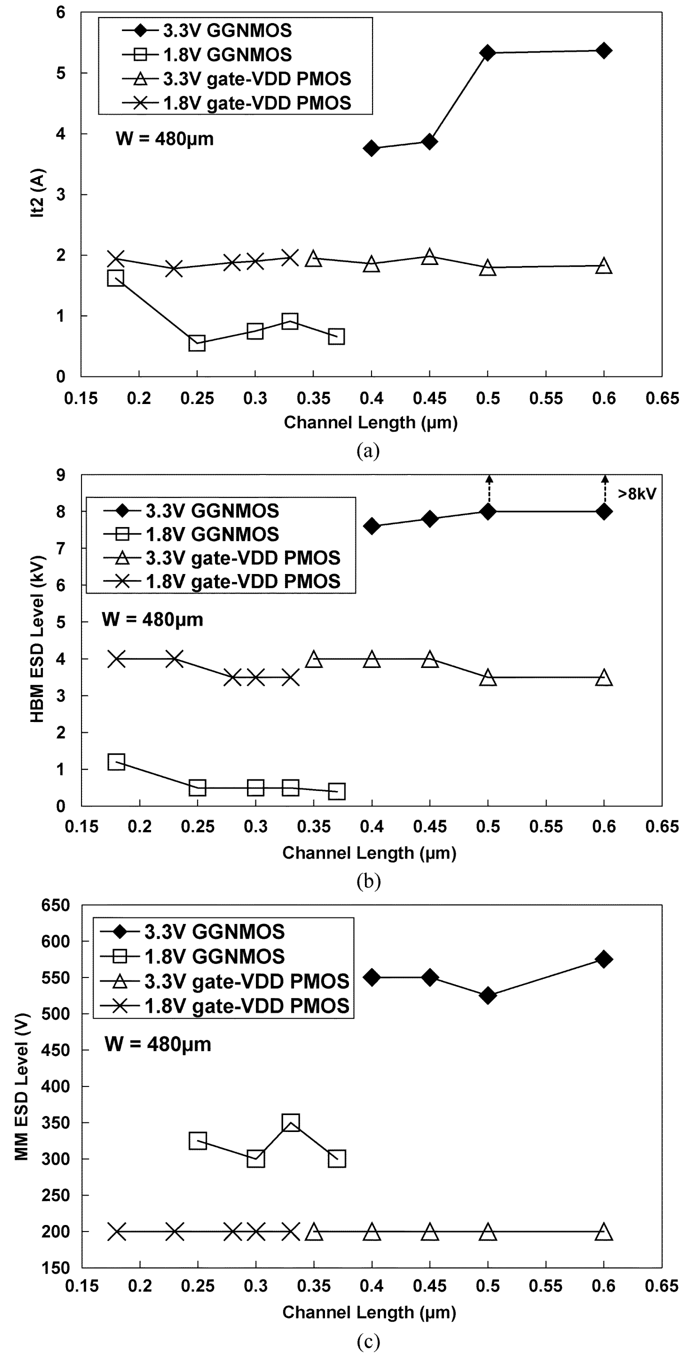

Fig. 10. Dependence of (a) I_{t2}, (b) HBM ESD level, and (c) MM ESD level on the channel length of GGNMOS and gate-VDD pMOS devices with different gate oxide thicknesses (1.8 or 3.3 V).

is optimized for best ESD robustness at 0.5 μm from this experimental result.

D. GGNMOS and Gate-VDD pMOS Devices With Different Total Channel Width

If the multifinger MOSFET can be uniformly turned on, the ESD robustness of the device is proportional to the total channel width (W) of the device. Therefore, the ESD robustness of the device can be improved by increasing the total channel width (W). In order to study the turn-on uniformity of GGNMOS and gate-VDD pMOS devices for this 0.18-μm salicided CMOS

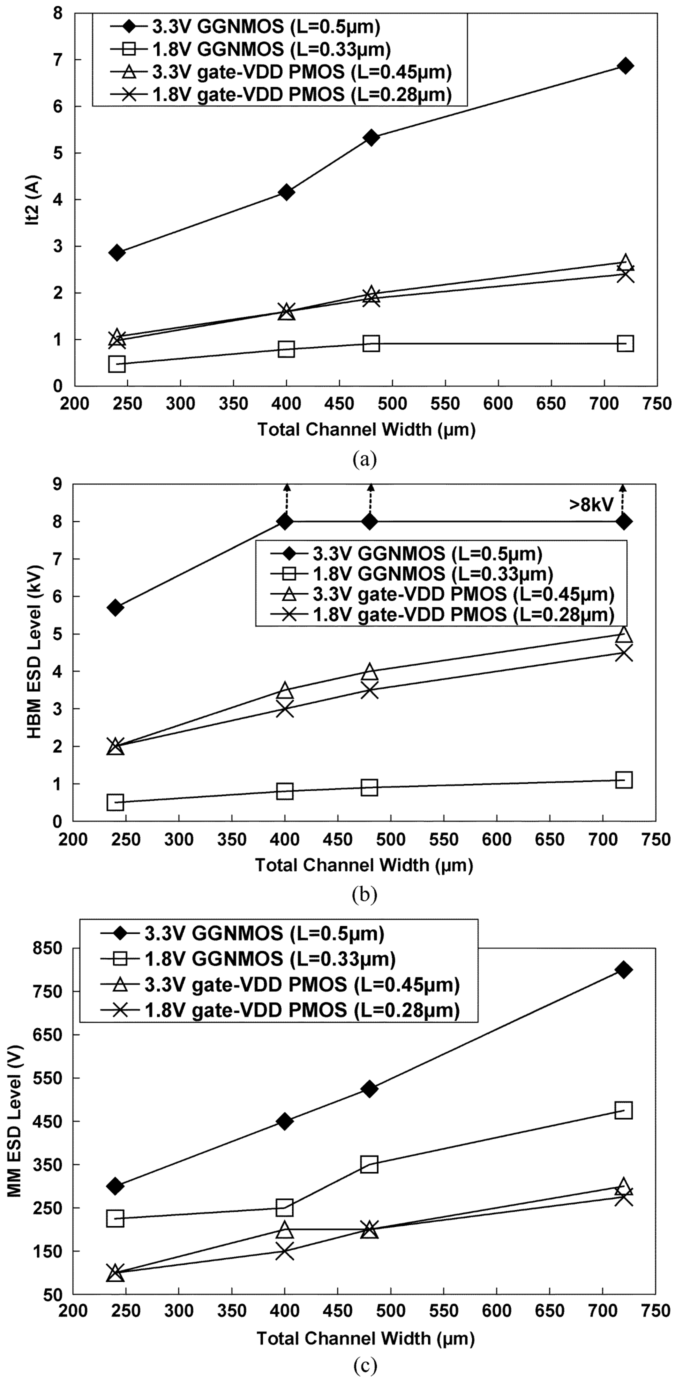

Fig. 11. Dependence of (a) I_{t2}, (b) HBM ESD level, and (c) MM ESD level on the total channel width of GGNMOS and gate-VDD pMOS devices with different gate oxide thicknesses (1.8 or 3.3 V).

technology, the dependence of ESD level on total channel width is investigated. The GGNMOS and gate-VDD pMOS devices with different total channel widths and different gate-oxide thicknesses (1.8 or 3.3 V) are fabricated in the testchip for investigation.

The I_{t2}, HBM ESD level, and MM ESD level of the GGNMOS and gate-VDD pMOS devices with different total channel width are shown in Fig. 11(a)–(c), respectively. The unit finger width is 20 μm for each device. Different finger numbers of 12, 20, 24, and 36 were drawn to have different total channel width of 240, 400, 480, and 720 μm, respectively. The 3.3-V GGNMOS devices have both boron and arsenic ESD implantations but the 1.8-V GGNMOS devices have only the boron ESD implantation. There are no ESD implantation in the 1.8- and 3.3-V gate-VDD pMOS. The channel length in this study of the 1.8-V GGNMOS, 3.3-V GGNMOS, 1.8-V gate-VDD pMOS, and 3.3-V gate-VDD pMOS devices are 0.33, 0.5, 0.28, and 0.45 μm, respectively. In Fig. 11, the 1.8-V GGNMOS with $W = 720$ μm has a low ESD level due to the nonuniform turn-on behavior of the GGNMOS device among its multiple fingers. Therefore, a gate-driven or substrate-triggered technique [20] is used to enhance the turn-on uniformity of the nMOS device with multiple fingers for ESD protection in this 0.18-μm salicided CMOS technology. The issues of nonuniform turn-on for 1.8- and 3.3-V gate-VDD pMOS devices are not as serious as that for GGNMOS devices in Fig. 11 because the pMOS device does not have an obvious snapback phenomenon after drain breakdown.

III. Diode With ESD Implantation

The diodes can be used as a forward diode string or a reverse breakdown device for on-chip ESD protection design. With a higher doping concentration, the P-type ESD implantation can also be used to reduce the reverse junction breakdown voltage of the diode or field-oxide device and to sustain a higher ESD robustness under reverse-biased conditions. In this section, ESD robustness of the normal P-type diode (P^+/N-well diode, Dp), normal N-type diode (N^+/P-well diode, Dn), and N-type diode with P-type boron ESD implantation (Dn with B-imp.) under forward- and reverse-biased stress conditions in this 0.18-μm salicided CMOS process are studied. The dependences of ESD robustness of these diodes on the device dimensions are also studied.

A. Device Structures of the Diodes

The layout top view and the device cross-sectional view of the diodes with different p/n junctions are shown in Fig. 12, where the additional silicide-blocking mask is used to remove the silicide on the p/n diffusion of the diode, thus overcoming the shallow trench isolation (STI) boundary issue on the diode structure [21]. The P^+/N-well diode shown in Fig. 12(a) is called the normal P-type diode (Dp), the N^+/P-well diode shown in Fig. 12(b) is called the normal N-type diode (Dn), and the N^+/P^+ diode shown in Fig. 12(c) is called as the N-type diode with boron ESD implantation (Dn with B-imp.).

The power consumption generated by ESD current through the device can be calculated as follows:

$$\text{Power} = I_{\text{ESD}} \times V_{\text{op}} = I_{\text{ESD}}^2 \times R_{\text{op}} \tag{1}$$

where

I_{ESD} ESD current through the device, which depends on ESD voltage source;

V_{op} operating voltage of the device under ESD stress;

R_{op} operating resistance of the device under ESD stress.

When the diode is under a reverse-biased condition, it typically has a junction breakdown voltage of 10–11 V. For such

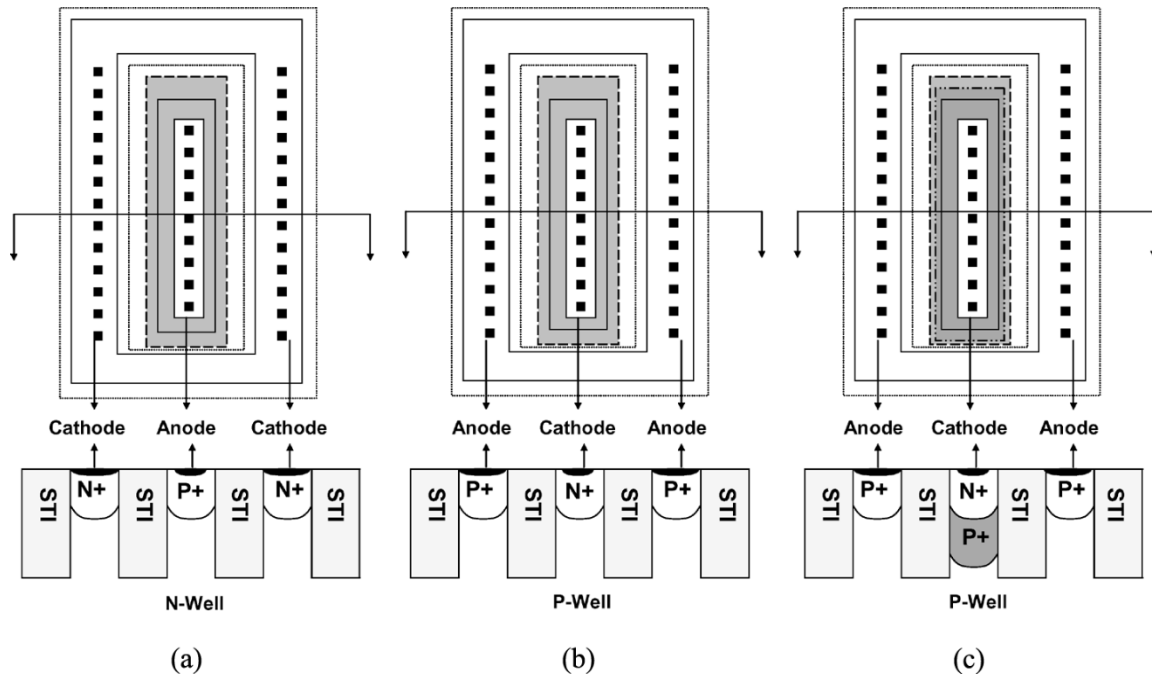

Fig. 12. Layout top view and the device cross-sectional view of (a) normal P-type diode (Dp), (b) normal N-type diode (Dn), and (c) N-type diode with boron ESD implantation (Dn with B-imp.).

a high operating voltage injecting ESD current through the device, a much larger power is generated at the diode junction to burn out the diode. In order to solve this problem, the P-type boron ESD implantation with a higher doping concentration is added at the cathode to reduce the reverse junction breakdown voltage of the diode and to sustain higher ESD robustness under the reverse-biased condition. In this study, the three diodes shown in Fig. 12 with the same total junction perimeter (P_t) of 120 μm are fabricated in the testchip for investigation in the 0.18-μm salicided CMOS process.

B. Experimental Results

The dc I–V characteristics of the three diodes under reverse-biased conditions are shown in Fig. 13(a)–(c). The doping dose of the boron ESD implantation is 5E13 atoms/cm^2 and the implant energy is 80 keV. The breakdown voltages (V_b) of the three diodes are also indicated in Fig. 13. The breakdown voltage (V_b) is measured as the voltage when the current is 1 mA. From the measured results, the additional boron ESD implantation can effectively reduce the reverse junction breakdown voltage from 11.7 V [in Fig. 13(b)] to only 6.1 V [in Fig. 13(c)]. With a lower operating voltage, the power and heat under reverse-biased PS-mode (positive-to-VSS) ESD stress conditions can be reduced with the same ESD current. Therefore, the diode with the boron ESD implantation is expected to have a higher ESD robustness.

The TLPG-measured I–V curves of the three diodes under reverse-biased conditions (ND-mode (negative-to-VDD) for P-type diode and PS-mode for N-type diode) are shown in Fig. 14. All three diodes have the same total junction perimeter (P_t) of 120 μm. For the normal P-type diode (Dp) without any ESD implantation, the I_{t2} is 0.29 A and V_{t2} is 20.95 V. For the normal N-type diode (Dn) without any ESD implantation, the I_{t2} is only 0.19 A and V_{t2} is 29.59 V. When the P-type boron ESD implantation is added at the cathode of Dn, the I_{t2} increases up to 0.24 A and V_{t2} is 23.04 V. The I_{t2} of Dn with and without boron ESD implantation under PS-mode ESD stress condition is compared in Fig. 15. The I_{t2} of the N-type diode (Dn) with boron (B) ESD implantation is increased to 126% of the normal N-type diode (Dn). This experimental result verifies the effectiveness of boron ESD implantation on N-type diodes for ESD protection under reverse-biased conditions.

Fig. 16 shows the HBM ESD level of the N-type diode. Under PS-mode ESD stress, the normal N-type diode is operated in the reverse-biased condition to discharge ESD current. Under NS-mode (negative-to-VSS) ESD stress, the normal N-type diode is operated in the forward-biased condition to discharge ESD current. The normal N-type diode with a total junction perimeter of 120 μm under NS-mode ESD stress condition can sustain HBM ESD level greater than 8 kV, whether the boron ESD implantation is used or not. However, the normal N-type diode with a total junction perimeter of 120 μm and without boron ESD implantation has a HBM ESD level of 0.5 kV under the PS-mode ESD stress condition. When the boron ESD implantation is added at the cathode of Dn, the HBM ESD level increases to 1 kV. From the experimental results, the diodes can sustain a higher ESD level under the forward-biased stress condition than that under the reverse-biased stress condition. The N-type diode with boron ESD implantation can enhance the I_{t2} and ESD level under PS-mode stress conditions.

C. Diodes With Different Spacing From Anode-to-Cathode

The TLPG-measured I–V curves of the normal N-type diodes (Dn) with a different anode-to-cathode spacing (X)

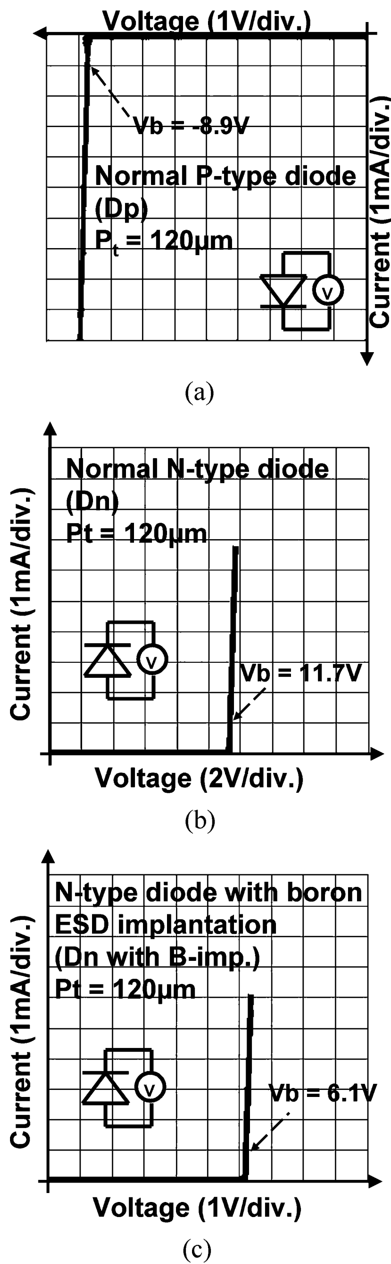

Fig. 13. Measured dc I–V curves for (a) normal P-type diode, (b) normal N-type diode, and (c) N-type diode with boron ESD implantation. The breakdown voltages (at $I = 1$ mA) are indicated.

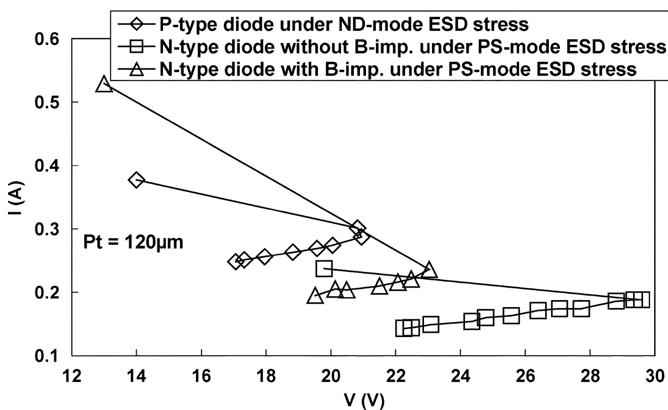

Fig. 14. TLPG-measured I–V curves of the three diodes under reverse-biased stress condition.

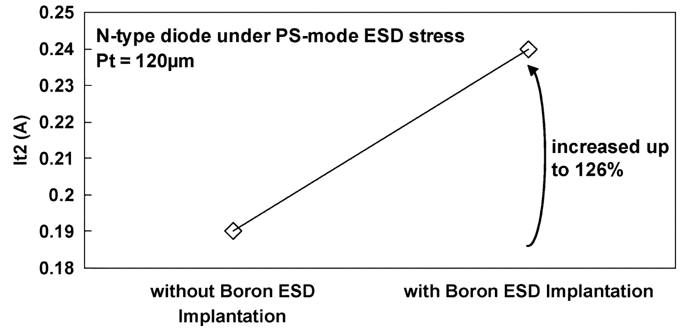

Fig. 15. Comparison on the I_{t2} of the N-type diodes with and without boron ESD implantation under PS-mode ESD stress condition.

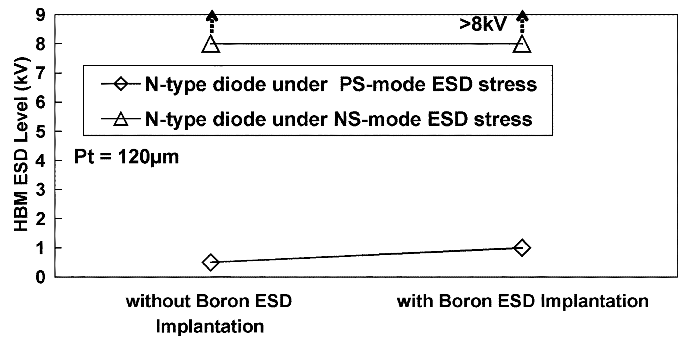

Fig. 16. HBM ESD level of the N-type diodes with and without boron ESD implantation under the PS-mode or NS-mode ESD stresses.

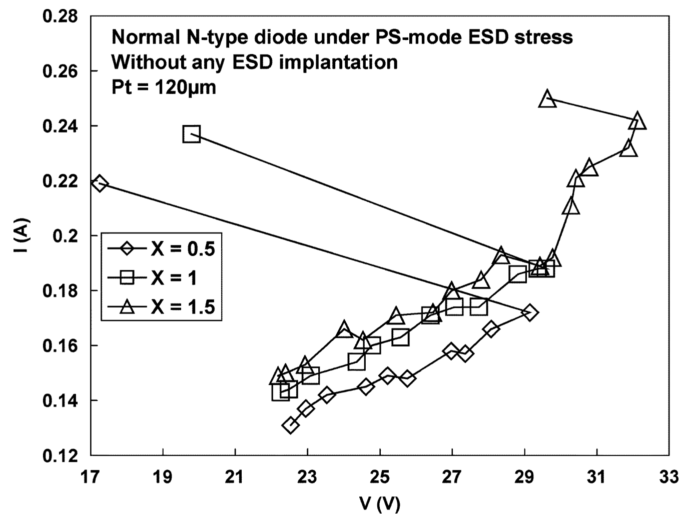

Fig. 17. TLPG-measured I–V curves of the normal N-type diodes (Dn) with different anode-to-cathode spacings under reverse-biased stress condition. All the normal N-type diodes are without boron ESD implantation.

and under reverse-biased conditions are shown in Fig. 17. All the diodes have the same total junction perimeter (P_t) of 120 μm. The boron ESD implantation is not used at the cathode of the N-type diode in this investigation. For the diode with X $=$ 0.5 μm, the I_{t2} is 0.18 A and the V_{t2} is 29 V. For the diode with X $=$ 1 μm, the I_{t2} is 0.19 A and the V_{t2} is 29.5 V. For the diode with X $=$ 1.5 μm, the I_{t2} is increased to 0.24 A and the V_{t2} is 32 V. The dependence of the I_{t2} and HBM ESD level on the anode-to-cathode spacing of the normal P-type and N-type (without boron ESD implantation) diodes are shown

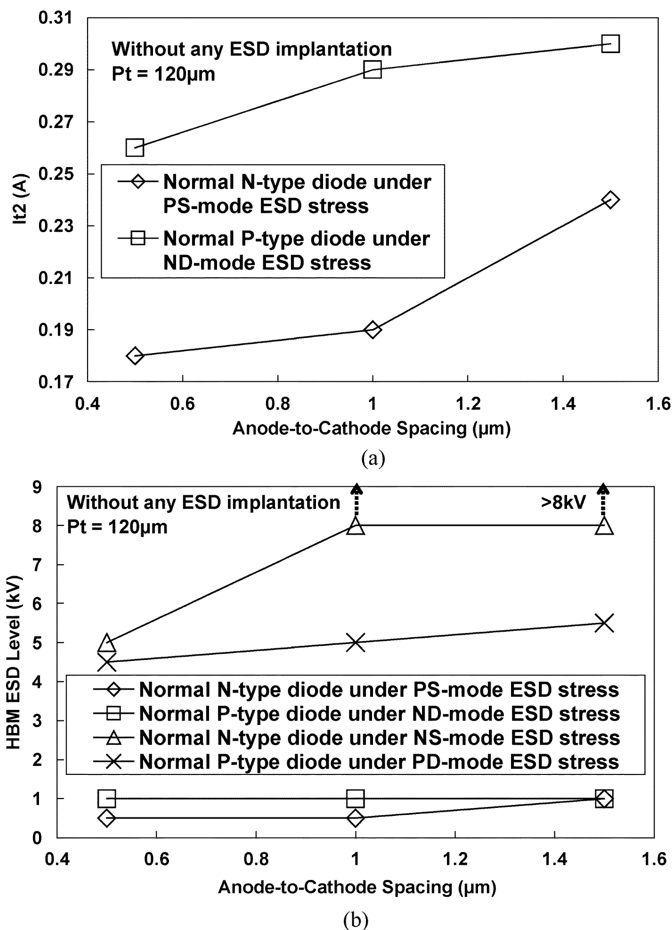

Fig. 18. Dependence of (a) I_{t2}, and (b) HBM ESD level, on the anode-to-cathode spacing of normal N-type (Dn) and P-type (Dp) diodes without any ESD implantation.

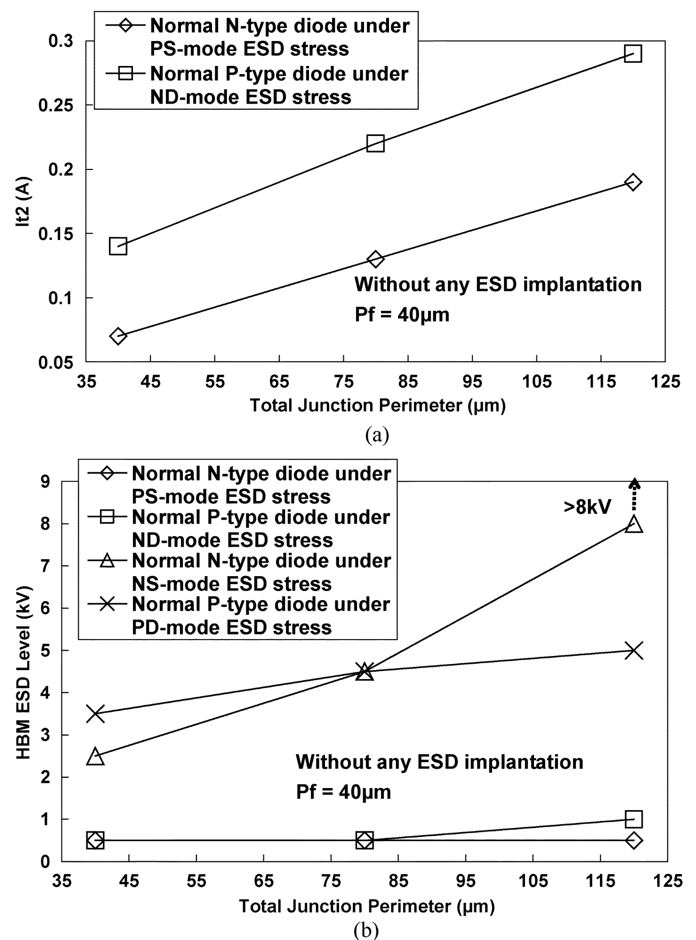

Fig. 19. Dependence of (a) I_{t2}, and (b) HBM ESD level, on the total diode junction perimeter of normal N-type (Dn) and P-type (Dp) diodes without any ESD implantation.

in Fig. 18(a) and (b), respectively. The experimental results show that the ESD robustness of the normal P-type and N-type (without boron ESD implantation) diodes under forward- and reverse-biased stress conditions are increased when the spacing from anode-to-cathode is increased. The NS-mode HBM ESD level is greater than 8 kV of the normal N-type diode, with the anode-to-cathode spacing of 1–1.5 μm in this 0.18-μm salicided CMOS technology.

D. Diodes With Different Total Junction Perimeter

The I_{t2} and ESD level of the normal P-type and N-type diodes with different total junction perimeter (P_t) are compared in Fig. 19(a) and (b), respectively. These diodes are drawn with a fixed unit finger junction perimeter of 40 μm and different finger numbers of 1, 2, and 3 to have different total junction perimeter of 40, 80, and 120 μm, respectively. The boron ESD implantation is not added at the cathode of the N-type diode in this investigation. The nonuniform turn-on issue among the multiple fingers of GGNMOS devices is not observed in diodes because there is no snapback phenomenon after reverse junction breakdown of the diodes. When the total junction perimeter of the diode is increased, the I_{t2} and HBM ESD level of the diode are almost linearly increased. From the experimental results, the NS-mode HBM ESD level of the normal N-type diode with a total junction perimeter of 120 μm is greater than 8 kV in this 0.18-μm salicided CMOS technology.

IV. Conclusion

The second breakdown current (I_{t2}) and ESD level of nMOS devices and diodes with different ESD implantations for on-chip ESD protection have been examined in a 0.18-μm 1.8 V/3.3 V salicided bulk CMOS technology. The gate-grounded nMOS devices with both boron and arsenic ESD implantations display a great improvement in ESD robustness. The effectiveness of boron ESD implantation in N-type diodes for ESD protection under a reverse-biased stress condition is also verified. From the experimental results, the additional ESD implantations in a 0.18-μm salicided CMOS technology are useful for on-chip ESD protection design. Along with the process solution, the layout considerations for the channel length of MOSFET transistors and the anode-to-cathode spacing of the diodes for ESD protection need to be optimized to obtain the highest ESD level.

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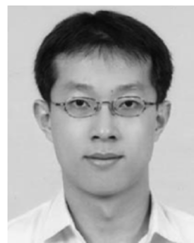

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