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Wafer bonding for high-brightness light-emitting diodes via indium tin oxide intermediate layers

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Abstract

A direct wafer-bonding technique has been used to fabricate high-brightness light emitting diodes (LEDs). However, bonding processes were usually performed at elevated temperatures, possibly causing degradation in the quality of the LED structure. In addition to this, misorientation between the two bonded wafers may have caused defects between the wafers. In this study, these two problems were solved by bonding the InGaP/GaAs and GaAs wafers with an indium tin oxide (ITO) polycrystalline film at temperatures below 650 °C. It was found that the bonding occurred mainly through the In transport from the InGaP to ITO, and that the electrical resistance decreased with the bonding temperature.
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1. Introduction

High-efficiency light-emitting diodes (LEDs) operating in the green (555 nm) through red spectral region (650 nm) have been realized employing the AlGaInP alloy system. The brightness of these LEDs was intensified using the wafer-bonding technique [1]. Using this technique, a transparent GaP wafer was bonded to an epitaxial LED structure that was grown on a GaAs substrate. After the optically absorbing GaAs substrate was removed, light extraction from the chip was significantly improved. However, there were some issues of quality that remained to be solved. First, since wafers were usually mechanically aligned using the orientation flats of the wafers, a twist misorientation between the wafers was unavoidable [2]. This twist angle caused small voids and screw dislocation networks at the interface and resulted in an increase of electrical resistance of bonded interfaces [3–5]. In addition to this, the elevated temperatures (700–1000 °C) [5], at which bonding processes were usually performed, may have degraded the quality of the LED structure.

To solve these two problems, a highly transparent conducting indium tin oxide (ITO) film was chosen as the intermediate bonding layer in this study. ITO films have been commonly prepared on substrates for various optoelectric devices, such as transparent electrodes, transparent heaters, antireflection coatings and electromagnetic shield coatings [6–9]. Since ITO is a polycrystalline film, it is unnecessary to

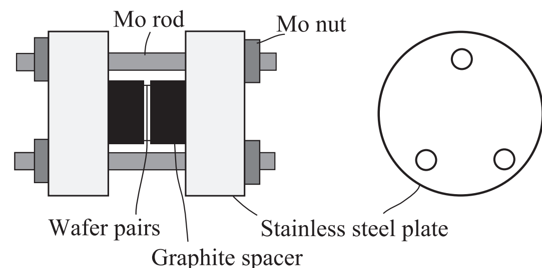

Fig. 1. Differential thermal expansion fixture for clamping the wafer pair in the bonding furnace.

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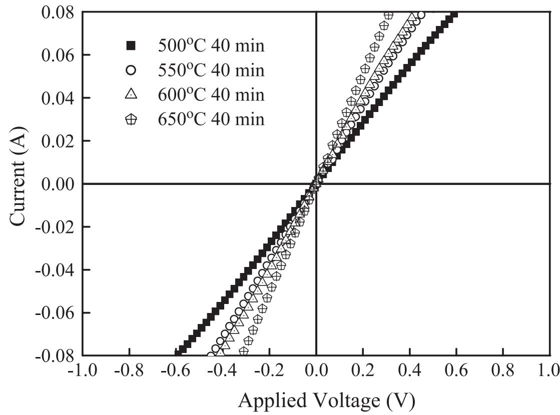

Fig. 2. Current-voltage (I–V) characteristics of wafer-bonded GaAs/$In_{0.5}Ga_{0.5}P$-ITO/GaAs interface (2×2-mm^2 die) at bonding temperatures ranging from 500 to 650 °C.

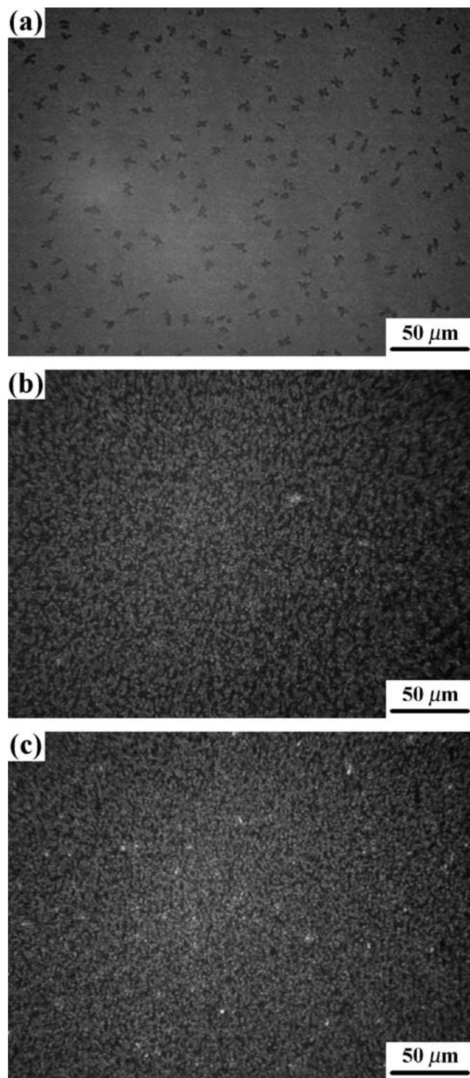

Fig. 3. IR transmission optical micrographs of the interface of GaAs/$In_{0.5}Ga_{0.5}P$-ITO/GaAs bonded at temperatures of (a) 500 °C, (b) 550 °C, and (c) 600 °C for 40 min.

align the two wafers. Therefore, the principal goal of this research has been to develop a low-temperature wafer-bonding process by using ITO film as the intermediate bonding layer.

2. Experimental details

The devices fabricated in this study were used only as demonstrators of the bonding process and were not suitable for high-brightness LEDs. However, because the goal of this study is to develop an effective bonding process, readily available wafers were chosen. Two types of substrates, n-$In_{0.5}Ga_{0.5}P$/n-GaAs and ITO/n-GaAs wafers, were used for optimization of the process. The processes involved the epitaxy of an $In_{0.5}Ga_{0.5}P$ film on one GaAs wafer and then bonding the wafer to another GaAs wafer coated with an ITO film. The $In_{0.5}Ga_{0.5}P$ epitaxial films (400 nm) were grown by metalorganic chemical vapor deposition. Before depositing, GaAs wafers were heated to 600 °C and held for several minutes in a H_2 atmosphere at a pressure of 0.1 atm. The reactants were trimethylindium (TMIn), trimethygallium (TMGa), PH_3, which were transported into the reactor by H_2 gas. The Si dopant was provided by disilane (Si_2H_6). The growth rate of $In_{0.5}Ga_{0.5}P$ epitaxial film at 800 °C was 0.46 nm/s. As for the ITO films (300 nm), they were grown by electron beam evaporator. Pellets composed of pure indium

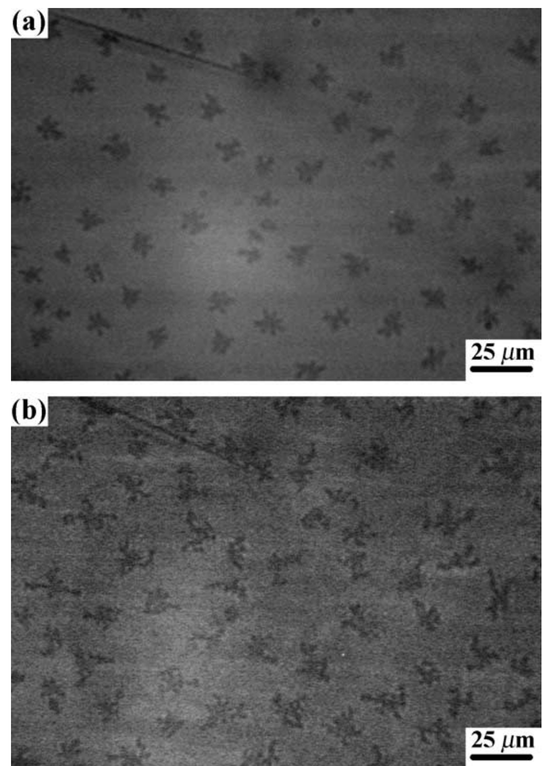

Fig. 4. IR transmission optical micrographs of the interface of GaAs/$In_{0.5}Ga_{0.5}P$-ITO/GaAs bonded at temperatures of 500 °C for (a) 1 and (b) 4 h.

oxide and tin oxide (99.99%) were used as source material. The chamber was evacuated to 5×10^{-6} Torr after loading GaAs wafers and source material. Then samples were heated to the deposition temperature (250 °C). The working pressure and O_2 flow rate were 4×10^{-4} Torr and 20 sccm, respectively. The rate of evaporation was controlled within the range of 10–12 nm/min. The atomic scale surface roughness of these $In_{0.5}Ga_{0.5}P$ coated and ITO coated wafers (over a 5×5 μm^2 area) were measured using atomic force microscopy (AFM). Both of their surfaces were very rough with typical peak-to-valley distances of 3.9 and 11.9 nm, respectively. The electric resistance of the ITO film was about 2×10^{-4} Ω-cm.

Wafers were diced into 1×1 cm^2 samples with a diamond saw and then cleaned in a clean room using a series of deionized water, acetone, isopropyl and a solution of H_2SO_4, H_2O_2 and H_2O. The cleaned samples were stacked in a differential thermal expansion fixture made of stainless steel, molybdenum and high-purity graphite [10], as shown in Fig. 1. The sample stack was clamped at room temperature with only a minimal applied compressive load. When the processing temperature increased, the compressive stress on the sample stack increased due to the differential thermal expansion between the various materials comprising the sample holder. The estimated compressive stress at the bonding temperature was about 100 Kg/cm^2 [10]. The actual stress, however, could not be determined by calculation due to the fact that both the sample stack and the holder undergo plastic deformation at elevated temperatures. Since high temperatures may destroy the LED structure, samples were bonded in argon ambient at temperatures lower than 650 °C for 40 min.

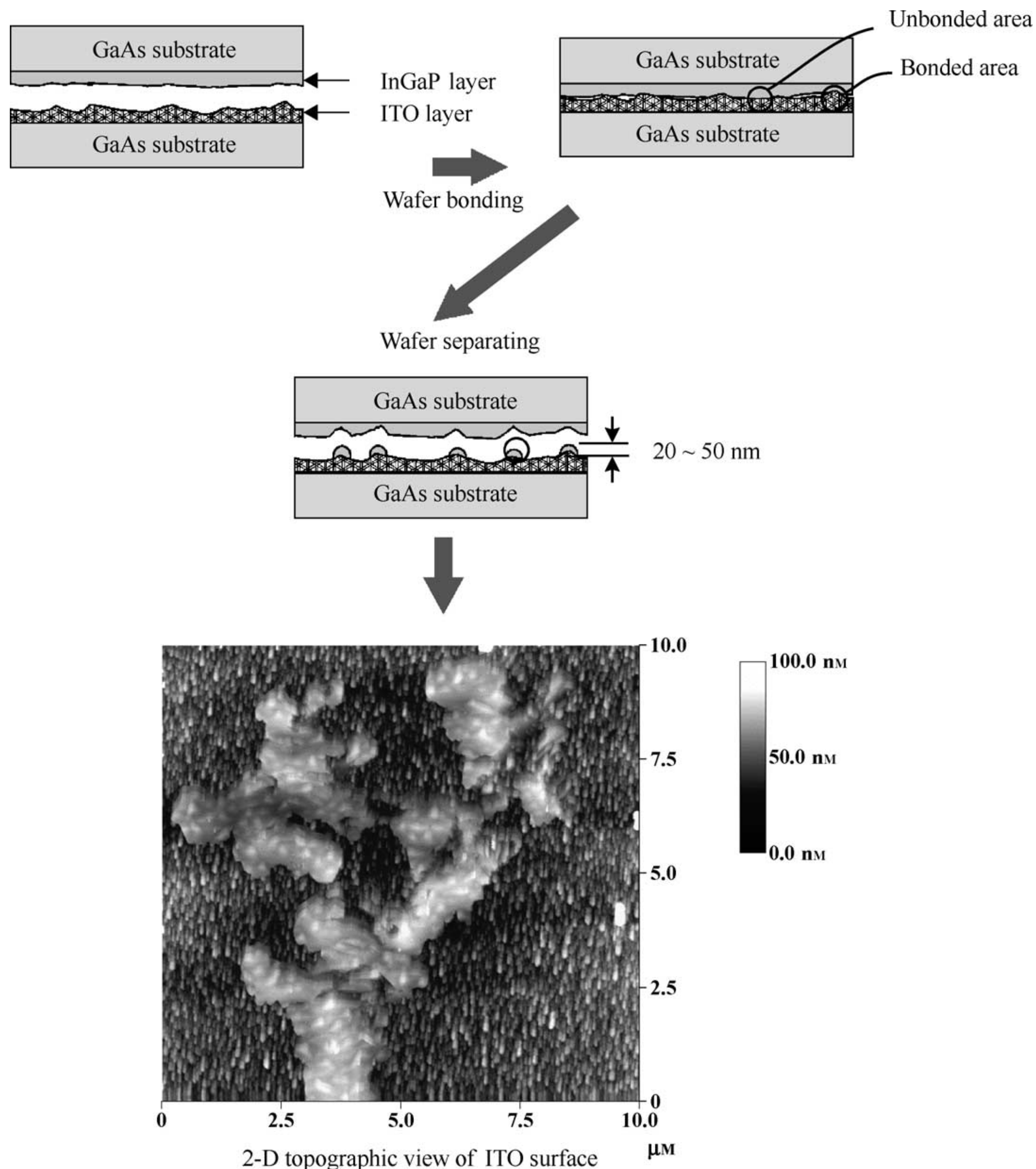

Fig. 5. Illustration of the GaAs/$In_{0.5}Ga_{0.5}P$-ITO/GaAs bonding and separating process and AFM image of the snowflake features on the ITO surface.

The exposed outer surfaces of bonded samples were then polished with #600 sandpaper and 1.0-μm diamond paste. After the samples were cleaned with DI water and isopropanol, the bonded interface was characterized using infrared (IR) transmission optical microscopy. All current-voltage (*I–V*) characteristics were measured by HP 4156B. Full-sheet alloyed ohmic contact metallizations of Au/Ge/Ni were applied to the outer surfaces of the bonded samples. The samples were then diced into 2×2-mm^2 chips and mounted onto headers for electrical testing.

3. Results and discussion

Fig. 2 shows the *I–V* characteristics of the GaAs bonded structures. The characteristics of samples bonded at temperatures below 500 °C were not shown in Fig. 2 since the samples were separated during the dicing process. The bonded structures at temperatures greater than 500 °C exhibited ohmic (linear) *I–V* characteristics. The resistance was found to decrease with the increase of bonding temperature. For a 2×2-mm^2 chip, the resistance was 7.5 Ω when the bonding temperature was 500 °C. The resistance decreased to 3.9 Ω when the bonding temperature increased to 650 °C. For the purpose of comparison, the electrical characteristics of a single GaAs wafer were also measured. It was found that the *I–V* properties of GaAs did not change much after annealing at temperatures below 650 °C. This observation suggested that, because there is no bonded interface in single wafer experiments, the decrease of the resistance of the bonded samples must have been a result of the improvement of the bonded interface.

IR transmission optical microscopy was also used to study the effects of the temperature on the bonded interface. The snowflake-like features seen in Fig. 3 correspond to the bonded areas, which were found to increase with the bonding temperature. As shown in Fig. 3, when the sample was bonded at 500 °C, few areas bonded, and many voids (unbonded areas) formed between bonded samples. As mentioned previously, the surfaces of the $In_{0.5}Ga_{0.5}P$ coated substrate and the ITO coated substrate were very rough. In other words, when samples were placed in contact with each other, the contact area ratio was very small. Therefore, the ratio of bonded areas was very low when samples were bonded at low temperature. When the temperature increased to 600 °C, most of the areas bonded because both the reaction rate and mass transport rate increased with the bonding temperature. Since the electrical conductivity increases with the bonded areas, it is not surprising that electrical resistance decreases with temperature (Fig. 2).

For the purpose of comparison, the InGaP/n-GaAs substrate was also bonded directly to the GaAs substrate (without ITO as intermediate layer) at temperatures lower than 650 °C. It was found that the qualities of the samples bonded without the ITO intermediate layer were poorer than those with ITO layer. Samples bonded at temperatures below 550 °C were separated during the dicing process. When the bonding temperature was 650 °C, the resistance was as high as 21.5 Ω, which was five times higher than that with ITO layer.

It was also found that the area of bonded snowflake-like features increased with the annealing time. As shown in Fig. 4, at 500 °C, the size of the snowflake-like features increased from 12 to 20 μm, when annealing time increased from 1 to 4 h. After the samples were separated, the morphology of the snowflake features was investigated using AFM and was schematically illustrated in Fig. 5. It is obvious that the bonded sample was separated through the InGaP layer of the snowflake-like features. The "thickness" of the snowflake-like feature was about 20–50 nm.

The composition of the snowflake was analyzed by Auger electron spectroscopy (AES). The sputtering etching rate of the composition depth profiles was about 149 Å/min. As shown in Fig. 6, the In concentration on the ITO surface of the snowflake (concave up region) was higher than that on the unannealed ITO surface. Furthermore, as shown in Fig. 7, the In concentration on the InGaP surface of the

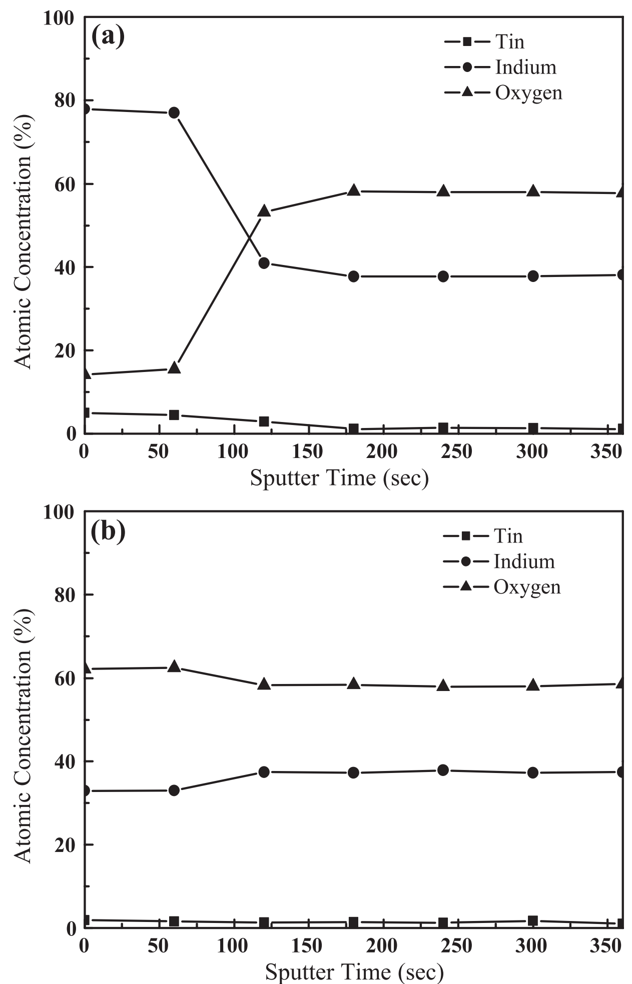

Fig. 6. AES depth profile spectra (a) at the snowflakes features on the separated ITO surface and (b) at the regions near the snowflakes features on the separated ITO surface.

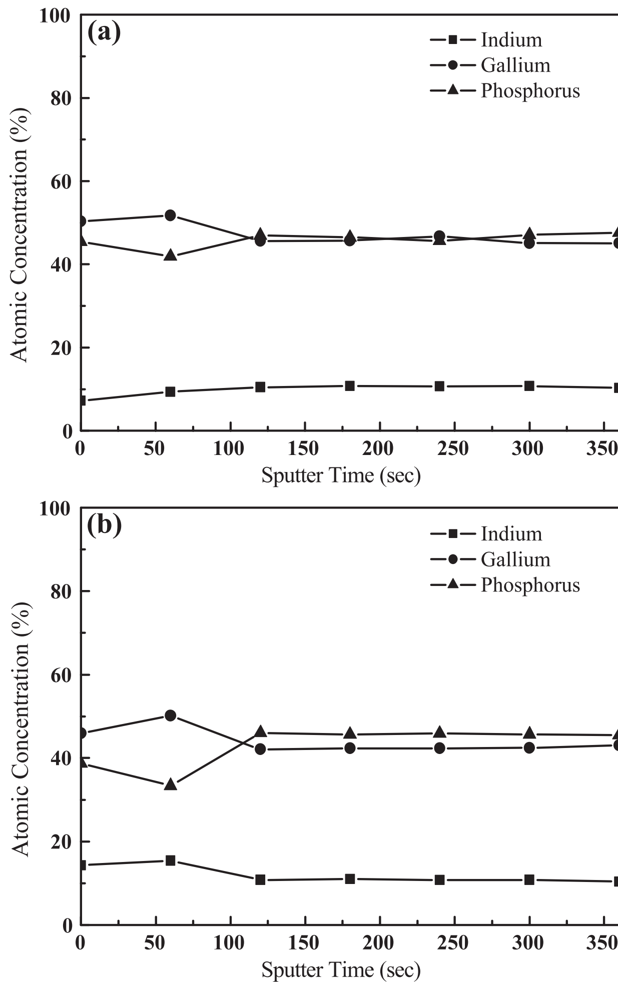

Fig. 7. AES depth profile spectra (a) at the snowflakes features on the separated $In_{0.5}Ga_{0.5}P$ surface and (b) at the regions near the snowflakes features on the separated $In_{0.5}Ga_{0.5}P$ surface.

snowflake (concave down region) was lower than that on the unannealed InGaP surface. This observation strongly suggested that the bonding mechanism between $In_{0.5}Ga_{0.5}P$/GaAs and ITO/GaAs substrates occurred mainly through the In transport from $In_{0.5}Ga_{0.5}P$ to ITO surface during bonding.

To confirm the mass transport mechanism of the samples during bonding, dot-patterned surfaces, which were used to simulate the contact areas formed between nonflat wafers, were introduced at the bonding interfaces. As shown in Fig. 8, this process involved the creation of controlled dot patterns on one wafer surface (either an ITO or an InGaP surface) by etching photolithographically generated patterns and then bonding the patterns to an unpatterned wafer. The diameter and the height of the dots are 10 μm and 50 nm, respectively, and the distance between two dots is 25 μm. Fig. 9 shows the transmission IR images of both samples bonded at 550 °C for 40 min. As shown in Fig. 9(a), the shape of the dot-patterned ITO in the bonded sample did not change much, meaning that little material flowed from the dot-patterned ITO to the unbonded interface. However, as shown in Fig. 9(b), the InGaP dot patterns in the bonded

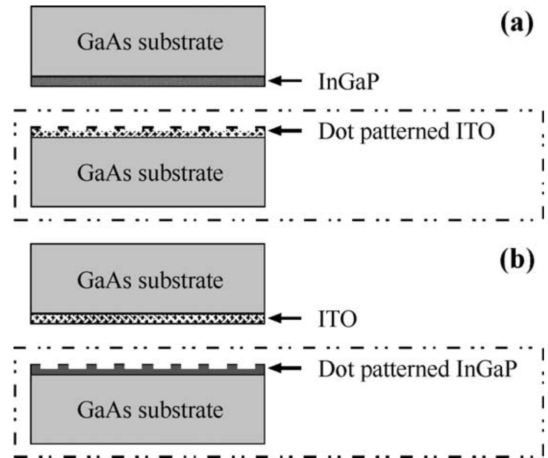

Fig. 8. Illustrations of wafer bonding process of (a) dot-patterned ITO–unpatterned $In_{0.5}Ga_{0.5}P$ bonded sample and (b) dot-patterned $In_{0.5}Ga_{0.5}P$–unpatterned ITO bonded sample.

sample disappear. Scanning acoustic microscopy was also used to confirm the disappearance of the $In_{0.5}Ga_{0.5}P$ dot patterns. After samples were allowed to anneal at 550 °C, no $In_{0.5}Ga_{0.5}P$ dot patterns were found on the bonded interface. These observations, in addition to the observations from the

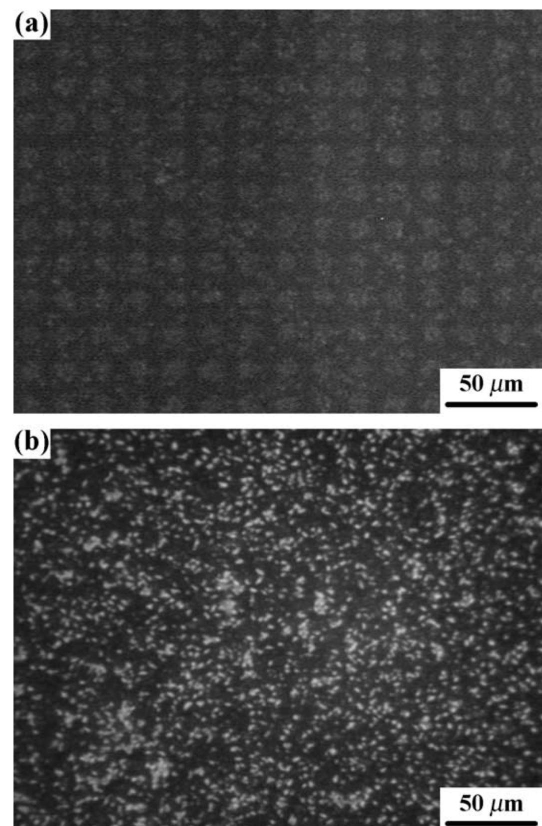

Fig. 9. IR transmission optical micrographs of (a) dot-patterned ITO–unpatterned $In_{0.5}Ga_{0.5}P$ bonded sample and (b) dot-patterned $In_{0.5}Ga_{0.5}P$–unpatterned ITO bonded sample (both samples were bonded at 550 °C for 40 min).

AES depth profiles (Figs. 6 and 7), clearly demonstrated that the bonding mechanism between $In_{0.5}Ga_{0.5}P$/n-GaAs and ITO/n-GaAs wafers were mainly through mass transport (especially In) from the $In_{0.5}Ga_{0.5}P$ to the ITO surface.

4. Summary

In this study, a highly transparent ITO film was used as an intermediate layer to bonded wafers. The investigation of the correlation between the wafer's electrical resistance and bonding mechanism to bonding temperatures has led to the development of a simple effective process for preparing bonded structures. Two types of substrates, n-$In_{0.5}Ga_{0.5}P$/n-GaAs and ITO/n-GaAs wafers, were used for process optimization. It was found that the bonding mainly occurred through the In transport from the InGaP to ITO surface. The bonded areas between wafers were found to increase with the bonding temperature, resulting in decreases of electrical resistance.

The process developed in this study involves the use of a relatively uniform pressure and moderately high temperature (650 °C) to produce optimal results. When samples were bonded at 650 °C, most of the areas were bonded, with no voids found at the bonded interface, and the resistance was only 3.9 Ω for a 2×2-mm^2 chip. Using this procedure, it was possible to fabricate bonded wafers with the electrical resistances low enough for high-brightness LEDs.

Acknowledgments

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