Available online at www.sciencedirect.com

SCIENCE DIRECT

Thin Solid Films 478 (2005) 293–298

thin solid films

www.elsevier.com/locate/tsf

Application of plasma immersion ion implantation on seeding copper electroplating for multilevel interconnection

Shao-Yu Chiu[a], Ying-Lang Wang[b,*], Shih-Chieh Chang[b], Ming-Shiann Feng[a]

[a]Institute of Materials Science and Engineering, National Chiao Tung University, Hsinchu, Taiwan, R.O.C.
[b]Taiwan Semiconductor Manufacturing Company, Ltd., Tainan, Taiwan, R.O.C.

Received 20 June 2003; accepted 5 November 2004
Available online 8 January 2005

Abstract

In this study, an effective seeding technology, plasma immersion ion implantation of palladium (PIII Pd), was proposed to achieve defect-free gap filling for copper electroplating (Cu-ECP). It was found that a threshold dosage (~5.2×10^{18} m^{-2}) of PIII Pd was required to drive Cu-ECP and the dependence of Pd dosage on the implantation time was quasi-linear. The thickness of electroplated copper films increased as the Pd dosage increased. Too high a Pd dosage caused a rough copper film with high resistivity (>10 μΩ cm) while too low a Pd dosage resulted in an insufficient nucleation site for Cu-ECP, leading to poor film adhesion. In addition, a higher substrate bias of PIII was suggested to enhance the gap-filling capability of Cu-ECP and the Cu(111) formation of electroplated copper films.
© 2004 Elsevier B.V. All rights reserved.

Keywords: Plasma immersion ion implantation (PIII); Palladium; Seed layer; Copper; Electroplating

1. Introduction

Copper has been the material of choice to replace aluminum alloys for sub-0.13-μm multilevel interconnection due to its lower resistivity and higher electromigration resistance [1,2]. In 1997, IBM (International Business Machines) reported full copper wiring of 0.25-μm complementary metal-oxide semiconductor devices, which invoked a myriad of research activities in the development of copper multilevel interconnection for ultralarge-scale integration technologies [3]. Among several deposition methods of copper, including physical vapor deposition (PVD), chemical vapor deposition, electroless and electroplating (ECP), ECP was the current method to deposit copper into Damascene features because of its lower cost, higher throughput, and superior gap-filling capability [4–9]. In the process of ECP, however, a thin and continuous seed layer was necessary to provide an effective path for electric current [8]. The quality of electroplated copper films was strongly dependent on the step coverage of seed layers. Recently, the method of palladium (Pd) activation on TaN_x barriers for autocatalytic electroless copper deposition was continuously investigated [10–12]. It offered advantages of low cost, no external power supply and good selectivity. However, difficult control of bath chemistry eliminated its practicability.

In this article, plasma immersion ion implantation of Pd (PIII Pd) was explored to be a seeding technology for copper electroplating (Cu-ECP) in semiconductor processing [13]. Compared with electroless Pd in a $PdCl_2$/HF solution, PIII Pd had advantages of no degradation, no impurity, high implantation rate and wide process window for reproducibility [14–16]. In this study, the effect of PIII-Pd seed layers on electroplated copper films was discussed.

2. Experiment

A substrate used in this study was a 6- or 8-in. silicon wafer covered with a 1.2-μm-thick thermal SiO_2 as an

* Corresponding author. Tel.: +886 6 5098069; fax: +886 6 5052081.
E-mail address: ylwang@tsmc.com (Y.-L. Wang).

0040-6090/$ - see front matter © 2004 Elsevier B.V. All rights reserved.
doi:10.1016/j.tsf.2004.11.187

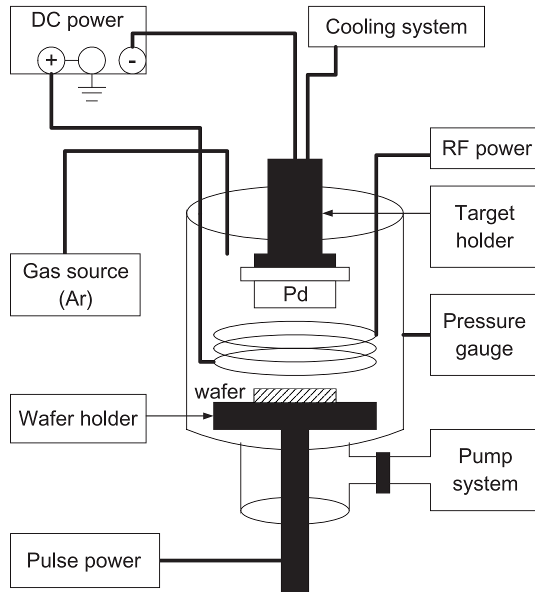

Fig. 1. Schematic of the PIII system.

interlayer dielectric. Subsequently, the dielectric film was patterned by photolithography and etched by reactive ion etching (RIE). A 50-nm-thick PVD-TaN_x layer was then deposited as an adhesion/barrier layer. Finally, a sliced wafer with a size of 2×3 cm^2 was used for PIII experiments. The dosage and implantation depth profile of PIII Pd were examined by Rutherford backscattering spectrometer and secondary ion mass spectrometry, respectively.

All ECP work was carried out in a tank of a non-conducting material. A counterelectrode was platinum and a working electrode was a wafer with size of 1×3 cm^2. A contact to the electrodes was implemented outside of an electrolyte with an alligator clip. Agitation air was introduced into the electrolyte from a compressor. The electrolyte was composed of $CuSO_4\cdot5H_2O$ (30 kg/m^3), H_2SO_4 (275 kg/m^3), chloride ions (100 ppm) and 2-mercaptopyridine (2MP) (10 ppm) [9].

X-ray diffraction (XRD) was used to investigate the crystal orientation of electroplated copper films. Surface

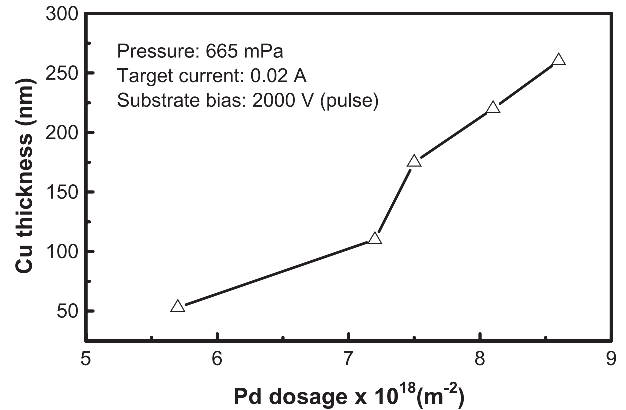

Fig. 3. Deposited Cu thickness vs. Pd dosage. The deposition time was 3 min.

morphology and step coverage were examined using a field-emission scanning electron microscope (FESEM) while a four-point probe detector was used to measure the sheet resistivity of deposited copper films.

3. Results and discussion

Fig. 1 illustrates a schematic diagram of the PIII reactor. A Pd target was bombarded by ions using a negative bias and then sputtered Pd atoms were ionized by argon inductively coupled plasma. Consequently, the Pd ions in the plasma were accelerated by a plasma sheath and implanted into a wafer by a negative voltage pulse. The depth profile of PIII Pd was a gradual transition from a metal-rich surface to an metal-deficient substrate [17]. After Pd implantation, a copper film was subsequently deposited by ECP.

3.1. Effect of Pd dosage

Rutherford backscattering spectrometry (RBS) results of Fig. 2 show that the Pd dosage was a quasi-linear function with the implantation time of PIII. The Pd

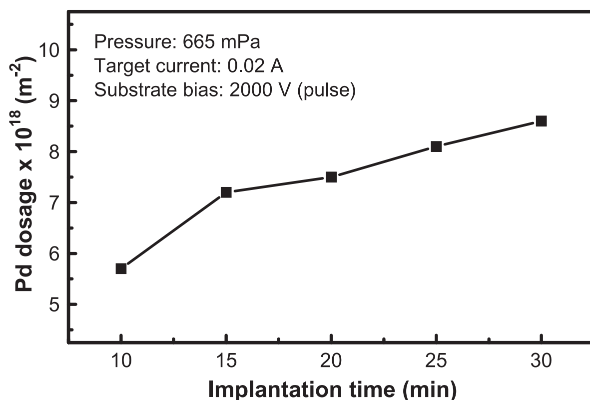

Fig. 2. Pd dosage by RBS measurements vs. implantation time of PIII.

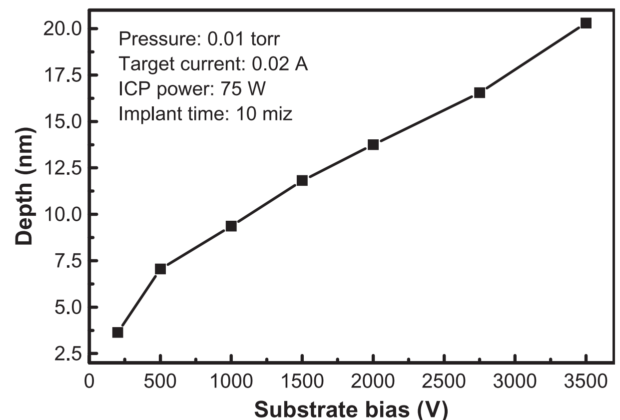

Fig. 4. Depth of Pd implantation with various of negative bias voltages.

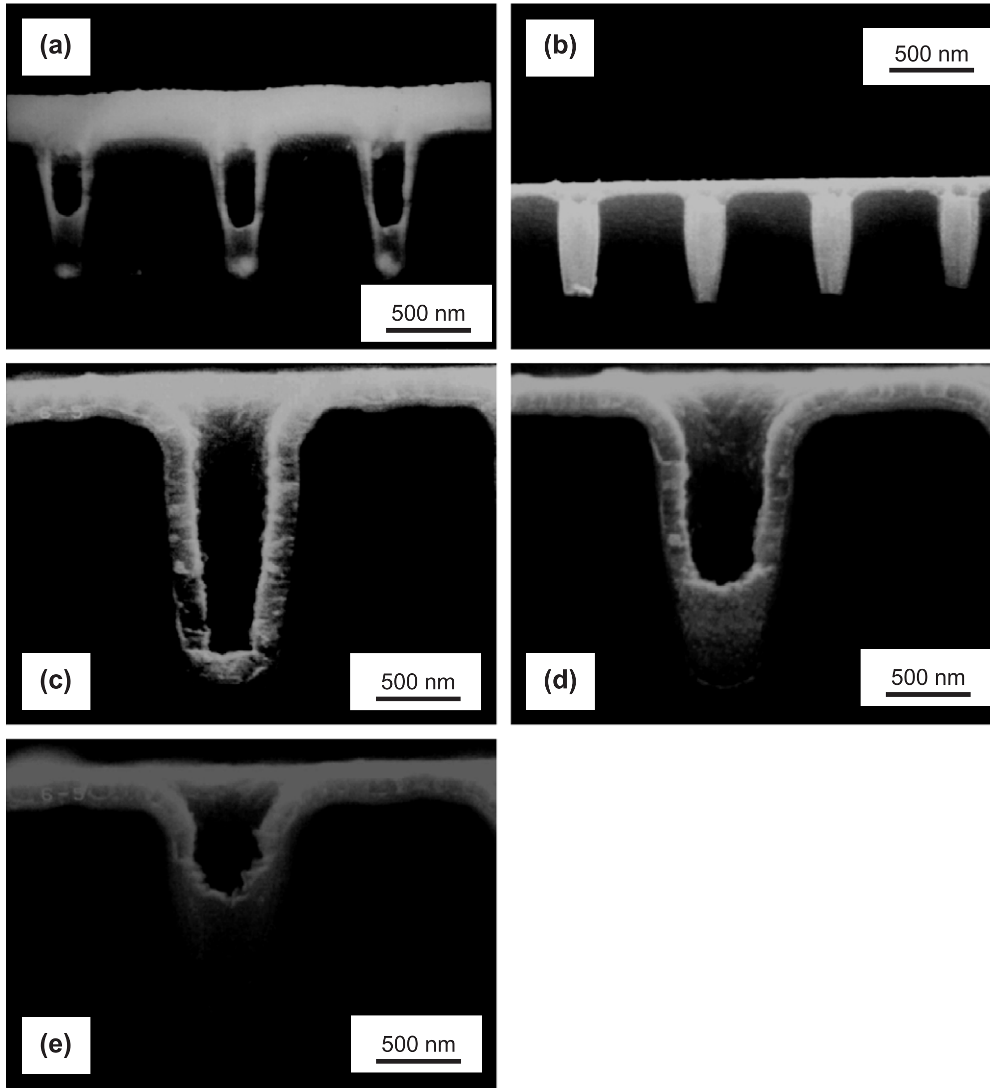

Fig. 5. SEM cross-sectional profiles of 4:1 AR, 0.35-μm bias deposited at (a) 3.33 mA/cm^2, 1000 V, 10 min, (b) 3.33 mA/cm^2, 3500 V, 10 min, (c) 3.33 mA/cm^2, 3500 V, 1 min, (d) 3.33 mA/cm^2, 3500 V, 3 min and (e) 3.33 mA/cm^2, 3500 V, 5 min.

dosage was in a range from 5.7×10^{18} to 8.6×10^{18} m^{-2}. In the early stage of the PIII process, the slope was likely higher. The quasi-linear variation in the whole range may be due to plasma charging effect on the substrate surface, and then an extra energy barrier was generated to lower the Pd dosage. Fig. 3 reveals that the copper thickness (at 2 mA/cm^2) increased with increasing the Pd dosage because the energy barrier for copper nucleation and growth decreased as the Pd dosage increased. A threshold Pd dosage of ~5.2×10^{18} m^{-2} was necessary for driving Cu-ECP. During Cu-ECP, copper was selectively nucleated on isolated Pd sites and then a continuous copper film was formed. The resistivity of copper films was dependent on the Pd dosage. Too high a Pd dosage resulted in a rough copper film with high resistivity (>10 μΩ cm) due to high copper growth rate and high Pd incorporation, whereas too low a Pd dosage generated insufficient nucleated sites for Cu-ECP leading to poor

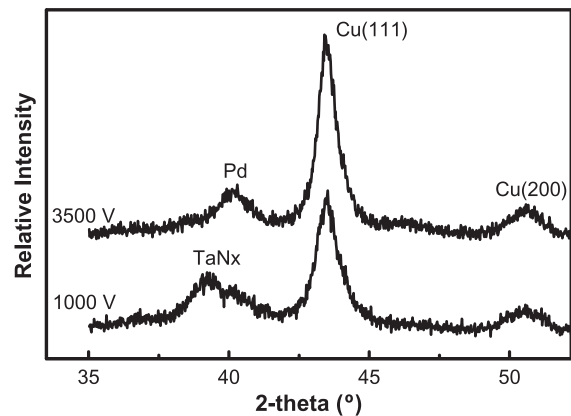

Fig. 6. XRD patterns (incidence angle: 50°) for electroplated copper films on Pd-implanted specimens produced using substrate bias voltage of 1000 and 3500 V. The plating current density was 3.33 mA/cm^2 and the deposition time was 3 min.

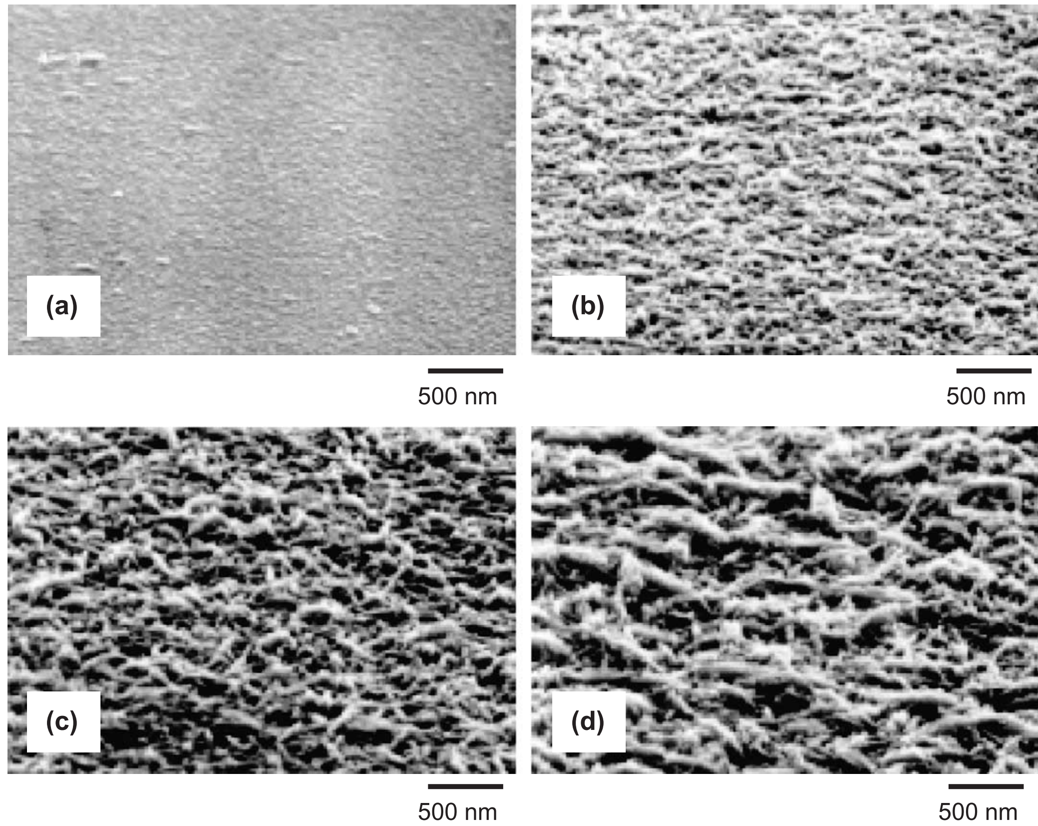

Fig. 7. SEM images of electroplated copper films for the applied current densities of (a) 3.33 mA/cm^2, (b) 6.67 mA/cm^2, (c) 10 mA/cm^2, and (d) 13.33 mA/cm^2. The deposition time was 3 min.

film adhesion as well as an increase of copper resistivity. The adhesion test was examined by 3M Scotch tapes. A copper film deposited on a low-Pd-dosage substrate was fully pulled away by Scotch tapes while peeling did not occur on a high-Pd-dosage substrate.

3.2. Effect of substrate bias

Fig. 4 shows the effect of bias voltages on the implantation depth of PIII Pd. The implantation depth increased from 3.6 to 20.3 nm as the substrate bias increased from 250 to 3500 V due to a higher implantation energy resulting from a higher bias voltage. The gap-filling capability of Cu-ECP in 4:1 aspect ratio, 0.35-μm bias with different substrate bias voltages of 1000 and 3500 V was shown in Fig. 5. Fig. 5a reveals that an anti-conformal profile with a void occurred when the lower substrate bias voltage (1000 V) was applied. A plausible explanation was that the lower substrate bias voltage generated a disorderly doping direction and formed a weaker seeding gradient between the sidewall

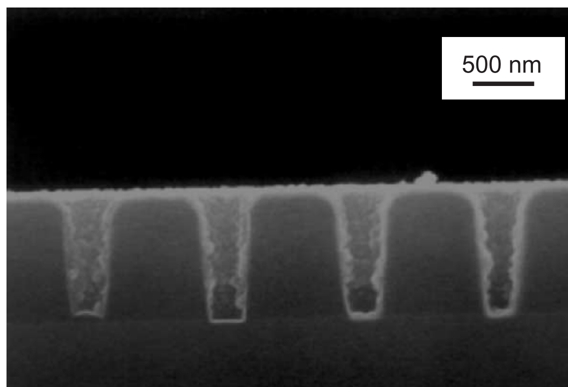

Fig. 8. SEM images of electroplated copper in 0.35-μm bias deposited by 1 mA/cm^2 for 3 min.

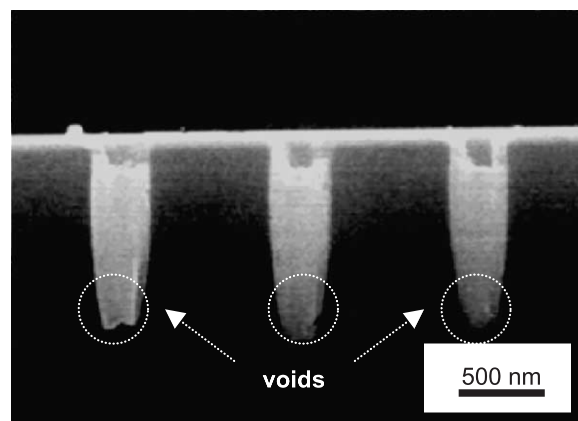

Fig. 9. SEM images of electroplated copper in 0.35-μm bias deposited on Pd-sputtered specimens by 3.33 mA/cm^2 for 10 min.

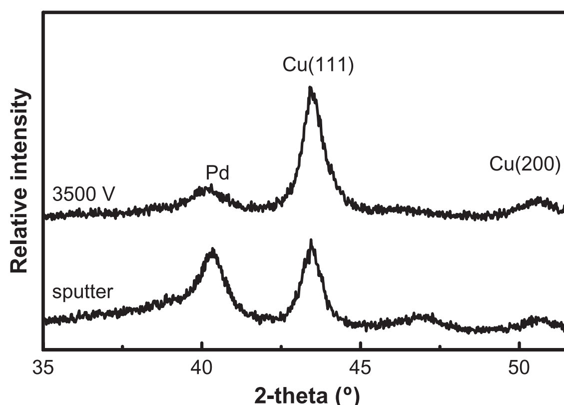

Fig. 10. XRD patterns (incidence angle: 50°) for electroplated copper films on Pd-sputtered and Pd-implanted specimens. The plating current density was 3.33 mA/cm^2 and the deposition time was 3 min.

and the bottom in a feature. In contrast, Fig. 5b shows that bottom-up filling was achieved using the higher substrate bias voltage (3500 V) because a more vertically downward doping generated a distinct concentration gradient of PIII Pd. As a result, the copper deposition rate was higher on the feature bottom than that on the feature sidewall. The evolution of deposition profiles for the bottom-up filling was shown from Fig. 5c to e.

Fig. 6 shows the XRD patterns of the electroplated copper films deposited on the substrates with two PIII bias voltages of 1000 and 3500 V. Two peaks at ~43.5° and ~50.6° indicated Cu(111) and Cu(200). In a face-center-cubic structure, a (111) texture was favored by the minimization of surface and interfacial energy, whereas a (200) texture was favored by the strain energy minimization [18]. The observed textures of the electroplated copper films may result from a competition between these mechanisms as mentioned. As the substrate bias increased from 1000 to 3500 V, the intensity ratio of (111)/(200) increased from 6.9 to 10 for a copper film with a thickness of ~600 nm. However, the (111)/(200) ratio was 6.2 for a copper film deposited on a sputtered-Pd substrate even the copper thickness was ~900 nm. Therefore, it was suggested that strain energy increased with increasing substrate bias during grain growth, resulting in a decrease in the Cu(200) intensity.

3.3. Effect of plating current density in ECP

Fig. 7 shows that the surface morphologies of the electroplated copper films became rougher and more porous as an applied current density of Cu-ECP increased. This was because copper ions in the diffusion layer became more depleted near the cathode surface under a high electric field. The plating process was controlled by diffusion and copper ions were reduced fast resulting in copper agglomeration around the protrusions on the surface [18]. However, under an insufficient applied current density (1 mA/cm^2), a discontinuous copper film was obtained presumably due to a lack of driving force for Cu surface diffusion, as shown in Fig. 8.

3.4. Effect of seeding process

Compared to PIII Pd, sputtered Pd was also evaluated. It was found that the sputtered-Pd seed layer generated poor step coverage and asymmetrical void defects at the bottom corners of 4:1 AR, 0.35-μm bias after Cu-ECP, as seen in Fig. 9. On the other hand, Fig. 10 shows the XRD patterns with an incidence angle of 50° of copper films deposited on the PIII-Pd and the sputtered-Pd specimens. As expected, a weaker Cu(111) intensity was obtained on the sputtered-Pd specimen due to a disorderly doping direction of sputtering.

4. Conclusions

Compared with sputtering, PIII had a better potential to be the seeding procedure for Cu-ECP in the Damascene process. In this study, bottom-up filling was achieved using PIII Pd as a seed layer for Cu-ECP. It was found that the copper film thickness was a quasi-linear function with the Pd dosage. A higher filling capability and a higher Cu (111)/(200) intensity ratio of electroplated copper films were obtained using PIII Pd with a higher substrate bias voltage.

Acknowledgement

The authors thank the financial support from National Science Council (NSC) of Republic of China under grant NSC 89-CPC-7-009-001, and the technical support from National Nano Device Laboratory (NDL).

References

[1] C.S. Hau-Riege, C.V. Thompson, Appl. Phys. Lett. 78 (2001) 3451.
[2] C.-K. Hu, L. Gignac, R. Rosenberg, E. Liniger, J. Rubino, C. Sambucetti, A. Domenicucci, X. Chen, A.K. Stamper, Appl. Phys. Lett. 81 (2002) 1782.
[3] P.C. Andricacos, C. Uzoh, J.O. Dukovic, J. Horkans, H. Deligianni, IBM J. Res. Dev. 42 (1998) 567.
[4] T. Nguyen, L.J. Charneski, D.R. Evans, J. Electrochem. Soc. 144 (1997) 3634.
[5] T. Nguyen, L.J. Charneski, S.T. Hsu, J. Electrochem. Soc. 144 (1997) 2829.
[6] E.K. Yung, L.T. Romankiw, J. Electrochem. Soc. 136 (1989) 206.
[7] C. Lingk, M.E. Gross, J. Appl. Phys. 84 (1998) 5547.
[8] R.L. Jackson, E. Broadbent, T. Cacouris, A. Harrus, M. Biberger, E. Patton, T. Walsh, Solid State Technol. 41 (1998) 49.
[9] S.Y. Chiu, J.M. Shih, S.C. Chang, K.C. Lin, B.T. Dai, C.F. Chen, M.S. Feng, J. Vac. Sci. Technol. B 18 (2000) 2835.
[10] S.W. Hong, C.H. Shin, J.W. Park, J. Electrochem. Soc. 149 (2002) G85.
[11] S.W. Hong, J.W. Park, Electrochem. Solid-State Lett. 5 (2002) C107.
[12] H.H. Hsu, C.C. Hsieh, M.H. Chen, S.J. Lin, J.W. Yeh, J. Electrochem. Soc. 148 (2001) C590.

[13] J.H. Lin, T.L. Lee, W.J. Hsieh, C.C. Lin, C.S. Kou, H.C. Shih, J. Vac. Sci. Technol. A 20 (2002) 733.
[14] X.Y. Qian, D. Carl, J. Benasso, N.W. Cheung, M.A. Lieberman, J.E. Galvin, R.A. MacGill, M.I. Current, Nucl. Instrum. Methods B 55 (1991) 884.
[15] W. Ensinger, Mater. Sci. Eng. A253 (1998) 258.
[16] N.W. Cheung, Mater. Chem. Phys. 46 (1996) 132.
[17] W. Ensinger, Nucl. Instrum. Methods B120 (1996) 270.
[18] S.C. Chang, J.M. Shieh, K.C. Lin, B.T. Dai, T.C. Wang, C.F. Chen, Y.H. Li, C.P. Lu, M.S. Feng, J. Vac. Sci. Technol. B 19 (2001) 767.