Introduction to the Special Issue on Integrated Multimedia Platforms

MEDIA communication in the past was associated with a single specific application, typically telephone, TV, or various data transfer on computer networks. With the development of the Internet in wired or wireless forms, we are witnessing the convergence of different application functionalities into the same multimedia terminal. Such terminals ideally would support all functionality in different forms or levels depending on the environment in which they are deployed. Currently we can clearly depict four environments: the office, the home, the pocket, and the car. All such "environments" have dedicated terminals that require the implementation of several complex processing standards at different "levels" of performance and with different implementation constraints. In such scenarios new approaches to system design and new implementation challenges appear. The fact that the same processing standards, JPEG, MPEG, and network protocols appear on different terminals seems to facilitate the work of designers customizing basic IP for the specific application. In reality, the lack of high level tools and efficient design methodologies make the work of transforming the "reference standard" behavioral models into implementations according to specific constraints still a very difficult and time consuming task. Much of the time is consumed in "recoding" complex algorithms into implementation languages and reverifying functionality and conformance. Whether the task at hand is porting a multimedia standard onto a given DSP platform, finding the best partitioning between software and hardware coprocessing, defining a new application specified integrated circuit (ASIC) architecture, or minimizing power dissipation for a given performance constraint, we experience that the individual and combination of design tasks is an extremely difficult problem. New implementation technologies, such as modern reconfigurable hardware, provide new potential advantageous solutions. In reality, they also add new dimensions to the design problem, thus greatly increasing the complexity by offering new ways to realize multiple requirements, while currently not offering appropriate system level tools to assist the designer in exploring several design implementation solutions. As manual optimization becomes impractical, the designer loses the sense of control of the design unless new high-level tools can be developed to increase awareness and efficiency of the solution space exploration.

The goal of this Special Issue is indeed to capture recent fundamental developments and achievements in the areas of high-level tool for system-on-a-chip (SoC) design, namely architecture exploration, architecture design, algorithms design, design methodology, complexity analysis, and implementation tools.

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For this reason, the first part of this Special Issue is dedicated to papers tackling high-level tool issues. Seven papers examine overall architecture design with the emphasis on various design aspects and optimization constraints. Critical path, memory access latency, memory bandwidth efficiency, data flow optimization, memory access minimization, and power efficiency are the main topics. The second part of this Special Issue focuses on the optimization of individual modules particularly critical for implementation in an integrated multimedia system and typical common building blocks for some of the various versions of video and image compression standards.

In the first part, the first paper entitled "Evaluation of the Parallelization Potential for Efficient Multimedia Implementations: Dynamic Evaluation of Algorithm Critical Path" addresses the problem of getting a high-level global view of a complex algorithm. The methodology and the associated tool allow the designer to dynamically identify the critical path, thus avoiding static code analysis clearly inappropriate in multimedia compression implementations tasks and evaluating the parallelization potential. The two main innovations proposed are the possibility to perform the analysis under real input signals and the fact that no limitations are imposed on the usage of programming operators and on the usage of any data addressing and memory allocations modes for C and C++.

The second paper entitled "Memory Centric Design of an MPEG-4 Video Encoder" investigates the problem of multimedia system design by combining the algorithmic refinements and transformations with a memory centric optimization methodology so as to derive suitable memory architecture for video encoder systems. The combination of upfront algorithmic tuning with memory centric optimizations to transform the video application into a system consisting of functional blocks with localized data processing and a tailored memory hierarchy constitute the essence of the methodology. The resulting memory optimized functional description is proposed as the leverage for the cost-efficient mapping of the system on integrated multimedia platforms. Results on a MPEG-4 video encoder design case leading to pipelined system architecture are also reported and analyzed.

On the same issue of designing efficient data flows memory architectures, the third paper entitled "An Efficient Quality-Aware Memory Controller for Multimedia Platform SoC" investigates a new multilayer approach for memory controllers for SoC implementations. Minimization of latency providing different levels of bandwidths is certainly a common and important multimedia constraint. The paper provides results of achievable latency minimization of the proposed solution in the case of a STB implementation.

Another important element of consideration for potential optimization improvements is the cache architecture to be used for multimedia systems. The fourth paper entitled "Software-Controlled Cache Architecture for Energy Efficiency" investigates the achievable power dissipation savings on a specific MPEG-2 software decoder when a new software controlled cache architecture is used. The experimental results show considerable gain in energy efficiency when compared to classical cache controls without reducing the performance efficiency.

An example of the high-dimensional design spaces faced nowadays by multimedia system designers is provided in the paper entitled "Power-Rate-Distortion Analysis for Wireless Video Communication Under Energy Constraints." Using the new dynamic voltage scaling CMOS technology the paper jointly considers for the design the power constraints and the image distortion when reduced complexity algorithms are used by the video encoder. The result is a framework in which the classical video coding rate-distortion behaviors are extended to power-rate-distortion analysis where the goal is to minimize the image distortion under rate and power constraints. Such joint optimization is particularly important for mobile video application terminals.

An overall system optimization tailored to multimedia algorithm can also be achieved by means of a flexible instruction set architecture composed by a classical processor instruction set combined with higher level hardware block processing. Such approach is investigated by the paper entitled "Flexible Heterogeneous Multicore Architectures for Versatile Media Processing Via Customized Long Instruction Words." The paper studies a flexible reconfigurable controller for sequences of "customized long instruction words" that are able to express a middle-grained parallelism among the higher level hardware blocks and a reduced-instruction set computer (RISC).

To design sophisticated multimedia system, there are several important tasks such as defining a new architecture specific for a multimedia standard, defining an instruction set for a processor architecture, or guiding the optimization process in terms of control-flow and data-flow for specific architecture. The paper entitled "High-Abstraction Level Complexity Analysis and Memory Architecture Simulations of Multimedia Algorithms" reviews the state of the art of complexity analysis methodologies oriented to the multimedia system design. It demonstrates an ideal integrated tool for the automatic analysis capable of producing complexity results based on rich and customizable metrics, and reports some examples of complexity analysis results from multimedia standards/algorithms.

The last paper of the first part, entitled "Accelerate Video Decoding With Generic GPU" proposes to take advantage of a generic graphics processing unit (GPU) to accelerate the video decoding process by moving some of the decoding functions such as motion compensation to the GPU. The pipeline architecture for both central processing unit (CPU) and GPU are specifically designed with such goal and constitute the main innovation proposed in the paper.

In the second part of the Special Issue, the main processing functions or building blocks present in the more common standards are optimized for embedded implementations. They include: motion estimation, discrete cosine transform (DCT) and shape-adaptive transforms. A simplified binary motion estimation engine is studied by the paper entitled "DCT-Based Adaptive Thresholding Algorithm for Binary Motion Estimation" where a binary version of motion estimation is implemented aiming at low-complexity VLSI implementation.

One of the most distinct features of the MPEG-4 standard is the object-based coding for multimedia information. To achieve the description of video object, the shape-adaptive DCT is a critical module. For mobile applications, the tradeoffs between functionality and power efficiency are challenging. The goal for low power implementations of shape-adaptive DCT modules are studied in the paper entitled "An Energy-Aware IP Core Design for the Variable-Length DCT/IDCT Targeting at MPEG-4 Shape-Adaptive Transforms."

In current times, the challenge of multimedia systems implementations is the need of both flexible architectures and yet efficient implementations. The architecture should be as much as possible reconfigurable but at the same time easy to optimize for multiple functions. The paper entitled "A Method for Designing High-Radix Multiplier-Based Processing Units for Multimedia Applications" proposes such an architecture specific for video and image processing focusing on memory block optimization, pipeline stage parallelization and multiplexed interconnections. It provides an excellent case study for the design of this class of architectures for the implementation of integrated multimedia system.

For most recently adopted multimedia standards, the DCT is a widely used component for a multimedia system. Thus, an efficient implementation for DCT is a critical part for a multimedia system implementation. In the last article entitled "A New Time Distributed DCT Architecture for MPEG-4 Hardware Reference Model," the authors presented a very efficient implementation of the DCT module. The proposed time distributed architecture exploits the computational redundancy efficiently.

Although the selection of papers presented in this special issue is certainly of high quality and attacks from different sides the implementation and design challenges, the overview proposed is certainly far from being exhaustive and complete. The difficulties of the problems leave many aspects open to further development and advances. The space and time limits of this Special Issue also forced us to narrow the wide investigations and high quality contributions that have been received.

The Guest Editors would like to thank all the people who contributed to this Special Issue including the authors who submitted papers that we were unable to accommodate due to space limits. Many thanks also to the reviewers for their professional and accurate evaluations of the papers provided in a timely manner. The Guest Editors also wish to thank Dr. T. Sikora for giving us opportunity to organize this Special Issue.

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In 1995, he joined the David Sarnoff Research Center, Princeton, NJ, as a Member of Technical Staff. Later, he was promoted to Technology Leader and a Program Manager at Sarnoff. While at Sarnoff, he led a team of researchers and developed an optimized MPEG-2 software encoder. For his work in the encoder and MPEG-4 areas, he received two Sarnoff achievement awards and three Sarnoff team awards. Since 1992, he has actively participated in ISO's Moving Picture Experts Group (MPEG) digital video coding standardization process with particular focus on the scalability/compatibility issue. He is currently the co-editor of part 7 on the MPEG-4 committee. He has made more than 90 contributions to the MPEG committee over the past 11 years. His main research interests are compatible/scalable video compression, stereoscopic video coding, and motion estimation. In September 1999, he joined the faculty at National Chiao-Tung University, Hsinchu, Taiwan, R.O.C. He has published over 50 technical journal and conference papers in the field of video and signal processing. He holds 13 U.S. patents and 30 European and worldwide patents.

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