1.2 V sub-nanoampere A/D converter

G. Rachmuth, Y.-S. Yang and C.-S. Poon

CMOS-based integrated biochemical sensors generate photo currents at sub-nanoampere (nA) levels, which present a challenge for digital data acquisition. Proposed is a MOS current-mode analogue-to-digital converter with sub-nA sensitivity. Its inherent low-voltage low-power and small-size capabilities are ideal for portable chemi- or biosensor applications.

Introduction: High-performance analogue-to-digital converters (ADCs) are generally optimised for conversion speed and resolution with given size and power budget [1]. In CMOS-based mobile biochemical sensor applications [2, 3], however, speed and resolution are immaterial because of the slow reaction rates (>seconds) and inherent experimental errors (~10%) typical of most biochemical reactions. Instead, ADC sensitivity, power consumption and size are of major concern [4]. To convert sub-nA-level photo currents into voltage, [3] amplified the signal using large-gain (10^6) current mirrors, increasing power and area requirements and the current mirror's susceptibility to mismatch errors for a given chip area. In [5], increased ADC sensitivity was achieved by successive capacitive integration and voltage-to-frequency conversion at the expense of increased power consumption and long conversion time (~seconds).

In this Letter we propose a novel current-mode ADC (IADC) capable of digitising the photo currents in [2, 3] at a speed and resolution commensurate with such applications. The IADC operates at a supply voltage (V_{DD}) as low as 1.2 V, contains no capacitors or clocks, and can be directly integrated alongside the CMOS photodiode in any fabrication process.

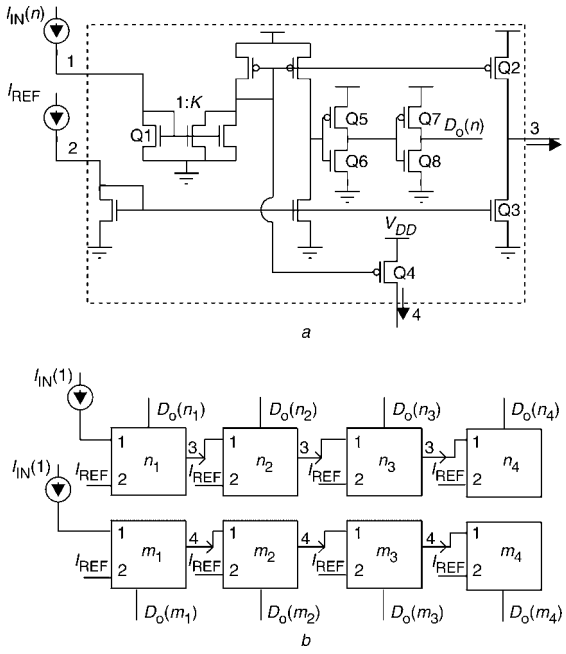

Fig. 1 *Subthreshold IADC*

a Circuit design for unit cell with $V_{DD} = 1.2$ V
n cell: input node, **1**; output node, **3**, *m* cells, input node, **1**; output node, **4**
b *n*-cell and *m*-cell IADC architectures

IADC design: Previous IADC designs allow high-speed conversion down to the µA range by biasing the transistors in the strong-inversion (above-threshold) regime [1, 6, 7]. To achieve sub-nA sensitivity and low V_{DD}, we used an algorithmic IADC cell architecture similar to [7] but with a modified circuit design that is amenable to subthreshold operations (Fig. 1*a*). Cells $n = 1, 2, \ldots, N$ are cascaded with the analogue output of one cell connected to the analogue input of the following cell (Fig. 1*b*). The analogue input of cell n, $I_{IN}(n)$, is scaled using a $1{:}k_n$ current mirror (Q1). The comparator (Q5–Q8) output, $D_O(n)$, is a HI if $k_n \cdot I_{IN}(n)$ is greater than a user-defined reference current I_{REF}, and is an LO otherwise. To operate in the sub-nA range, a transmission switch gated by $D_O(n)$ in [7] is omitted in order to avoid large switching current artifacts that may disrupt the signal conversion process. As a consequence, the input current into the next cell ($I_{IN}(n+1) = k_n \cdot I_{IN}(n) - I_{REF}$) via the current subtraction transistors Q2 and Q3 is no longer dependent on $D_O(n)$. This design reduces the IADC to a flash architecture, which allows the fastest conversion speed for any given operating conditions.

Traditional flash architecture generates a thermometer code according to a voltage divider sequence. Here, the $1{:}k_n$ scaling of input current in each cell provides an equivalent current divider sequence $[1 - (k_1 \cdot k_2 \cdots k_n)^{-1}]$, $n = 1, 2, \ldots, N$, for the range $I_{REF}/k_1 \leq I_{IN}(1) \leq I_{REF}$, where $I_{IN}(1)$ is the current input to the IADC, and k_1 is the mirror ratio of $n = 1$. When $k_n \cdot I_{IN}(n) < I_{REF}$ for cell n, the inputs to all subsequent cells are zero so that $D_O(n:N)$ is LO. Thus the analogue input is quantised by the largest value of n such that $D_O(n)$ is HI.

A drawback of the cell design in [7] is that in the critical region $k_n \cdot I_{IN}(n) \simeq I_{REF}$ where the currents in transistors Q2 and Q3 of cell n are almost balanced, the drain current of transistor Q1 in cell $n+1$ may cause a significant error. This difficulty is circumvented in the present design by redefining the input–output relationship of each cell as follows. A set of cells $m = 1, 2, \ldots, M$ are cascaded as before but with $I_{IN}(m+1) = k_m \cdot I_{IN}(m)$ via transistor Q4 (Fig. 1*a*). This results in a current divider sequence $(k_1 \cdot k_2 \cdots k_m)^{-1}$ for the range $0 \leq I_{IN}(1) \leq I_{REF}/k_M$, such that when $I_{IN}(m) > I_{REF}/k_m$, D_O ($m{:}M$) is HI. In this case, the analogue input is quantised by the smallest m such that $D_O(m)$ is LO. Both the n-cell and m-cell IADCs have a variable dynamic range that is set by I_{REF}. I_{REF} values in or below the nA range bias the transistors in the subthreshold regime, allowing the conversion of sub-nA currents.

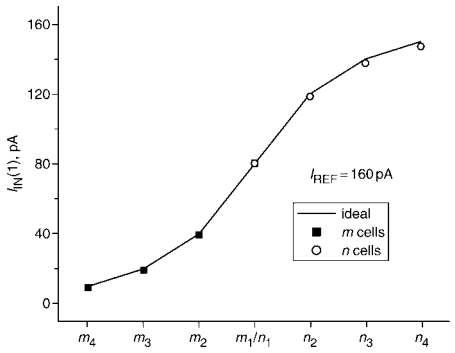

Fig. 2 *Simulation results for prototype (with $M = N = 4$, $I_{REF} = 160$ pA, $V_{DD} = 1.2$ V) showing input currents at which each m and n cell begins to switch*

——— corresponding theoretical values

Results: The above IADC design was simulated on T-Spice and a prototype chip was fabricated using an AMI 1.5 µm process. For convenience the results for 4 *m*-cells and 4 *n*-cells with $k_n = k_m = 2$ are presented here although the design can be extended to any number of cells with arbitrary current divider ratios. Simulations showed that the *m*-cells generally had higher sensitivity and accuracy than the *n*-cells (Fig. 2). Measurements of the fabricated IDAC with a Keithley 6485 picoammeter showed that the *m*-cells had an input current sensitivity of <100 picoampere (pA).

The IADC response bandwidth is determined by the conversion delay, which is given by the maximum rise or fall time (whichever is longer) of all cell responses when switching on or off, respectively. For each cell, this value is determined primarily by the corresponding comparator's switching time, $\tau \propto (C_L \cdot V_{DD})/(I_{IN} - I_{REF})$, where C_L is the load capacitance. Simulations showed that for $V_{DD} = 1.2$ V and a square-wave current input with amplitude $\hat{I}_{IN}(1) = 0.1$ nA and $I_{REF} = 1.6$ nA, the conversion delay was <500 µs. At $\hat{I}_{IN}(1) = 1$ nA and $I_{REF} = 16$ nA, the conversion delay was <15 µs.

In Fig. 3*a*, the fabricated IADC chip responded faithfully to a triangular-wave input with peak current $\hat{I}_{IN}(1) = 30$ nA at a frequency of 1 Hz. Similar results were obtained for $\hat{I}_{IN}(1)$ down to 1 nA. At even lower input currents or higher frequencies, measurements were limited by the response of the testbed, which was not designed to operate at such low current levels. Simulations showed that the IADC faithfully converted the signal with $\hat{I}_{IN}(1) = 50$ pA at a frequency of 1 Hz (Fig. 3*b*). In practice, the IADC can interface directly to the CMOS photodiode on chip, preserving the IADC response as predicted by simulations.

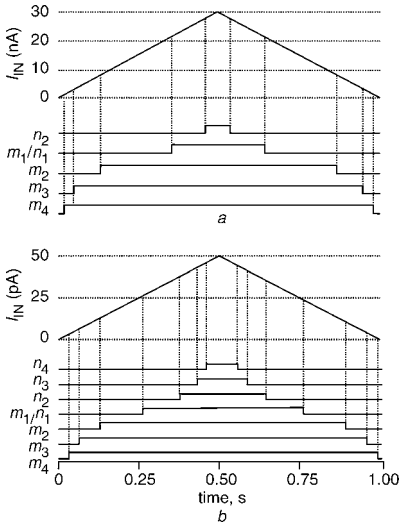

Fig. 3 *Fabricated and simulated IADC response*

a Response of fabricated *m* and *n* cells to 30 nA triangular-wave input, ($V_{DD} = 1.2$ V)
b Simulation results of *m* and *n* cells' response to 50 pA triangular-wave input, ($V_{DD} = 1.2$ V)

Because of inevitable current–mirror mismatch, the resulting current divider ratios may differ from the designed value of 2. In Fig. 3, a simple calibration procedure yielded the actual ratios of 2.44, 2.36 and 2.6 for m_4/m_3, m_3/m_2 and m_2/m_1, respectively. Once calibrated, proper IADC operation was achieved. In practice, mismatch errors may be further minimised by increasing transistor sizes or decreasing process dimensions for a given size.

Discussion: The salient features of this IADC are its high input sensitivity, a low V_{DD} and a programmable dynamic range, with a design that is simple, small, and power efficient. A conversion cell with $I_{REF} = 1$ nA uses < 10 nW of static power.

The resultant IDAC conversion speed is adequate for most biosensor applications. For example, the sub-nA level currents from the HRP-luminal-H_2O_2 system in [2, 3] can be digitised in < 1 s, allowing ample temporal resolution for the measurement of initial reaction rates that are important to enzyme kinetics.

This new IADC can be readily integrated with any portable CMOS sensor at reduced overall power, size, and cost. Its input sensitivity, speed and resolution can be further enhanced by employing sub-pA circuit [8] and low-voltage wide-input comparator [9] design techniques and with increased number of conversion cells.

Acknowledgments: The VLSI chips were fabricated with the support of the MOSIS Education Program. G. Rachmuth was a recipient of the US National Defense Science and Engineering Graduate Fellowship.

28 December 2004
Electronics Letters online no: 20058259
doi: 10.1049/el:20058259

G. Rachmuth (*Division of Engineering and Applied Sciences, Harvard University, Cambridge, MA 02138, USA*)

Y.-S. Yang (*Department of Biological Science and Technology, National Chiao Tung University, Hsinchu, Taiwan*)

C.-S. Poon (*Harvard-MIT Division of Health Sciences and Technology, MIT, Cambridge, MA 02139, USA*)

E-mail: cpoon@mit.edu

G. Rachmuth: Also at Harvard-MIT Division of Health Sciences and Technology, MIT, Cambridge, MA 02139, USA

References

1 Razavi, B.: 'Principles of data conversion system design' (IEEE, New York, 1995)
2 Lu, U., *et al.*: 'CMOS chip as luminescent sensor for biochemical reactions', *IEEE Sens. J.*, 2003, **3**, pp. 310–316
3 Lu, U., *et al.*: 'The design of a novel complementary metal oxide semiconductor detection system for biochemical luminescence', *Biosens. Bioelectron.*, **19**, 2004, pp. 1185–1191
4 Yotter, R.A., and Wilson, D.M.: 'A review of photodetectors for sensing light-emitting reporters in biological systems', *IEEE Sens. J.*, 2003, **3**, pp. 288–303
5 Simpson, M., *et al.*: 'An integrated CMOS microluminometer for low-level luminescence sensing in the bioluminescent bioreporter integrated circuit', *Sens. Actuators B*, 2002, **72**, pp. 134–140
6 Ravezzi, L., Stoppa, D., and Della Bettam, G.-F.: 'Current-mode A/D converter', *Electron. Lett.*, 1998, **34**, pp. 615–616
7 Nairn, D.G., and Salama, A.: 'Current-mode algorithmic analog to digital converter', *IEEE J. Solid State Circuits*, 1991, **25**, pp. 997–1004
8 Linares-Barranco, B., *et al.*: 'Current mode techniques for sub-pico-ampere circuit design', *Analog Integr. Circuits Signal Process.*, 2004, **38**, pp. 103–119
9 Hung, Y-C., and Liu, B-D.: 'A low-voltage wide-input CMOS comparator for sensor applications using back-gate technique', *Biosens. Bioelectron.*, 2004, **20**, pp. 53–49