

Simultaneous Power Supply Planning and Noise Avoidance in Floorplan Design

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Abstract—With today's advanced integrated circuit manufacturing technology in deep submicron (DSM) environment, we can integrate entire electronic systems on a single system on a chip. However, without careful power supply planning in layout, the design of chips will suffer from local hot spots, insufficient power supply, and signal integrity problems. Postfloorplanning or postroute methodologies in solving power delivery and signal integrity problems have been applied but they will cause a long turnaround time, which adds costly delays to time-to-market. In this paper, we study the problem of simultaneous power supply planning and noise avoidance as early as in the floorplanning stage. We show that the problem of simultaneous power supply planning and noise avoidance can be formulated as a constrained maximum flow problem and present an efficient yet effective heuristic to handle the problem. Experimental results are encouraging. With a slight increase of total wirelength, we achieve almost no static IR (voltage)-drop requirement violation in meeting the current and power demand requirement imposed by the circuit blocks compared with a traditional floorplanner and 45.7% of improvement on a ΔI noise constraint violation compared with the approach that only considers power supply planning.

Index Terms—Floorplanning, physical design, power supply planning, signal integrity.

I. INTRODUCTION

WITH the advent of further technology scaling, circuits which contain more functionality are operating at higher frequencies, currents, and power. The lower supply voltage helps to consume less power dissipation in general, but at the same time sabotages the noise margin of the devices as well. As a result, many effects that were less important in the previous technology of designs have become major factors in correct functionality and performance of these dense chips. In today's new interconnect-centric paradigm [1], power delivery and dissipation, timing, signal integrity, and reliability have become as important, or more important, as die area, which was a major concern for the previous technology.

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During manufacturing, numerous silicon failures are caused by signal integrity problems, such as IR (voltage)-drop, ΔI noise, and electromigration. IR-drop and ΔI noise may cause incorrect circuit functioning and timing requirement mismatch, while electromigration may cause damage to the circuits' life-time. These problems are on the rise due to the lack of existing design tools and methodologies to address these issues effectively. Under these circumstances, as [2] and [3] pointed out, the ability to design the chip, the package, and the surrounding system concurrently becomes a primary advantage.

A packaging technique utilizing flip-chip bonding, or controlled collapsible chip connection (C4), has been developed from IBM for decades to manufacture very large scale integration (VLSI) chips quickly and cost effectively [4], [5]. Nowadays, C4/flip-chip technology is more widely used in microprocessor and high-performance application specific integrated circuit (ASIC) manufacturing than wire-bonded technology is. The general C4 chip patterns are shown in Fig. 1. The use of area interconnect packaging in high-frequency microprocessors is motivated by its high bandwidth and good power distribution capability [6]. However, even though the technology minimizes on-chip voltage fluctuations, difficulty still lies in the interaction of two independent functional blocks that share a power source [7].

Postfloorplanning or postroute power supply synthesis have been applied to generate satisfactory power supply distribution, trying to meet the requirements of different components in system-on-a-chip (SoC) design. Due to reduced power supply voltage, tighter noise margin, and dc voltage drop, the task has been difficult [8]. Among the approaches of handling/estimating power delivery [9], [10], the planning of a mesh power rail followed by hierarchical power/ground (P/G) network designs is still a major method to design high-performance ICs and microprocessors [11]–[14]. Nevertheless, power supply synthesis after floorplanning cannot guarantee high-quality power supply under either obviously limited routing resources or infeasible routing constraint being generated. In many cases, when the circuit block locations and sizes are fixed, the constraints such as voltage drop and current density are so tight that there is no feasible power network design capable of keeping power supply noise within a specified margin. Hence, it is important to consider power supply planning during the early design stage, where the circuit block locations and shapes can be flexibly changed.

There has been a lot of research in floorplanning, e.g., [15]–[18]. Parallel to those works, interconnect-driven floorplanning related works [19]–[21] have been proposed to extend

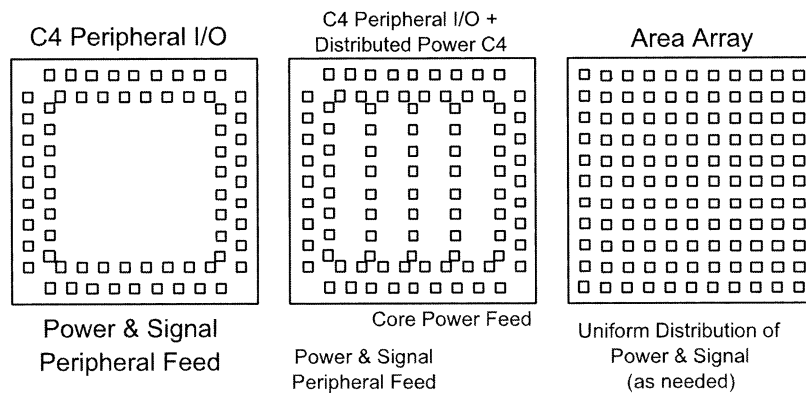


Fig. 1. C4 chip patterns from IBM online document.

the capability of the floorplanner. However, all these approaches ignored power supply planning. The resultant floorplans may suffer from serious local hot spots and insufficient power supply in some regions. In [22], the authors use two levels of packing for different kinds of P/G network requirements to take power planning into consideration. This model cannot handle the power delivery problem with a power supply noise constraint.

High-performance ICs require a robust power delivery network with nominal supply voltage fluctuations. We formulate the problem of simultaneous power supply planning and noise avoidance as a supply-demand problem for power delivery with side constraint for a power supply noise requirement. We use a constrained network flow model to represent this problem and handle it with a modified max-flow algorithm. We have incorporated our algorithm into a floorplanning algorithm for integrated floorplanning and power supply planning. (Note that our approach can be applied to any floorplanner as well.) Experimental results are encouraging. Comparing with a traditional floorplanner with no power supply planning at all [15] and a floorplanner with power delivery planning for avoiding hot spots [23], we obtain floorplans in a fixed die area but significantly better in terms of meeting the IR-drop requirements and minimizing the violations of ΔI noise constraint imposed by the circuit blocks. This approach can augment the P/G distribution network design and can be an alternative solution other than decoupling capacitance (decap) allocation in power supply noise avoidance during floorplanning [24].

The rest of the paper is organized as follows. Section II describes the floorplan design with power supply noise considerations and problem formulation. The network model and the algorithm for power supply planning with noise avoidance are presented in Section III. Section IV shows our approach for simultaneous power supply planning and noise avoidance in floorplanning. Experimental results are shown in Section V. The discussion and conclusion are presented in Sections VI and VII. This paper is an extension of [23] and [25].

II. FLOORPLANS WITH POWER SUPPLY NOISE CONSIDERATIONS

Because of deep submicron (DSM) technology, chips now contain more functions and are being driven to higher performance levels than ever before. Furthermore, reduced supply voltage in low power design nowadays tightens the noise

margin. Without careful layout planning, the design will suffer from local hot spots, insufficient power supply, and signal integrity problems, among which we focus primarily on IR-drop and ΔI noise.

In traditional VLSI design, as [5], [26], and [27] pointed out for power supply noise analysis, the resistive IR-drop occurs mostly on the chip and the inductive ΔI noise only occurs on the package. IR-drop is voltage drop of the power and ground due to current flowing in the P/G resistive network. However, as we move into DSM regime, the inductive component of wire impedance $j\omega L$ becomes comparable to R . Because of the self-inductance of the off-chip bonding wires and the on-chip parasitic inductance inherent to the power supply rails, the fast current surges result in voltage fluctuations in the power distribution network. These voltage fluctuations are also called simultaneous switching noise (SSN) or ΔI noise [28].

Scientists and engineers have been doing research on accurate transient power analysis, trying to minimize power supply noise across the entire chip. According to [29] and [30], SSN has always been a concern in sampled-analog and mixed-mode circuits, and a 10% supply voltage fluctuation may translate to more than a 10% timing uncertainty. C4 has been developed to manufacture VLSI chips quickly and cost effectively [4], [5]. C4/flip-chip technology provides high input/output (I/O) density, leading-edge cooling capability, and high reliability. An array of PbSn solder ball bumps are arranged around the surface of a chip, either in a peripheral or area-array configuration (Figs. 1 and 3). The major advantage of this technology is, after packaging, that the low-inductive/resistive power is fed across the face of the die, minimizing on-chip voltage fluctuations that lead to improved voltage tolerances, and thus improved on-chip frequencies. This technology also helps to replace global on-chip power rails by local power pads/bumps and smaller local rails, which saves chip area [6]. Nevertheless, the technology still suffers the problem of power delivery mainly in two constraints mentioned above.

The primary difficulties occurred in static and transient voltage drop during the planning of power supply in SoC design [7]. First, components in an IC share a common power source that supplies voltage and current to transistors. The transistors draw current when they turn on and off. The power network must be designed such that voltage and current supplies

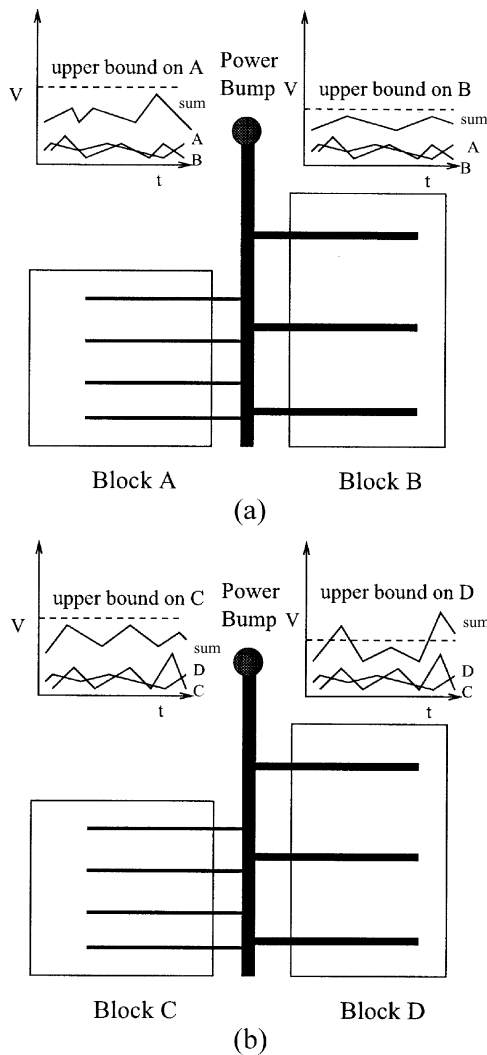


Fig. 2. Two examples of the ΔI noise constraint illustration when sharing power sources. The V-t curves are voltage fluctuations for blocks and the superposition seen in power supply bump. (a) The power supply bump is clean since the voltage fluctuations of two blocks are within the upper bound on ΔV for both blocks. (b) The power supply bump is noisy since the voltage fluctuations of block C and D exceeds the upper bound on the ΔV for block D.

from power sources are available to all transistors. IR-drop can have a significant impact on a design. Second, the interaction of two independent functional blocks that share a power source causes a voltage-drop problem. Illustrated in Fig. 2(b), the voltage fluctuation of block C and its subsequent load on the power bus affect the power supply voltage seen by block D and vice versa. If block D experiences a reduced supply voltage, it exhibits a higher-than-normal delay and might not function properly.

From the above observation, obviously, the positions of blocks are important variables in power supply planning and noise avoidance, meaning floorplanning will affect the quality of power delivery. In Fig. 3, there are two floorplans with the same area but different relative position of blocks in area-array design.¹ Block b_3 can get four power supply bumps to deliver

¹The area-array design figures shown in this paper only present power supply bumps and functional blocks. In fact, there are signal bumps in the design as well.

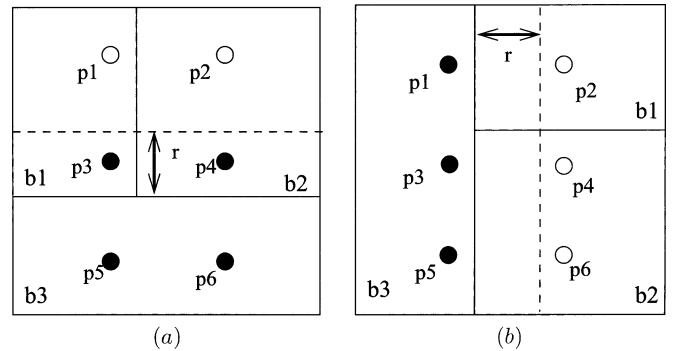


Fig. 3. Floorplanning affects power supply planning and noise avoidance. Block b_3 can get four power supply bumps to deliver power on the left floorplan (two within the block and two within a distance r) while it can possibly only get three power supply bumps on the right one. In (b), this block may also suffer from ΔI noise constraint violation.

power on the left floorplan while it can possibly only get three power supply bumps on the right one. This block may suffer from insufficient voltage delivered and power supply noise constraint violation, thus failing to function normally. Next, we introduce the models of the constraints in our problem formulation.

A. IR-Drop Requirement

IR-drop is caused by current drawn off of the P/G resistive network. If the wire resistance is too high or the cell current is large, an unacceptable voltage drop may occur, which causes the supply voltage to be lower than required. Similar to [31], the following equation gives the effective resistance (R) for pad transfer metal from a block to the power supply bump with $C1$ and $C2$ being constants derived from simulation, where $\text{dist}(b, p)$ is the distance between the center of the block and power supply bump

$$R = C1 + C2 * \text{dist}(b, p).$$

Using I_{avg} as the average dc current for the block, we can obtain voltage drop as $I_{\text{avg}} * R$. Trying to bound the resistance between a block and its power sources, we can alleviate IR-drop. If some blocks cannot obtain enough voltage for proper operation, the violation of IR-drop requirement will occur.

B. ΔI Noise Constraint

In general, the SSN voltage should be less than some peak voltage for a circuit to operate properly [28]. Here, we define this peak voltage as the upper bound on ΔV for a block, which is given by the intellectual property (IP) vendor. Let x_{ij} be the amount of current delivered from the power supply bump p_i to block b_j , $\delta(x_{ij}) = 1$, if $x_{ij} > 0$, which means the current delivering path from p_i to b_j will be used, $\delta(x_{ij}) = 0$ if $x_{ij} = 0$, and let $(dI/dt)_j$ be the maximum rate of current change during transition at block b_j , which is assumed given from IP vendor. Let L_i be the parasitic inductance for power supply bump p_i , which is described in the technology file, and let L_{ij} be the effective wire inductance from the power supply bump p_i to the

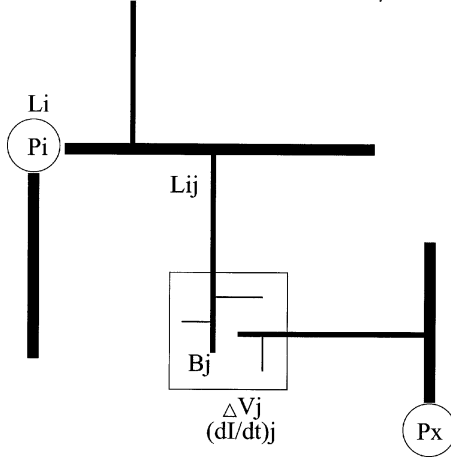


Fig. 4. Relationship between power supply bump and circuit block. The circuit block can obtain several power supply bumps to deliver power, as long as the noise constraint is not violated.

center of block b_j .² Also, let S_j be the set of all power supply bumps that connect to block b_j , let ΔV_j be the upper bound on ΔV for block b_j , and let $w_{ij} = d_{ij} / \sum_{k \in S_j} d_{kj}$ be the weight calculated from the distance between the power supply bump p_i and block b_j . We define the parasitic voltage drop from package to power supply bump p_i as

$$\Delta V_{\text{package}} = \sum_h \delta(x_{ih}) L_i \frac{\left(\frac{dI}{dt}\right)_h}{\sum_{k \in S_h} w_{kh} \delta(x_{kh})}.$$

We sum up all the $L(dI/dt)$ values from p_i to all the blocks to which the power supply bump delivers power to. This is to reflect the sharing of power sources by adding all the inductive induced voltage drop associated with the power sources. Also, each $L(dI/dt)$ value is divided by the weighted number of power supply bumps which deliver power to each block in the set S_h ($\sum_{k \in S_h} w_{kh} \delta(x_{kh})$) due to the sharing of power demand. We also define the inductive induced voltage drop from p_i to b_j as

$$\Delta V_{\text{wire}} = L_{ij} \frac{\left(\frac{dI}{dt}\right)_j}{\sum_{k \in S_j} w_{kj} \delta(x_{kj})}.$$

The summation of these two parts for each p_i and b_j , which is the total ΔI noise induced voltage drop, should be less than or equal to the upper bound on ΔV for block b_j

$$\Delta V_{\text{package}} + \Delta V_{\text{wire}} \leq \Delta V_j.$$

Block b_j can work properly only when the inductive induced voltage drop from package to p_i and from p_i to b_j do not exceed this bound. Fig. 4 shows the relationship between power supply bump and circuit block.

²Before a design is approved for manufacturing, it is essential to accurately assess inductance. During the floorplanning stage, however, much of the detailed information needed for assessing inductance is still unknown. So, at this stage, we use a simple model where the effective wire inductance is proportional to the distance between the center of the block and power supply bump. This part is for self-inductance only. From [32] and [33], the mutual inductance could be on the order of one third or less of the self-inductance and we consider it as lumped inductance.

C. Problem Formulation

The goal of this paper is to search for feasible power delivery distribution with the reduction of the distance between power supply bumps and circuit supply connections, and power supply noise minimization, i.e., we try to satisfy the demand of current and power for every block with delivery path resistance bounded and to avoid possible power supply noise during floorplanning. In area-array designs, I/O pads/cells can be placed inside the die and they need to be driven directly by power sources. In that case, we can simply treat I/O pads/cells as small circuit macros in our problem formulation.

Problem 2.1: Given a floorplan of n blocks b_1, \dots, b_n and their minimum current requirements d_1, \dots, d_n , respectively, and given a set of m power supply bumps p_1, \dots, p_m and the maximum current they can deliver s_1, \dots, s_m , respectively, find a feasible solution such that each circuit block b_j obtains d_j from power supply bumps, and each power supply bump p_i delivers current s_i or less. In addition, the resistance of the delivering path from power supply bumps to blocks should be bounded. Meanwhile, the power delivery assignment needs to meet the ΔI noise constraint

$$\left[\sum_h \delta(x_{ih}) L_i \frac{\left(\frac{dI}{dt}\right)_h}{\sum_{k \in S_h} w_{kh} \delta(x_{kh})} \right] + \left[L_{ij} \frac{\left(\frac{dI}{dt}\right)_j}{\sum_{k \in S_j} w_{kj} \delta(x_{kj})} \right] \leq \Delta V_j, \text{ for each } p_i, b_j \text{ such that } \delta(x_{ij}) = 1 \quad (1)$$

where those terms are defined in Section II-B.

III. POWER SUPPLY PLANNING WITH NOISE AVOIDANCE

In order to handle the power supply planning problem along with static IR-drop and noise constraints to be met, we need to develop reasonable and efficient strategies to deal with the constraints. In this section, we define a feasible power supply region to consider the IR-drop requirement, then introduce the construction of a special network for power supply planning based on a feasible power supply region for noise avoidance. In preserving the advantage of polynomial time max-flow algorithm, we also develop an effective algorithm to deal with the ΔI noise constraint. In addition, we introduce power zones to further reduce the size of the network graph for large designs.

A. Feasible Power Supply Region (FPSR)

We bound the resistance between a block and its power sources to reflect the IR-drop constraint. Given the current requirement and the upper bound on ΔV for a block, we can derive a region that is an expansion of the block in all four directions by a distance r . Such a region is referred to as the feasible power supply region (FPSR) for the block. Only the power supply bumps within the FPSR of a block can deliver power to the block. In Fig. 5, the FPSR of block b_2 is within the dashed lines, meaning four bumps $p_1 - p_4$ can deliver power to block b_2 .

B. Constrained Network Formulation

In this section, we then construct a special network graph and run a modified max-flow algorithm [34] based on the FPSR to

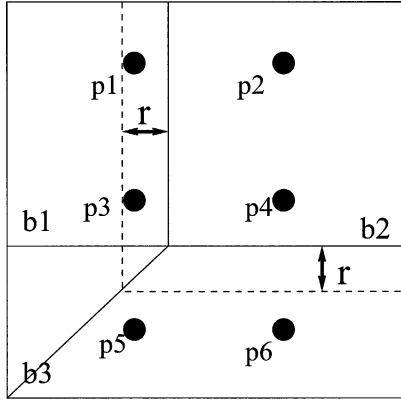


Fig. 5. Floorplan and the available power supply bumps. A circuit block can use the power supply bumps within its feasible FPSR.

solve the problem. The graph consists of two kinds of vertices besides the source s and the sink t : the circuit block vertices $B = \{b_1, b_2, \dots, b_n\}$ and the power supply bump vertices $P = \{p_1, p_2, \dots, p_m\}$. To simplify the presentation, we use the same name for a vertex and for the corresponding circuit block or power supply bump interchangeably.

The network graph $G = (V, E)$ is constructed as follows. There is an edge from the source s to every power supply bump vertex and there is an edge from every circuit block vertex to the sink t . The edge capacity from the source s to a power supply bump vertex p_i is s_i , which is the maximum current that can be delivered by p_i . The edge capacity from a circuit block vertex b_j to the sink t is d_j , which is the minimum current that is required by b_j . There is an edge from p_i to b_j if p_i is inside the FPSR of b_j . If such an edge exists, the edge capacity is set to ∞ . We wish to find the maximum flow from the source s to the sink t that satisfies the edge capacities and mass balance constraints at all nodes. We can state the problem formally as follows.

Minimize v

Subject to

$$\sum_{j:e_{ij} \in E} x_{ij} - \sum_{j:e_{ji} \in E} x_{ji} = \begin{cases} v, & \text{for } i = s \\ 0, & \text{for all } i \in V - \{s, t\} \\ -v, & \text{for } i = t \end{cases} \quad (2)$$

$$\left[\sum_h \delta(x_{ih}) L_i \frac{\left(\frac{dI}{dt}\right)_h}{\sum_{k \in S_h} w_{kh} \delta(x_{kh})} \right] + \left[L_{ij} \frac{\left(\frac{dI}{dt}\right)_j}{\sum_{k \in S_j} w_{kj} \delta(x_{kj})} \right] \leq \Delta V_j, \text{ for each } p_i, b_j \text{ such that } \delta(x_{ij}) = 1. \quad (3)$$

We refer to $x = \{x_{ij}\}$ satisfying (2) as a flow and the corresponding value of the scalar variable v as the value of the flow. x_{ij} is the amount of current delivered from p_i to b_j , $\delta(x_{ij}) = 1$ if $x_{ij} > 0$, $\delta(x_{ij}) = 0$, otherwise. $(dI/dt)_j$ is the maximum rate of current change during transition at b_j . L_i is the parasitic inductance for p_i and L_{ij} is the effective wire inductance from p_i to the center of b_j . S_j is the set of all power supply bumps that connect to b_j , ΔV_j is the upper bound on ΔV for b_j , and $w_{ij} = d_{ij} / \sum_{k \in S_j} d_{kj}$ is the weight calculated from the distance between p_i and b_j .

Fig. 6 illustrates the construction of the network graph for the floorplan example in Fig. 5. Block b_2 can get power supply

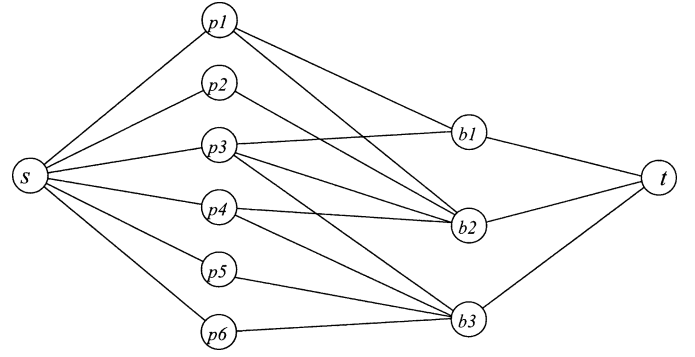


Fig. 6. Network graph captures the current and power demand of the circuit blocks, and the current and power that power supply bumps can provide in Fig. 5.

bumps $p_1 - p_4$ to deliver power, as shown in Fig. 5. The feasible power supply regions of block b_1 and b_3 are not shown in Fig. 5, where block b_1 can get power supply bumps p_1 and p_2 to deliver power, and block b_3 can get power supply bumps $p_3 - p_6$ to deliver power. Note that in Fig. 6 some power supply bump vertices can be connected to two circuit block vertices or more because a power supply bump can supply power to several circuit blocks at the same time, as long as the demanded current and power never exceeds the maximum amount that can be delivered by the power supply bump.

Any flow from the source to the sink in the network assigns current delivering from a power supply bump to a circuit block. If there is a feasible power supply planning solution satisfying all power requirement of the circuit blocks, the total flow on every edge from the circuit block vertex to the sink should equal to the edge capacity. It can be shown that our network flow algorithm optimally solves the power supply planning problem if we do not consider the other constraint we have introduced. We have the following theorem.

Theorem 3.1: A maximum flow in the network graph corresponds to a power supply planning solution which maximizes the amount of current and power delivered from the power supply bumps to the circuit blocks. A feasible solution with respect to FPSRs for all blocks exists if and only if all edges from the circuit block vertices to the sink are saturated.

As can be seen in the problem definition, the side constraints are nonlinear, so it may be treated as an NP-hard or an approximately NP-hard problem. We cannot use min-cost max-flow/min-cut or maximum bipartite matching algorithms to optimally solve this problem. In the following section, we introduce an efficient yet effective algorithm to minimize the violations of the ΔI noise constraint and still obtain maximum flow.

C. Priority_Augmenting_Path Algorithm

In this section, we describe a priority-based heuristic to deal with the power supply noise constraint in the max-flow algorithm. In the Ford-Fulkerson method [35], we try to find any augmenting path to increase the flow. However, randomly picking a feasible augmenting path may cause serious violations for the noise constraint in power delivery planning. Fig. 7 shows the constraint violation example when not carefully

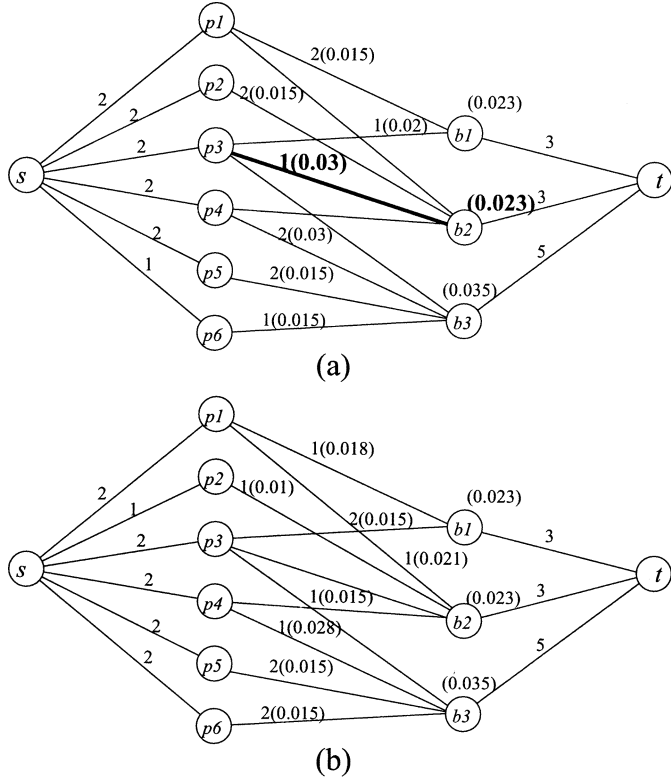


Fig. 7. Numeric examples include two max-flow solutions of the network graph from Fig. 6. Those numbers are calculated from the technology file, given IP parameters, and the estimation models used earlier. The darker numbers and the edge show that there is a ΔI noise constraint violation. The number on the edge is the amount of flow on that edge. The number inside the parentheses on the edges between power supply bumps and blocks is the amount of inductive induced voltage drop on that edge. The number inside the parentheses above the block node is the upper bound on ΔV for the block. (a) The solution with randomly choosing augmenting path. For example, $e(p1, b1)$ has 0.015 V for inductive induced voltage drop, which does not exceed $\Delta V_1 = 0.023$ V. However, for $e(p3, b2)$, it has 0.03 V, which exceeds $\Delta V_2 = 0.023$ V, indicating a violation. (b) The solution using the algorithm in Section III-C. There is no ΔI noise constraint violation.

augmenting the flow. Due to this observation, we implement an efficient algorithm to decide the order of finding augmenting paths based on the priority assigned on the edges between power supply bump vertices and block vertices in our network.

The main point is that we want to choose a path or edge with either low inductive induced voltage drop or large ΔV for the block to augment the flow. The reason for low inductive induced voltage drop is obvious: We want to deliver power via low voltage drop to blocks; the reason for large voltage tolerance of blocks on inductive induced voltage is that delivering power to small ΔV blocks is harder due to the cleaner power supply requirement. We use the following implementation to realize these two rationales.

We assign the cost first to reflect the rough inductive induced voltage drop without the effect of sharing the power demand of the block. The cost for edge e_{ij} from p_i to b_j is $c_{ij} = (dI/dt)_j * (L_i + L_{ij})$. We then assign priority values for the edges between p_i and b_j as follows. Note that for the forward and backward direction of the edges, we should assign different priority values so that the preferred augmenting path can be found. For the forward direction, the priority value $P_{ij} = (c_{ij}/N_j) + (1/\Delta V_j)$; for the

backward direction, the priority value $Q_{ji} = (N_j/c_{ij}) + \Delta V_j$, where N_j is the current number of power supply bumps which deliver power to block b_j . N_j needs to be updated whenever we obtain an augmenting path and augment the flow since the intermediate flow solution has been modified.

During the process of finding an augmenting path, we can use the priority values to select a preferred path. In this way, finding the augmenting path which minimizes the violations of the noise constraint can be accomplished. We have the following algorithm.

Algorithm Priority_Augmenting_Path

begin

$x := 0$;

while $G(x)$ contains a directed path from s to t **do**

 Identify an augmenting path U from s to t based on priority of the edge from some power supply bump to some block;

$\nu := \min\{r_{ij} : e_{ij} \in U, i, j \in V\}$;

 Augment ν units of flow along U ;

 Update $G(x)$ and $N_k, k \in B$;

end

end

In the algorithm, x is the flow vector, $G(x)$ is the residual network, r_{ij} is the residual capacity for edge e_{ij} , and ν is the residual capacity of the augmenting path U [34].

1) *Complexity Analysis*: We use the Edmonds–Karp algorithm to implement pure max-flow problem, where the runtime is $O(nm^2)$, and where $n = |V|$ and $m = |E|$ [35]. To be more specific, the number of iterations is at most $O(nm)$ and each iteration of the Ford–Fulkerson method can be implemented in $O(m)$ time using breadth-first search (BFS). We can use the Fibonacci heap to implement priority queue and obtain the logarithmic runtime in operations. In addition, the dequeue and enqueue operations in BFS both take $O(1)$ time originally, but in our proposed algorithm, they take $O(\lg n)$ time. The update of the number of power supply bumps which deliver power to blocks can be done in $O(nm)$ since they are only updated when we obtain augmenting paths. The runtime of the priority augmenting path algorithm hence is $O(nm(n \lg n + m))$. We have the following corollary.

Corollary 3.2: The priority augmenting path algorithm with prioritized breadth-first search solves the max-flow problem and heuristically minimizes side constraint violations in $O(n \lg n + m)$ time. Hence, the modified Edmonds–Karp algorithm runs in $O(nm(n \lg n + m))$ time.

D. Graph Reduction by Power Zones

Although the proposed approach runs correctly, there can be numerous power supply bump vertices in the network graph when the number of power supply bumps is large, making the graph size large. In this section, we introduce “power zones” to reduce the network graph size. A power zone represents the collaborative efforts of the power supply bumps in the proximity.

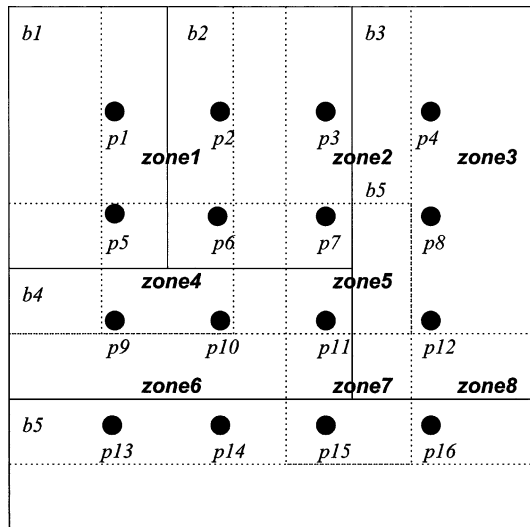


Fig. 8. Power zones in a floorplan.

By introducing power zones, the number of power supply bump vertices is reduced from the graph. This simplification gives a power supply planning as good as the method previously described, but at a reduced CPU time for running the network flow algorithm.

Precisely, power zones are the disjoint regions bounded by the boundaries of FPSRs (see Fig. 8). The network graph is then constructed as follows. Similarly, there is an edge from the source s to every power zone vertex and there is an edge from every circuit block vertex to the sink t . Again, the edge capacity from a circuit block vertex b_i to sink t is still d_i . However, the edge capacity from source s to power zone vertex z_j is set to be the sum of the maximum amount the power supply bumps inside the corresponding power zone can deliver, i.e., $\sum_{p_k \in z_j} s_k$. There is an edge from power zone z_i to block b_j if z_i is inside the FPSR of b_j . If such an edge exists, the edge capacity is again set to be ∞ .

Here, we show a way to obtain power zones out of a floorplan. First, we allocate a “zone index” (which is a binary number) for each power supply bump. Depending on which FPSR’s power supply bump is contained, a proper zone index is set. This can be done by setting the bits (in the binary number) corresponding to the FPSRs which contain the power supply bump to be one, and keeping the remaining bits at zero. The detail of this is best explained by an example.

Consider a floorplan in Fig. 8. The power supply bump p_7 is contained by the FPSRs of blocks b_2 , b_3 , and b_4 . We set second, third, and fourth bits in a binary number to be one and keep other bits to be zero. Therefore, the zone index of p_7 is set to $b'01110$. Similarly, the zone index of p_{11} will be $b'01110$; this means they are in the same zone. On the other hand, the zone index of p_{10} will be $b'01011$, since p_{10} is inside the FPSRs of blocks b_1 , b_2 and b_4 . Because the zone index of p_{10} is different from those of p_7 and p_{11} , p_{10} is in a different power zone. By sorting power supply bumps according to the zone index, power supply bumps in the same power zone can be easily clustered in $O(m \lg m)$ time.

IV. FLOORPLANNING WITH POWER SUPPLY PLANNING AND NOISE AVOIDANCE

Our floorplanning algorithm with simultaneous power supply planning and noise avoidance is based on the Wong–Liu floorplanning algorithm [15]. Recall that the Wong–Liu algorithm uses Polish expressions to represent floorplans and searches for an optimal floorplan using simulated annealing by iteratively generating Polish expressions. Once a Polish expression is examined, the shapes of the blocks are optimized and the total wirelength is used as the interconnect cost. In this paper, in addition to optimizing total wirelength and chip area, we propose performing simultaneous power delivery planning and power supply noise avoidance design with respect to the current floorplan being considered and, as a result, obtain a much better floorplan with fewer power supply noise constraint violations.

We choose to optimize the floorplan in fixed die context in this paper, but our approach can also comply with the objective of minimizing chip area in floorplanning. In fact, it is intuitive to implement this feature in shape curve computation. During shape curve computation of the floorplan generation in minimal area and wirelength, we can search for the nearest point on the final shape curve to match the given aspect ratio of the fixed die. In this way, we will not obtain the solution which has too small value of the x or y dimensions in a shape curve and, eventually, we can obtain the floorplans which are inside the fixed die.

The cost function used to evaluate a floorplan in [15] is $A + \lambda W$, where A is the total area of the packing, W is the half-perimeter estimation of the interconnect cost, and λ is a constant which controls the relative importance of these two terms. In this paper, we use the cost function $\alpha A + \beta W + \gamma P$ for floorplanning with simultaneous power supply planning and noise avoidance, where A can be either total area of the packing or fixed die penalty if using fixed die implementation, which is zero if the area of the floorplan is within the fixed die and is the difference between the area of the current floorplan and fixed die area otherwise, W is total wirelength estimation,³ and P is the power supply cost penalty, which is positive if the current floorplan cannot find a max-flow solution and/or obtain the violations of power supply noise constraint and is zero if there is a max-flow solution and no constraint violations for current floorplan. The coefficients α , β , and γ are constants that control the relative importance of the three terms.

V. EXPERIMENTAL RESULTS

We have tested our approach on some Microelectronics Center of North Carolina (MCNC) building block benchmarks. All experiments were carried out on a 650-MHz+ Pentium III processor. The minimum amount required by a circuit block and the maximum rate of current change during transition at a circuit block are roughly proportional to its area. The power supply bumps are in a regular array structure and the maximum amount of power they can deliver are all the same. (In fact, our approach can be applied to other equivalent structures.) The values of parasitic and wire inductance and other technology

³Here, we use simplified model for timing constraint since we consider floorplans which need immediate attention to power supply planning and signal integrity issues.

TABLE I
COMPARISON OF OUR APPROACH WITH [15] AND [23] ON MCNC BENCHMARKS. THE WIRELENGTH DATA ARE DESCRIBED IN SECTION V

Data	Block#	Traditional Floorplanner [15]		Floorplanner with Power Supply Planning [23]			Simultaneous PSP-NA		
		IR-drop Vio(%)	Noise Vio(%)	IR-drop Vio(%)	Noise Vio(%)	Time (hr)	IR-drop Vio(%)	Noise Vio(%)	Time (hr)
apte	9	0	54	0	54.6	0.2	0	3.9	0.24
xerox	10	0	61	0	61.4	0.6	0	9.1	0.44
hp	11	27.3	65	0	60.4	0.11	0	7.3	0.1
ami33	33	31.3	48	3.1	45.1	1.3	3.1	9.9	1.7
ami49	49	4.1	62	0	44.6	3.6	0	7.6	3.74
Average		12.54	58	0.62	53.2		0.62	7.5	

parameters are from ITRS'97 roadmap [36], 0.18 μm . As for bump pitch, we use the scaling number from [31]. In order to show the effectiveness of our approach, we implement three algorithms: 1) the traditional approach without any power supply planning consideration [15], 2) the approach with rough IR-drop requirement consideration in power supply planning [23], and 3) the feature approach in simultaneous power supply planning and noise avoidance.

Table I shows the comparison between the floorplans obtained from our approach, those obtained from a traditional floorplanner in [15] without any power supply planning consideration, and those obtained from the approach (in [23]) with supply-demand-only power supply planning consideration during the annealing process. All the floorplans obtained are within a fixed die area with 7% dead space. We use the IR-drop requirement violation and noise constraint violation (in percentage) to reflect the effectiveness of our approach. Since we use FPSR to bound the power delivering path's resistance to prevent static IR-drop violation, we thus use a percentage, which is the number of blocks that obtain insufficient current and power due to IR-drop normalized by total number of blocks, to show the IR-drop requirement violation. The ΔI noise constraint violation percentage is the number of power supply bump-block edge constraint violations normalized by the number of total power supply bump-block edges in the network. From Fig. 7, we can see that if there is no violating edge in the network graph, the ΔI noise constraint violation percentage is 0%. The floorplans obtained from our approach have far fewer IR-drop violations, over which is 50% improvement on the ΔI noise constraint violations, and less than 5% of the total wirelength increase on average compared with the floorplan obtained in [15]. We have listed the CPU time for those benchmarks, in which we spent less than 4 h for ami49.

VI. DISCUSSION

Here, we discuss some issues that are worth mentioning in floorplanning and power supply planning. We have seen the execution time for MCNC benchmarks in Section V. In fact, those benchmarks are modified for the purpose of experimentation in this paper, since there are no benchmarks specified for power supply planning and noise avoidance experiments. We can actually modify GSRC benchmarks to fulfill the purpose of experimentation as well. However, for larger problems such as the 300-block problem in Gigascale Silicon Research Center (GSRC) benchmarks, it will take a substantially longer

runtime to obtain the results. One possible way to speed up the runtime is to take advantage of the nature of simulated annealing. Like [19], we can use multistage simulated annealing, which uses different cost functions in different stages of the optimization process. This approach can save running time without sacrificing the quality of the result. Another alternative is to partition the floorplan into supermodules to reduce the problem size for simulated annealing [37].

In Section II-A, we mention that the effective resistance for pad transfer metal from a block to a power supply bump is proportional to the distance between the center of the block and power supply bump $\text{dist}(b, p)$; actually, it is not very accurate. At the granularity level of a floorplan, it is possible that there are multiple power supply bumps associated with a block. Moreover, if we consider a block with large height: width ratio (assume width \gg height), it is possible for this block to tap a power supply bump that is located along the width of the block and further away from the boundary with the effective resistance. In order to reflect a more accurate estimation of the effective resistance, we have two possible approaches. One is to compute different effective resistances for width and height (r_w and r_h) of blocks which have a large height : width ratio. In this case, we do not use uniform effective resistance to be extended in both directions for tapping power supply bumps, but will slightly increase the complexity of the problem. Another one is that we can chop large blocks into smaller modules, thus $\text{dist}(b, p)$ becomes $\text{dist}(b_i, p)$, where power supply bump p belongs to small module b_i , $b = \cup_i b_i$. However, there is a tradeoff between accurate estimation and the size of the graph we use in our algorithm. We can adapt from experienced parameters to adjust between better estimation and problem size.

We have formulated the problem in Section II-C, where we treat two constraints IR-drop and Ldi/dt independently and separately. In fact, since the drop in the supply network is the sum of the static IR-drop and the inductive induced drop, ideally these two should not be treated separately. We consider them separately for simplified and conservative modelings. Typically, an IP block specifies the minimum voltage required to meet specifications, and we consider the worst case scenario that we bound the IR-drop and let it be a fixed value. Thus, the upper bounds on ΔV for blocks become the difference between the specification and the IR-drop bound. The reason we consider the constraints in separate worst-case bounds is because the circuit should operate correctly even under the worst-case scenarios [24]. However, we can actually combine these two constraints using the

same algorithm. We can simply change ΔV_j in Section III-C to be dynamically updated when we take the difference between the static IR-drop and the maximum permitted drop for each power supply bump-block edge. This alternative approach, nevertheless, cannot use precomputed values for ΔV_j , and it needs a small amount of additional spaces.

VII. CONCLUSION

We have presented an approach to simultaneously solving power supply planning and noise avoidance in floorplan design. The efficient yet effective priority-based heuristic we have introduced ensures the polynomial time max-flow algorithm for this difficult problem and experimental results are encouraging. With a slight increase of total wirelength, we can obtain a big improvement on IR-drop and ΔI noise constraint violations in the floorplanning stage.

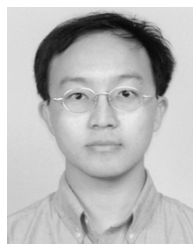
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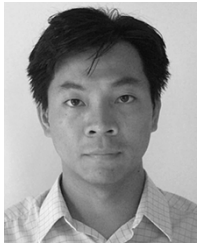
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