A Novel PHINES Flash Memory Cell with Low Power Program/Erase, Small Pitch, Two-Bits-Per-Cell for Data Storage Applications

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***Abstract*—A novel programming by hot-hole injection nitride electron storage (PHINES) Flash memory technology is developed. The memory bit size of 0.046 μm^2 is fabricated based on 0.13-μm technology. PHINES cell uses a nitride trapping storage cell structure. Fowler–Nordheim (FN) injection is performed to raise V_t in erase while programming is done by lowering a local V_t through band-to-band tunneling-induced hot hole (BTBT HH) injection. Two-bits-per-cell feasibility, low-power and high-speed program/erase, good endurance and data retentivity make it a promising candidate for Flash EEPROM technology in gigabit era applications.**

***Index Terms*—Band-to-band hot hole (BTB HH), charge gain, charge loss, EEPROM, Flash memory cell, Flash memory, nitride storage, over-erasure.**

I. Introduction

INTEREST in nitride-based localized trapping storage Flash memory cells has revived for 10-min-cell operation, which can double the memory density [1]–[3]. Besides, they also show better scalability since charges are stored in nitride traps rather than a polysilicon floating-gate in conventional Flash memory cells. Nitride storage memories do not have floating-gate-induced drain turn-on and coupling issues, which are believed to be the scaling limitations of conventional floating-gate memories [4], [5]. Various operation schemes were proposed based on the nitride-storage cell structure. SONOS Flash memory with modified Fowler–Nordheim (FN) tunneling programming by electrons and direct-tunneling erasing by holes was proposed a long time ago [6]. The absence of erratic bits and low power operation make SONOS a good candidate for next generation Flash technology. However, the cell retention is still an issue now [7]. Besides, its large cell size ($6F^2$ per bit [6]) and slow program/erase (P/E) speeds limit its applications. Recently, NROM cell with channel-hot-electron (CHE) programming and band-to-band tunneling induced hot hole (BTBT HH) erasing [2] has demonstrated excellent intrinsic cell performance. In spite of many advantages, previous works [8]–[13] reveal that reliability issues including read disturb, over erase and cell retention after cycling are major challenges of a NROM cell. Swift *et al.* proposed to use uniform tunneling for erasing [3] instead of the HH injection to reduce stress induced degradation in erase. However, for mass data storage, CHE programming is still not suitable due to its high power consumption.

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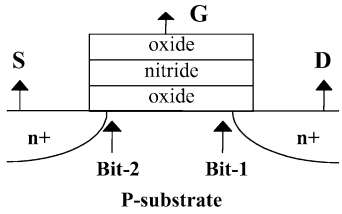

Fig. 1. Schematic representation of a PHINES cell structure.

In this paper, a novel PHINES cell [1] is proposed based on the nitride storage cell structure. PHINES cell, with its superior reliability, virtual ground array, two-bits-per-cell storage and low power operation, can meet the need of high-density data storage. In addition, PHINES cell with one-bit-per-cell storage has a larger operation window and sensing current, which is suitable for code storage application. Sections II and III will discuss the cell structure and operation principles. Section IV demonstrates its reliability characteristics. Finally, a conclusion will be made in Section V.

II. PHINES Cell Structure

The PHINES memory cell is a NMOSFET with an ONO stack as the gate dielectric (Fig. 1). The key cell parameters are listed in Table I. The test single cell structure is arranged in a virtual-ground array as shown in Fig. 2, which is free of field isolation. The gate length and gate width are 0.19 and 0.14 μm, respectively. A double poly technology, novel low-temperature dielectric film fill-in and planarization process is introduced to form a sufficiently thick insulating layer between the local buried-diffusion (BD) bit-lines and the wordlines (WLs) [14]. Fig. 3(a) and (b) shows the TEM pictures of the cell, in which the X-pitch and Y-pitch are 0.33 and 0.28 μm, respectively. The thickness of each ONO layer is 9, 6, and 6 nm from top to bottom. The top oxide and bottom oxide are formed by thermal oxidation while nitride is performed by chemical vapor deposition. Unit cell as small as 0.092 μm^2 $(5.46F^2)$ is achieved by using 0.13-μm technology and the bit size of 0.046 μm^2 $(2.73F^2)$ is realized with two-bits-per-cell storage. Although

TABLE I
KEY CELL PARAMETERS

Design rule	0.13μm
Gate Length	0.19μm
WL Width	0.14μm
BL Width	0.14μm
Unit Cell Area	0.092μm^2
Unit Bit Area	0.046μm^2
Bottom Oxide	6nm
Nitride	6nm
Top Oxide	9nm

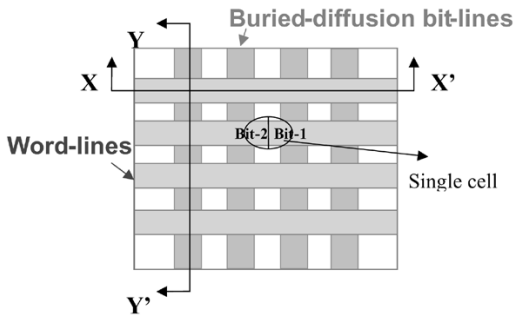

Fig. 2. Array architecture of a test single cell structure.

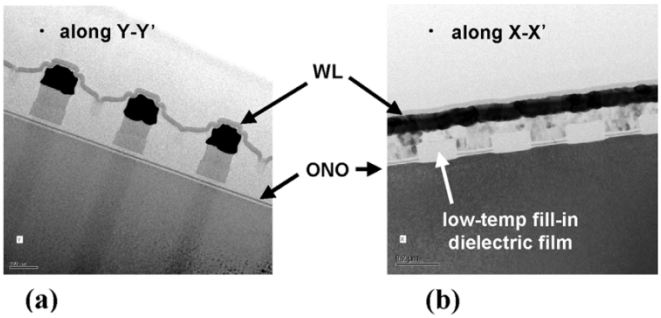

Fig. 3. TEM pictures of a PHINES cell along (a) Y-Y′ and (b) X-X′ (refer to Fig. 2).

PHINES cell can be operated in NOR and NAND array, we only focus on the single-cell characteristics and operation mechanisms in this paper.

III. CELL OPERATION PRINCIPLE

PHINES cell uses gate FN injection (negative gate-to-substrate bias) and BTBT HH injection as the erase and program methods, respectively. The bias conditions are given in Table II. Schematic representations of PHINES cell operation are shown in Fig. 4. Fig. 5 shows the erasing characteristics and the V_t is almost saturated after 1 ms. As shown in Fig. 6, electrons are injected from the gate via tunneling through the top oxide (path 1) in erase operation. Some of the tunnel electrons are captured by the traps (path 2) of the nitride (either deep traps or shallow traps), while the others will inject into the substrate (path 3). Electrons in the shallow traps will easily be drawn out due to the high electric field (path 4) and only electrons in deep traps remain in the nitride. Accordingly, the erase saturation may be caused by the limited amount of deep nitride traps

TABLE II
PHYSICAL MECHANISMS AND BIAS CONDITIONS FOR PHINES CELL OPERATION. PLEASE REFER TO FIG. 1 FOR THE CORRESPONDING TERMINALS AND BIT-1 AND BIT-2 IN A PHINES CELL

		Program (BTBT HH)	Erase (-Vg FN)	Read (Backward)
Bit-1	Vg	-6V	-7V	3V
	Vd	5V	F	0V
	Vs	0V	F	1.6V
	Vb	0V	10V	0V
Bit-2	Vg	-6V	-7V	3V
	Vd	0V	F	1.6V
	Vs	5V	F	0V
	Vb	0V	10V	0V

and cell V_t will saturate while all deep traps are filled with electrons. PHINES cell does not have an over-erasure problem due to the self-convergent behavior by FN injection, which can help improve the uniformity and tighten the V_t distribution of the erased cells.

The program of a PHINES cell is done by lowering a local V_t through edge BTBT HH injection. Fig. 7 shows the program characteristics of the two bits. In Fig. 7(a), Bit-1 is programmed to a low V_t, while Bit-2 is in the erased state. Bit-2 is subsequently programmed in Fig. 7(b). Since the program is done by bit-by-bit, and shot-by-shot tracking, a verify step is applied after each program shot to well control the program behavior of each bit. The program of each bit stops as its V_t or current passes the program verify. Over-program induced low V_t state leakage between two columns can be suppressed, and tight current and V_t distributions of the program state can be achieved. Read of a PHINES cell is performed by a backward-read scheme as shown in Table II. To read Bit-1 (Bit-2), a source (drain) bias is applied to reduce the channel potential near Bit-2 (Bit-1). The current–voltage (*I–V*) characteristics of each state are shown in Fig. 8. Figs. 9 and 10 show the P/E cycling endurance of one-bit-per-cell and two-bits-per-cell operation, respectively. The V_t window is almost unchanged up to 10-K P/E cycles. A slight window closure is observed after 100-K cycles, which should result from the stress induced degradation of the ONO film.

The electrical performance of a PHINES cell is summarized in Table III. Program can be finished within 200 μs and erase can be done in 2 ms. V_t-windows of 2 and 1.2 V are obtained for one-bit-per-cell and two-bits-per-cell operation. Since the program current is less than 50 nA/bit, high programming rate can be achieved by parallel programming. Besides, FN-erase also consumes extremely low current (10 fA/cell). Both program and erase are low power operations, which makes it suitable for mass storage (data Flash) applications.

IV. CELL RELIABILITY

Fig. 11 shows the data retention characteristics of three P/E states. V_t loss is less than 0.5 and 0.2 V for high-V_t bits and low-V_t bits, respectively, after 150 °C, 168-h bake in 10 K P/E

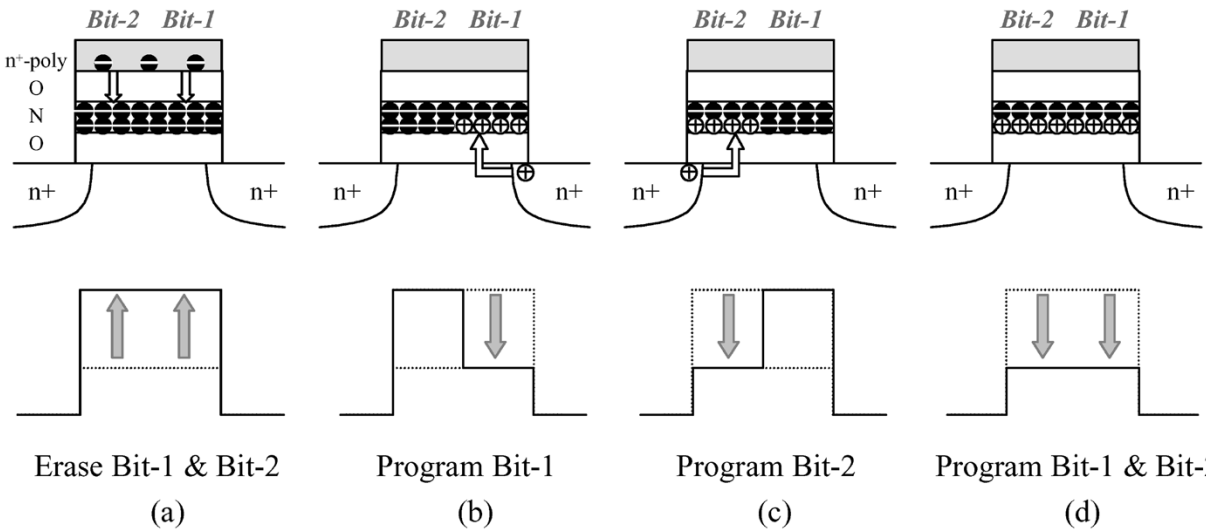

Fig. 4. Schematic representation of charges stored in a PHINES cell (top) and channel surface potential (bottom) with two-bits storage. (a) Bit-1 and Bit-2 at erased state. (b) Bit-1 at programmed state and Bit-2 at erased state. (c) Bit-1 at erased state and Bit-2 at programmed state. (d) Bit-1 and Bit-2 at programmed state.

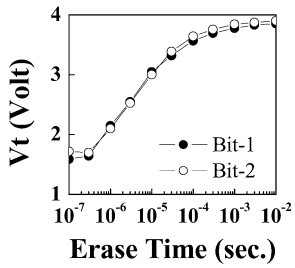

Fig. 5. Negative FN erase characteristics of a PHINES cell. Threshold voltage (V_t) is defined as the applied gate voltage at which the drain current is 1 μA.

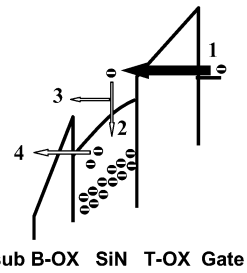

Fig. 6. Schematic representation of electrical field during negative FN injection in PHINES erase operation.

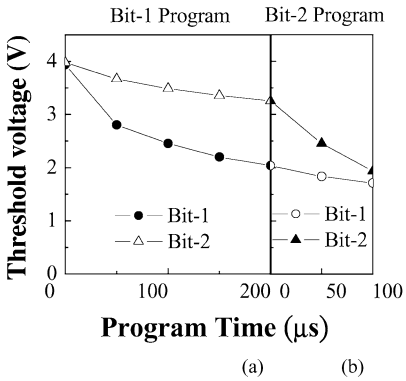

Fig. 7. Programming characteristics of a PHINES cell. (a) Bit-1 is programmed to low V_t while Bit-2 is maintained at high V_t. (b) Bit-2 is programmed to low V_t while Bit-1 is maintained at low V_t.

cycled cells. Fig. 12 shows the temperature effect on data retention in a high V_t state. Three storage temperatures are compared: 25 °C, 85 °C, and 150 °C. Excellent data retention is obtained. In previous studies [15], hot electron injection tends to fill traps

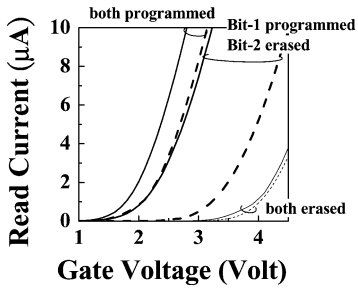

Fig. 8. *I–V* characteristics of three cell states (both bits are erased, one bit is programmed and the other bit is erased, both bits are programmed). Solid line represents the *I–V* of Bit-1 and dash line represents the *I–V* of Bit-2. The cells are fresh cells.

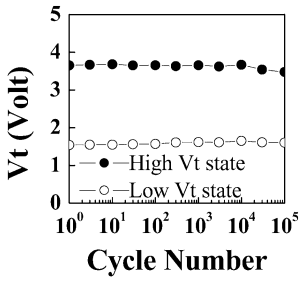

Fig. 9. Endurance behavior of one-bit-per-cell application.

with shallower energy in a stressed oxide film. We also use this characterization method to monitor the nitride effect. High V_t state charge loss behavior of two electron injection techniques (FN injection and substrate hot electron injection) is compared in Fig. 13. Two devices are stressed by constant voltage stress ($V_g = -24$ V, $V_d = V_s = V_b = 0$ V) for 1000 s. After stress, HH injection is performed to lower the V_t of the devices. Finally, FN injection and substrate hot electron (SHE) injection are used to inject electrons into two devices to raise V_t to 5 V, respectively. V_t shift is measured in the high temperature condition (150 °C). As shown in Fig. 13, the device with FN electron injection shows less charge loss than the device with SHE injection. It is surmised that hot electrons in SHE will jump over the oxide barrier and are randomly captured by deep and shallow

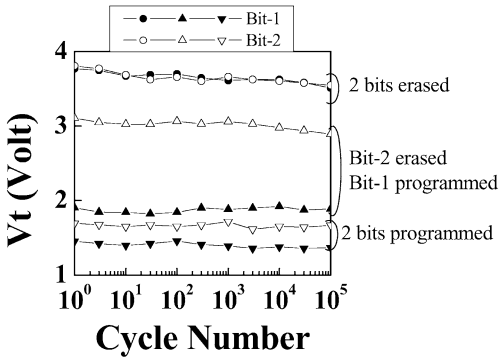

Fig. 10. Endurance behavior of two-bits-per-cell application. The cycle is repeated by erase ⇒ Bit-1 program ⇒ Bit-2 program. Circles represent that both bits are at high V_t. Up-triangles represent that Bit-1 is at low V_t and Bit-2 is at high V_t. Down-triangles represent that both bits are at low V_t.

TABLE III
THE ELECTRICAL PERFORMANCE OF A PHINES CELL. THE V_t WINDOW IN THE TABLE DENOTES THE INITIAL OPERATION WINDOW, WHICH DOES NOT INCLUDE CHARGE LOSS, READ DISTURB, AND OTHER RELIABILITY MARGINS

Program Current	< 5x10^{-8}A/bit
Erase Current	<10^{-14}A/bit
Program Time	200μs/page
Erase Time	2 ms/sector
Vt Window - 1 Bit	2 Volts
Vt Window - 2 Bit	1.2 Volts

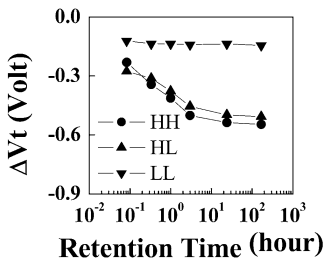

Fig. 11. Data retention (V_t loss) versus bake time of three P/E states. The storage temperature is 150 °C. The cells are 10 K P/E cycled.

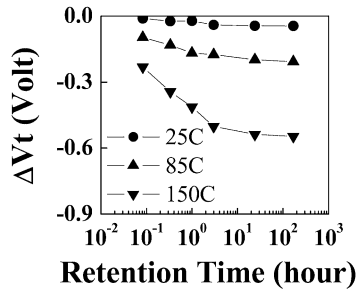

Fig. 12. Temperature effect on data retention in a high V_t state. The cells are 10 K P/E cycled.

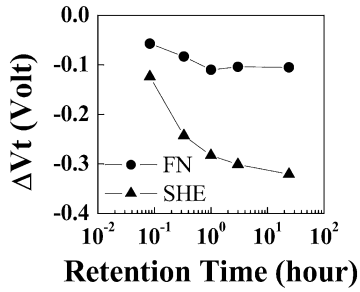

Fig. 13. Effects of electron injection methods on high V_t state charge loss at high temperature of 150 °C. After stress of $V_g = -24$ V for 1000 s, two devices are conditioned to high V_t state ($V_t = 5$ V) by two electron injection methods and V_t shift is measured. Two electron injection methods are FN ($V_g = -8$ V, $V_b = 10$ V) injection and SHE injection ($V_g = 2$ V, $V_s = V_d = 0$ V, $V_{\mathrm{PWELL}} = -6$ V, $V_{\mathrm{NWELL}} = -7$ V).

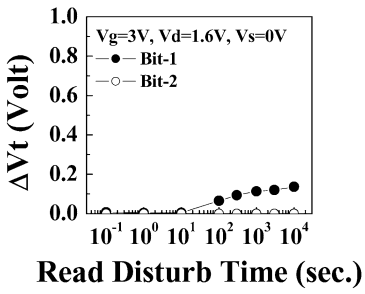

Fig. 14. Read disturb evaluation of a PHINES cell.

traps of nitride. Electrons in shallower traps will easily escape during a storage period and charge loss is observed. However, tunnel electrons by FN injection tend to stay in deep traps of nitride since electrons in shallow traps will be drawn out by high electric field as shown in Fig. 6. According to the Frenkel–Poole model, electrons in deeper traps have longer emission time and good data retention is obtained accordingly.

Read disturb is another reliability issue for Flash memory. As the device is in low V_t states, continuously reading the device will induce disturbance due to the high channel current and hot electron injection. V_t will increase and the read current will degrade accordingly. We also evaluate the read disturb characteristics of a PHINES cell. As shown in Fig. 14, the read condition ($V_g = 3$ V, $V_d = 1.6$ V, and $V_s = 0$ V to read Bit-2) is applied to the device while two bits are both at low V_t state (V_t is around 2 V). The V_t shift of both bits is measured. A V_t drift of 0.2 V is observed in Bit-1 by continuous read of 10 000 s while there is almost no disturbance in Bit-2. The reason is that a high voltage is applied on the drain, which induces hot electron injection at the drain side. Accordingly, the V_t of Bit-1 increases due to hot electron injection and no V_t shift is observed in Bit-2. Likewise, continuously reading Bit-1 ($V_g = 3, V_d = 0$, and $V_s = 1.6$ V) will cause hot electron injection at the source side, which will cause read disturbance in Bit-2.

V. CONCLUSION

PHINES unit cell size of 0.092 μm^2 achieved by 0.13 μm technology is demonstrated. The low power P/E operation, good endurance and data retention, two-bits-per-cell feasibility (0.046 μm^2/bit), as well as its simpler process and absence of floating-gate interference issues, make it a promising candidate for future Flash EEPROM technology.

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During 1991 to 1993, he worked on the modeling and simulation of field emission devices and developed a three-dimensional vacuum microelectronic field emission device simulator. After two years of military service, he joined Macronix International Company, Ltd., Hsinchu, in 1995 as a Device Engineer. From 1995 to 2000, he has been engaged in simulation, modeling, and design of nonvolatile memory devices. Since 2000, he has been working on the development of nitride-storage Flash memory technology, including the novel device concepts, reliability physics, test chip design, and scaling feasibility.His current research focuses on the device characterization and reliability physics of nonvolatile memory devices.

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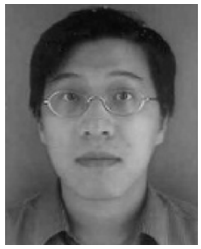

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In 1987, he joined Rapro Technology, Fremont, CA, as a co-founder with the responsibility on RTPCVD reactor design and process development. From 1991 to 1992, he was with Paradigm Technology, San Jose, CA, where he worked on 0.35-μm 4-Mb SRAM technology development. In 1992, he joined LSI Logic, Santa Clara, CA, where he worked on advanced logic technology development and served as Integration Manager of the R&D Division until 1997. He joined the Technology Development Division of the Macronix International Company, Hsinchu, Taiwan. He currently leads Technology Development Center and is responsible for the development of advanced nonvolatile memory and embedded SOC technologies. He has published more than 30 papers in technical journals and conferences.

Chih-Yuan Lu (M'77–SM'84–F'94) received the B.S. degree from National Taiwan University, Taipei, Taiwan, R.O.C., in 1972, and the Ph.D. degree in physics from Columbia University, New York, NY, in 1977.

He was a Professor at National Chiao-Tung University, Hsinchu, and then with AT&T Bell Labs from 1984 to 1989. He later joined ERSO/ITRI in 1989 as a Deputy General Director responsible for the MOEA grand Submicrometer Project. This project successfully developed Taiwan's first eight-inch manufacturing technology with high- density DRAM/SRAM. In 1994, he become the co-founder of Vanguard International Semiconductor Corporation, which is a spin-off memory IC company from ITRI's Submicrometer Project. He was the Vice President of Operation, Vice President of R&D, and later President from 1994 to 1999. He is the chairman and CEO of Ardentec Corporation, a VLSI testing service company and also serves Macronix International Company (MXIC), Ltd, Hsinchu, as a Senior Vice President/CTO. He led MXIC's technology development team to successfully achieve the state-of-the-art nonvolatile memory technology and is now responsible for MXIC's overall memory operation. He has published more than 100 papers and has been granted 123 international patents.

Dr. Lu and was elected a Fellow of the APS. He also received the IEEE Millennium Medal, and the semiconductor R&D Award in Taiwan from Pan Wen Yuan Foundation. He was also granted the National Science & Technology Achievement Award by the Prime Minister of Taiwan because of his leadership and achievement in ITRI's Submicrometer Project.