# A Novel Program-Erasable High-$\kappa$ AlN–Si MIS Capacitor

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***Abstract*—We demonstrate a programmable-erasable MIS capacitor with a single layer high-$\kappa$ AlN dielectric on Si having a high capacitance density of $\sim$ 5 fF/$\mu$m$^2$. It has low program and erase voltages of $+4$ and $-4$ V, respectively. Such an erase function is not available in other single layer $Al_2O_3$, AlON, or other known high-$\kappa$ dielectric capacitors, where the threshold voltage ($V_{th}$) shifts continuously with voltage. This device exhibits good data retention with a $V_{th}$ change of only 0.06 V after 10 000 s.**

***Index Terms*—Capacitor, erase, high-$\kappa$, program.**

## I. Introduction

FOR analog and RF [1]–[6] ICs and memory applications, capacitors with a high capacitance density are preferred. It is also desirable to have a program-erasable capability. This is especially important for RF ICs where process variations can shift the resonance frequency of LC tank away from designed values, creating impedance mismatches and bandpass frequency differences [6]. Program-erasable capacitors can also extend the data retention for DRAMs leading to less frequent re-flashing cycles. In this letter, we propose and demonstrate an MIS capacitor on Si using a single layer of high-$\kappa$ AlN dielectric, which exhibits the program-erase function as well as good data retention. The single-layer high-$\kappa$ capacitor has a programmable capacitance–voltage ($C$–$V$), which can be erased by $-4$ V bias for 1 ms. In contrast, this does not occur for high-$\kappa$ $Al_2O_3$ or AlON capacitors. The possible erase mechanism may be due to the smaller bandgap ($E_G \sim 5.0$ eV) or $\Delta E_V$ of AlN compared with $Al_2O_3$, which could permit hole injection or electron tunneling out of high density of trap states. After $10^4$ s, the program-erase cycle showed good retention of threshold voltage ($V_{th}$) shift of only 0.06 V.

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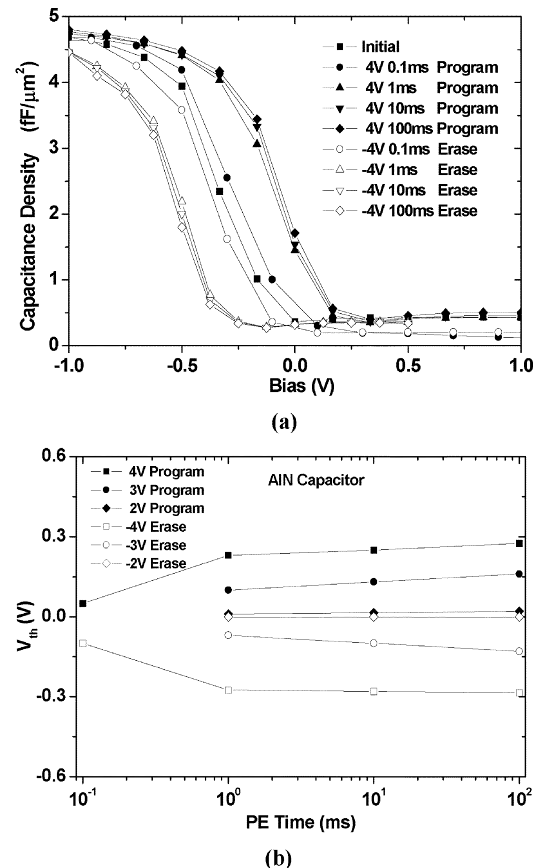


Fig. 1. (a) Measured $C$–$V$ characteristics, and (b) the threshold $V_{th}$ as a function of the duration of the applied voltage, for a single-layer high-$\kappa$ AlN-Si MIS capacitor. The program and erase properties were obtained by applying voltages from $\pm 2$ to $\pm 4$ V, respectively.

## II. Experimental Details

The MIS capacitors were fabricated using low temperature high-$\kappa$ dielectric process [1]–[14] on 4-in 5–10 $\Omega$-cm p-type Si wafer. The device layout is similar to the high-$\kappa$ MIM capacitor used in RF circuits [1], [2], [5]. First, the $n^+$ doping region is formed to connect the bottom plate of capacitor (similar to source/drain to connect channel). Then 500-nm isolation $SiO_2$ was deposited. After defining active capacitor area, an AlN dielectric of 16 nm was deposited by PVD system and annealed at 400 °C for 5 min in a furnace under $N_2$ ambient. Finally, Al metal were deposited and patterned to form top electrodes with capacitors area of 100 $\mu$m$\times$ 100 $\mu$m. (Note that the processing at 400 °C low temperature would permit integration into the back

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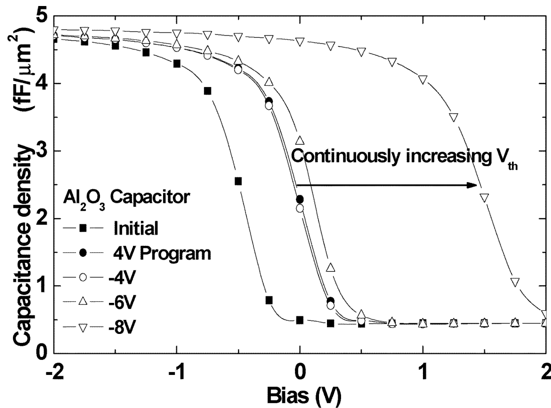
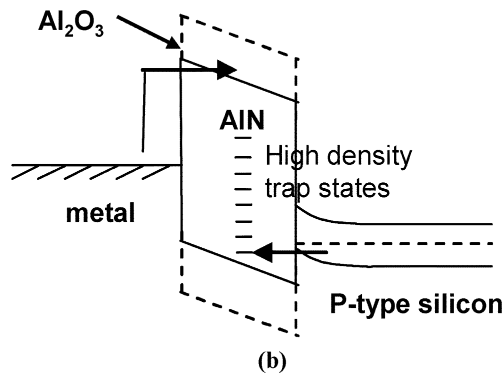
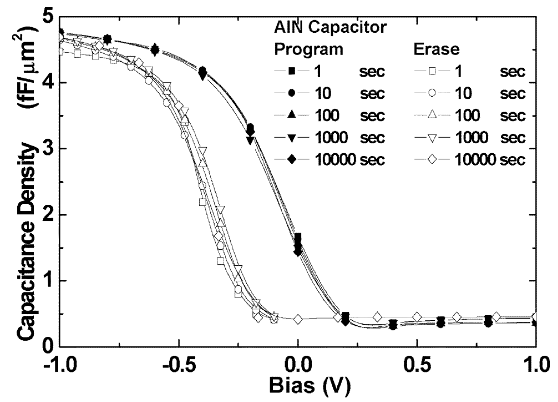



(a)

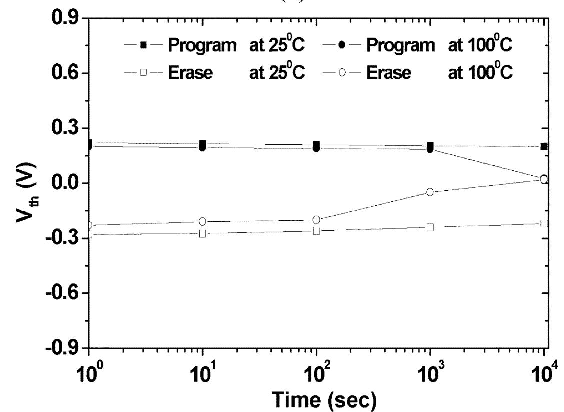



(b)

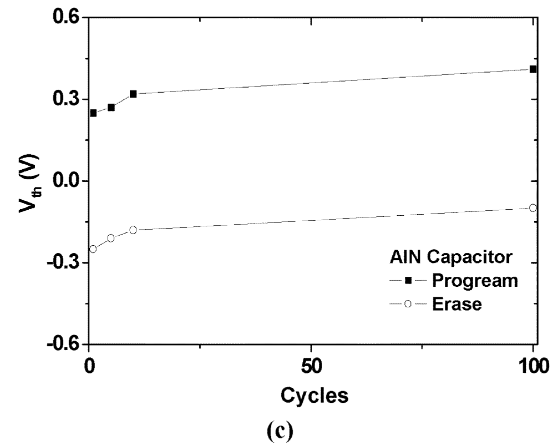
Fig. 2. (a) Measured $C$–$V$ characteristics of a high-$\kappa$ single-layer $Al_2O_3$ dielectric on Si and (b) the schematic band diagram of the metal-gate/dielectric/Si capacitor.




(a)




(b)




(c)

Fig. 3. (a) $C$–$V$ characteristics of an AlN MIS capacitor used for retention, measured from 10 to 10 000 s after removing the 1 ms $+4$ V program or $-4$ V erase voltage. (b) The threshold $V_{\mathrm{th}}$ as a function of retention time, derived from (a) and (c) the cycling property of Al–AlN–Si capacitor.

end of a VLSI fabrication line.) For comparison, we also fabricated single layer $Al_2O_3$, AlON, and $Si_3N_4$ capacitors. All the $C$–$V$ characteristics were measured by HP4284A at 1 MHz, and a pulse generator was used for the program and erase study.

## III. Results and Discussion

Fig. 1(a) and (b) shows the measured $C$–$V$ characteristics and time dependence of the $V_{\mathrm{th}}$ shift for a high-$\kappa$ AlN MIS capacitor. The capacitor was measured under applied $\pm 2$ to $\pm 4$ V voltages for times from 0.1 to 100 ms. The $V_{\mathrm{th}}$ shifts increase with increasing applied voltage. The $V_{\mathrm{th}}$ shifts of 0.24 V for $+4$ V, and of $-0.27$ V for $-4$ V applied for 1 ms shows that the AlN capacitor can be programmed or erased, similar to SONOS memory [15]. In sharp contrast, only a few millivolts of $V_{\mathrm{th}}$ changes are measured in $Si_3N_4$–Si capacitor fabricated by VLSI backend process with close capacitance density. The larger hysteresis of $C$-$V$ curve indicates the stronger carrier trapping (higher density and/or deeper energy of traps) in the AlN device than that of $Si_3N_4$ capacitor. The $|V_{\mathrm{th}}|$ increase largely with increasing program-erase time from 0.1 to 1 ms and gradually saturates from 1 to 100 ms, suggesting a switching speed of $\sim$ 1 ms at 4-V bias. The feature of nearly symmetrical positive and negative $V_{\mathrm{th}}$ for program and erase functions is important for low-voltage applications. In addition, high-capacitance density of $\sim$ 4.8 fF/$\mu$m$^2$ and low leakage current of $6 \times 10^{-8}$ A/cm$^2$ at $-2.5$ V are measured in high-$\kappa$ AlN dielectric capacitor, which are close to those for high-$\kappa$ $Al_2O_3$ MIM capacitors reported before [1], [2]. The high capacitor density is especially important for backend capacitor [1]–[7] due to the very thick equivalent oxide thickness (EOT) $> 5$ nm and hence the low leakage current. On the other hand, low leakage current is one of the most important factors for high-$\kappa$ gate dielectric with typical EOT $\leq 1.5$ nm [8]–[14]. The capacitor density of AlN–Si device is also much higher than that for SONOS capacitors [15].

Fig. 2(a) shows data for the high-$\kappa$ $Al_2O_3$ capacitors. The $Al_2O_3$ capacitor has nearly the same capacitance density and the close $V_{\mathrm{th}}$ shift with AlN capacitor. However, continuous increasing $V_{\mathrm{th}}$ with increasing applied negative voltage at top

Al electrode is measured without erase function, which may be due to increasing trapped negative charges in the high-$\kappa$ dielectric [15]. Similar features, without the erase function, are found in the AlON capacitor, even for $-10$ V applied voltages. No such erase function is reported for other known high-$\kappa$ SiN dielectric [4], [5] and it seems to be unique for high-$\kappa$ AlN dielectrics. Fig. 2(b) shows the schematic band diagram of metal-gate/high-$\kappa$/Si capacitor. The possible erase mechanism may arise from the smaller bandgap ($E_G \sim 5.0$ eV) or $\Delta E_V$ for AlN compared with $Al_2O_3$. This could permit hole injection or electron tunneling out from the high density of trap states, which is less possible for large $E_G$ $Al_2O_3$.

In Fig. 3(a) we show the retention behavior of an AlN capacitor after program or erase voltages of $+4$ or $-4$ V, from 10 to 10 000 s. Good program-erase retention properties are evident from the small shift of the $C$–$V$ curves at up to 10 000 s after removing the 1-ms program-erase voltage. To evaluate the program-erase retention property further, Fig. 3(b) shows $V_{\mathrm{th}}$ as a function of time, as derived from the measured $C$–$V$ curves in Fig. 3(a). The extended time retention is preserved with only a small $V_{\mathrm{th}}$ change of only 0.06 V, after removing the write voltage for 10 000 s. However, the memory window is closed quickly at a raised temperature of 100 °C. Fig. 3(c) shows the cycling property. The memory window remains almost unchanged although a $V_{\mathrm{th}}$ shift of 0.15 V is measured for both on- and off-state. Further improvement is required to extend the high temperature retention and cycling, although these results are already useful for DRAM improvement.

## IV. Conclusion

We have demonstrated a program-erasable high-$\kappa$ AlN–Si MIS capacitor with good retention. This novel program-erasable capacitor with high-capacitance density of $\sim$ 5 fF/$\mu$m$^2$, low voltage of $\pm$4-V operation, good retention property and low temperature process compatible with VLSI backend line should find wide applications for 1T1C static-dynamic memory and program-erasable varactor for RF ICs.

## References


[1] S. B. Chen, J. H. Chou, A. Chin, J. C. Hsieh, and J. Liu, "High density MIM capacitors using $Al_2O_3$ and $AlTiO_x$ dielectrics," *IEEE Electron Device Lett.*, vol. 23, no. 2, pp. 185–187, Feb. 2002.

[2] S. B. Chen, C. H. Lai, A. Chin, J. C. Hsieh, and J. Liu, "RF MIM capacitors using high-K $Al_2O_3$ and $AlTiO_x$ dielectrics," in *Proc. MTT-S Int. Microwave Symp.*, vol. 1, 2002, pp. 201–204.

[3] D. Coolbaugh, E. Eshun, R. Groves, D. Harame, J. Johnson, M. Hammad, Z. He, V. Ramachandran, K. Stein, S. S. Onge, S. Subbanna, D. Wang, R. Volant, X. Wang, and K. Watshon, "Advanced passive devices for enhanced integrated RF circuit performance," in *Proc. RF-IC Symp.*, 2002, pp. 341–344.

[4] T. Soorapanth, C. P. Yue, D. K. Shaeffer, T. H. Lee, and S. S. Wong, "Analysis and optimization of accumulation-mode varactor for RF ICs," in *Symp. VLSI Circuits Dig.*, 1998, pp. 32–33.

[5] M. Y. Yang, C. H. Huang, A. Chin, C. Zhu, B. J. Cho, M. F. Li, and D. L. Kwong, "Very high density RF MIM capacitors (17 fF/$\mu$m$^2$) using high-$\kappa$ $Al_2O_3$ doped $Ta_2O_5$ dielectrics," *IEEE Microw. Wireless Compon. Lett.*, vol. 13, no. 10, pp. 431–433, Oct. 2003.

[6] C. Zhu, H. Hu, X. Yu, A. Chin, M. F. Li, and D. L. Kwong, "Voltage temperature dependence of capacitance of high-K $HfO_2$ MIM capacitors: A unified understanding and prediction," in *IEDM Tech. Dig.*, 2003, pp. 379–382.

[7] C. H. Lai, C. F. Lee, A. Chin, C. H. Wu, C. Zhu, M. F. Li, S. P. McAlister, and D. L. Kwong, "A tunable and program-erasable capacitor on Si with long tuning memory," in *Proc. RF-IC Symp. Dig.*, 2004, pp. 259–262.

[8] D. S. Yu, A. Chin, C. C. Laio, C. F. Lee, C. F. Cheng, W. J. Chen, C. Zhu, M.-F. Li, S. P. McAlister, and D. L. Kwong, "3D GOI CMOSFETs with novel $IrO_2$(Hf) dual gates and high-$\kappa$ dielectric on 1P6M-0.18 $\mu$m-CMOS," in *IEDM Tech. Dig.*, 2004, pp. 181–194.

[9] D. S. Yu, K. C. Chiang, C. F. Cheng, A. Chin, C. Zhu, M. F. Li, and D. L. Kwong, "Fully silicided NiSi:Hf–$LaAlO_3$/smart-cut-Ge-on-insulator n-MOSFETs with high electron mobility," *IEEE Electron Device Lett.*, vol. 25, no. 6, pp. 559–561, Jun. 2004.

[10] C. H. Huang, D. S. Yu, A. Chin, W. J. Chen, C. X. Zhu, M.-F. Li, B. J. Cho, and D. L. Kwong, "Fully silicided NiSi and germanided NiGe dual gates on $SiO_2$–Si and $Al_2O_3$–Ge-on-insulator MOSFETs," in *IEDM Tech. Dig.*, 2003, pp. 319–322.

[11] C. H. Huang, M. Y. Yang, A. Chin, W. J. Chen, C. X. Zhu, B. J. Cho, M.-F. Li, and D. L. Kwong, "Very low defects and high performance Ge-on-insulator p-MOSFETs with $Al_2O_3$ gate dielectrics," in *Symp. VLSI Tech. Dig.*, 2003, pp. 119–120.

[12] H. Iwai, S. Ohmi, S. Akama, C. Ohshima, A. Kikuchi, I. Kashiwagi, J. Taguchi, H. Yamamoto, J. Tonotani, Y. Kim, I. Ueda, A. Kuriyama, and Y. Yoshihara, "Advanced gate dielectric materials for sub-100 nm CMOS," in *IEDM Tech. Dig.*, 2002, pp. 625–628.

[13] A. Chin, Y. H. Wu, S. B. Chen, C. C. Liao, and W. J. Chen, "High quality $La_2O_3$ and $Al_2O_3$ gate dielectrics with equivalent oxide thickness 5–10 Å," in *Symp. VLSI Tech. Dig.*, 2000, pp. 16–17.

[14] A. Chin, C. C. Liao, C. H. Lu, W. J. Chen, and C. Tsai, "Device and reliability of high-$\kappa$ $Al_2O_3$ gate dielectric with good mobility and low $D_{it}$," in *Symp. VLSI Tech. Dig.*, 1999, pp. 135–136.

[15] C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, and K. Kim, "A novel SONOS structure of $SiO_2$/SiN/$Al_2O_3$ with TaN metal gate for multi-Giga bit flash memories," in *IEDM Tech. Dig.*, 2003, pp. 613–616.