Novel Program Versus Disturb Window Characterization for Split-Gate Flash Cell

Hung-Cheng Sung, Tan Fu Lei, Te-Hsun Hsu, Ya-Chen Kao, Yung-Tao Lin, and Chung S. Wang

***Abstract*—In this letter, a new methodology for program versus disturb window characterization on split gate Flash cell is presented for the first time. The window can be graphically illustrated in V_{wl} (word-line)-V_{ss} (source) domain under a given program current. This method can help us understand quantitatively how the window shifts versus bias conditions and find the optimal program condition. The condition obtained by this method can have the largest tolerance for program bias variations. This methodology was successfully implemented in 0.18-μm triple self-aligned (SA3) split-gate cell characterization to provide program condition for 32 M products.**

***Index Terms*—Disturb, Flash memory, operation window, program, split-gate.**

I. Introduction

THE split-gate Flash memory proposed by Silicon Storage Technology Inc. (SST) is commonly used in standalone and embedded nonvolatile memory because of the advantages of fast erase speed, high programming efficiency, and most important, no verification after program and erase. The erase is achieved by field-enhanced Fowler–Norheim (F–N) tunneling through sharp poly tip, and the program is accomplished by source-side hot carrier injection (SSI) [1], [2]. Although the above mechanisms provide good physics foundation for fast erase and program, a robust characterization methodology for determining operation condition is still crucial to guarantee reliable one shot program and erase. For erase condition, the window characterization is more straightforward because only word-line is biased. Generally, higher word-line voltage yields faster erase speed and better cycling performance [3]. The upper limit of erase voltage is constrained only by the reliability of word-lines and high voltage transistors. However, the program window characterization window characterization is much more difficult due to its complex bias conditions for both selected and unselected cells. A good program condition requires not only fast program efficiency on selected cells but also very limited disturb effect on unselected cells. In this letter, we convert the constraints on programming and disturb into clear graphical illustration and develop an easy methodology to find optimal program condition from single cell measurement.

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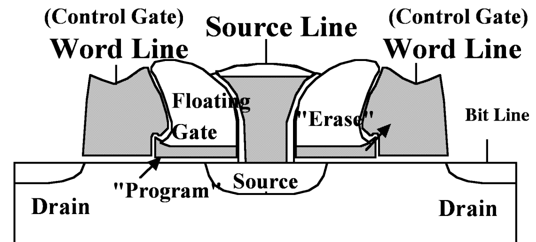

Fig. 1. Schematic diagram of the SA3 split-gate Flash memory cell in this letter. The erase is by field-enhanced F–N tunneling through sharp poly tip, and the program is accomplished by source-side hot carrier injection (SSI).

II. Device Fabrication

The Flash memory cells used in this letter were fabricated by 0.18-μm triple self-aligned (SA3) Split-gate Flash technology [4]. Drawing of the cross-section of the cell is shown in Fig. 1. Firstly, floating gate oxide is grown prior to floating gate poly deposition. Next, shallow-trench isolation (STI) is formed to become the first self-alignment to floating gate. After memory well implantation and thick nitride deposition, the region for floating gate and source line is defined and opened. Then, thick tetraethylorthosilicate (TEOS) spacers and source poly lines are formed to become second self-alignment, which is source-line to floating gate. After thick nitride is removed, floating gate is defined by TEOS hard mask, and high temperature oxide is deposited to act as tunneling oxide. Afterwards, word-line poly was deposited and etched to become spacer word-line, which is the third self-alignment to floating gate.

III. Program Versus Disturb Window Characterization

In split-gate Flash, programming is operated at following conditions. Source node (V_{ss}) biased at high voltage, word-line (V_{wl}) slightly turned-on and bit-line connected to a constant current source (I_{dp}). This program condition can cause three disturb stress modes which are: 1) column punch-through disturb (PTC); 2) row punch-through disturb (PTR); and 3) reverse tunneling disturb (RT) [5], [6]. The disturbed bits' location and stress conditions are shown in Fig. 2. The program time and disturb duration are determined by product specification and array architecture. In this letter, we use 32-M Flash as the target vehicle. The program time is 10 μs, and the disturb time for PTC, PTR, and RT is 1, 40, and 260 ms, respectively. For the criteria, the program specification is defined as "programmed state current (I_{r0}) smaller than 5% of erased state current (I_{r1})," and the disturb specification is defined as "cell current drop ratio ($\Delta I_{\mathrm{r1}}/I_{\mathrm{r1}}$) smaller than 10% after program disturb."

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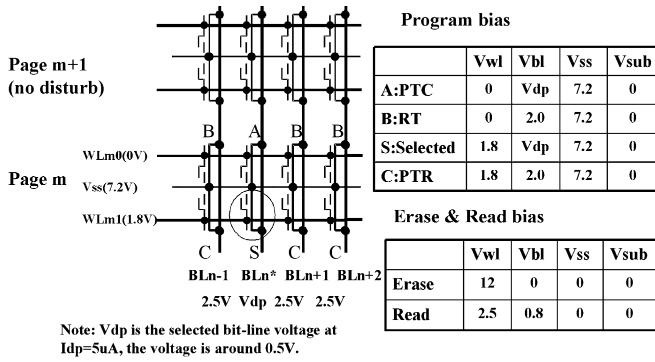

	Vwl	Vbl	Vss	Vsub
A:PTC	0	Vdp	7.2	0
B:RT	0	2.0	7.2	0
S:Selected	1.8	Vdp	7.2	0
C:PTR	1.8	2.0	7.2	0

	Vwl	Vbl	Vss	Vsub
Erase	12	0	0	0
Read	2.5	0.8	0	0

Fig. 2. Cell array and bias voltage for program, erase, readout and three disturb conditions, which are: (A)PTC, (B) PTR, and (C) RT. Note that the cells outside the selected page are immune from disturb stress.

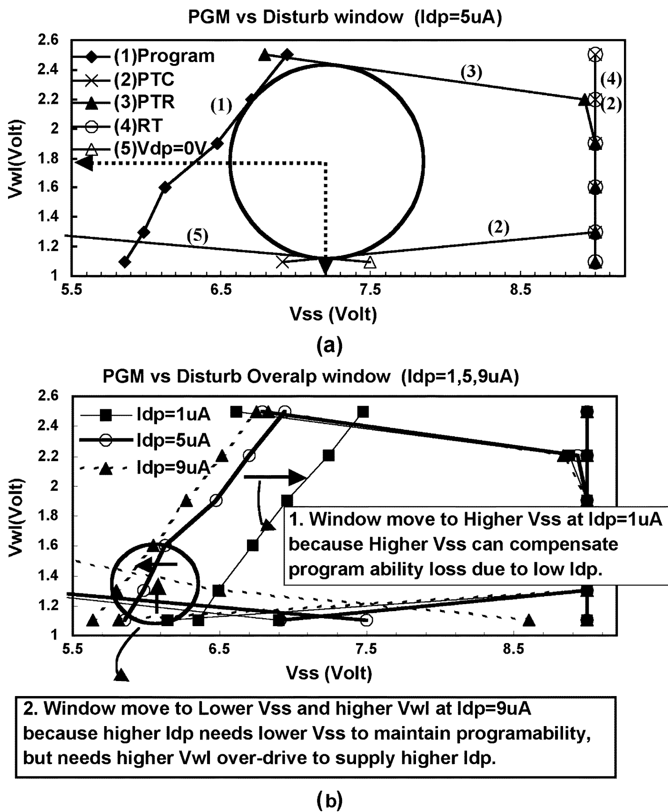

Fig. 3. (a) Program versus disturb window and the operation circle. The programming time is 10 μs and program current is 5 μA. (b) Program versus disturb window varies with $I_{\rm dp}$ from 1, 5 to 9 μA. Since the channel doping is well adjusted in this SA3 cell, no significant disturb boundary shift is observed under $I_{\rm dp}$ variation.

For a given program current ($I_{\rm dp}$) and program time, the program versus disturb window can be presented in $V_{\rm wl}$ (word-line)-$V_{\rm ss}$ (source) domain. The plot is shown in Fig. 3(a). A valid program condition must be enclosed by following five boundary conditions to guarantee fast programming and very limited disturb behavior. Note that the $V_{\rm ss}$ voltage is constrained at 9 V in this window characterization.

- *Curve 1: Programming.* The curve meets $I_{\rm r0} = 5\%$ of $I_{\rm r1}$ after 10 μs programming. The right lower side of curve 1 (higher $V_{\rm ss}$ and lower $V_{\rm wl}$) is the region passing program specification. The higher $V_{\rm ss}$ has better programming. Because it can supply more kinetic energy to the channel electrons and also attract more hot electrons to floating gate through source to floating gate coupling. While the effect of $V_{\rm wl}$ on programming is from the modulation of constant-current program circuitry; lower $V_{\rm dp}$ is accompanying with lower $V_{\rm wl}$ to maintain constant current programming, as a result, higher lateral field is induced by higher voltage drop between $V_{\rm ss}$ and $V_{\rm dp}$. Therefore, lower $V_{\rm wl}$ can have better programming.
- *Curve 2: PTC.* The curve meets $\Delta I_{\rm r1}/I_{\rm r1} = 10\%$ after 1-ms disturb. The source and bit lines of PTC are the same as the ones of programming selected bits, while the word-lines of PTC are grounded to turn off current. In real situation, some leakage can still exist and cause undesired injection under high source to drain voltage drop; as a result, PTC disturb gets worse at higher $V_{\rm ss}$ and lower $V_{\rm dp}$. Since $V_{\rm dp}$ decreases with $V_{\rm wl}$ in order to maintain constant current programming, the illustration of PTC disturb trend on $V_{\rm ss}$-$V_{\rm wl}$ domain is that the left upper side of the curve (lower $V_{\rm ss}$ and higher $V_{\rm wl}$) is the region passing PTC disturb specification.
- *Curve 3: PTR.* The curve meets $\Delta I_{\rm r1}/I_{\rm r1} = 10\%$ after 40-ms disturb. PTR happens on the same word-line of program selected bits, so the word-line is on and source line is bias at high voltage. To prevent undesired programming on erased cell, an inhibited voltage ($\sim$2 V at worst case) is applied on unselected bit lines to stop the leakage flowing from source to drain. However, the leakage can still exist and cause undesired programming if $V_{\rm wl}$ or $V_{\rm ss}$ is too high. Thus, PTR tends to happen under higher $V_{\rm wl}$ and $V_{\rm ss}$ voltage. The presentation of the trend on $V_{\rm ss}$-$V_{\rm wl}$ domain is that the bottom left side of curve 3 (lower $V_{\rm wl}$ and $V_{\rm ss}$) is the region passing PTR specification.
- *Curve 4: RT.* The curve meets $\Delta I_{\rm r1}/I_{\rm r1} = 10\%$ after 260-ms disturb. RT happens on the bits with source lines connected to high voltage, word-lines grounded and bit lines connected to inhibited voltage. The disturb mechanism is solely caused by reverse tunneling from word-line to floating gate and is only dependent on $V_{\rm ss}$ voltage. The trend is the higher the $V_{\rm ss}$ voltage, the worse the RT disturb. Therefore, the left side of the curve is the region passing RT specification.
- *Curve 5: Drain voltage during programming* $(V_{\rm dp}) = 0$V. The lower boundary of window is enclosed by $V_{\rm dp} = 0$ V. Beyond this boundary, $V_{\rm dp}$ will become negative voltage, which is not allowed in the design for this letter.

To find an optimal program condition from Fig. 3(a), a maximum circle, named as operation circle, is drawn within the enclosed window, and the circle center is chosen as the best program condition for a given $I_{\rm dp}$. The reason is that the circle center has largest voltage variation allowance for $V_{\rm wl}$ and $V_{\rm ss}$. Note that the scale at *X* and *Y* axes are kept the same.

Next step is to find the best $I_{\rm dp}$ setting. As shown in Fig. 3(b), we can see that the operation window changes with $I_{\rm dp}$. The reason of the window change is explained in Fig. 3(b). Comparing the maximum circle size between $I_{\rm dp} = 1, 5$, and 9 μA in Fig. 4, we can find that $I_{\rm dp} = 5$ μA has the largest circle size,

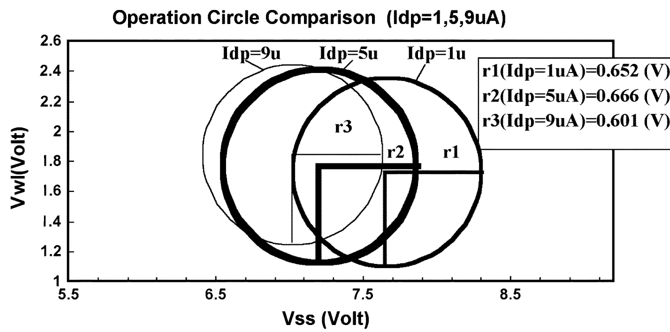

Fig. 4. Operation circle comparison between $I_{\rm dp} = 1, 5, 9\ \mu$A. The optimal program condition is chosen at r2 center ($I_{\rm dp} = 5\ \mu$A) because it has largest operation circle, the condition is $V_{\rm ss} = 7.2$ V, $V_{\rm g} = 1.75$ V, and $I_{\rm dp} = 5\ \mu$A.

which means 5 μA is the best program current setting. Therefore, we choose the center of operation circle at $I_{\rm dp} = 5\ \mu$A as the best program condition, which is: $V_{\rm s} = 7.2$ V, $V_{\rm wl} = 1.8$ V at $I_{\rm dp} = 5\ \mu$A. This methodology was successfully implemented in $0.18\ \mu$m SA3 single cell characterization to determine program setting for 32 M-product.

IV. Conclusion

A new methodology for program versus disturb window characterization in split gate Flash cell is presented in this letter for the first time. With this new methodology, the optimal program condition can be determined from single cell measurement. In addition, the quantitative window information can help us to evaluate the tradeoff clearly between various program settings.

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References

[1] S. Kianian, A. Levi, D. Lee, and Y.-W. Hu, “A novel 3 volts-only, small sector erase, high density Flash E^2PROM,” in *Symp. VLSI Tech. Dig.*, 1994, pp. 71–72.

[2] B. Yeh, “Single transistor non-volatile electrically alterable semiconductor memory device,” U.S. Patent 5 029 130, Jul. 1991.

[3] K. C. Huang, Y. K. Fang, D. N. Yaung, C. W. Chen, H. C. Sung, D.-S. Kuo, and C. S. Wang, “The impacts of control gate voltage on the cycling endurance of split gate Flash memory,” *IEEE Electron Device Lett.*, vol. 21, no. 7, pp. 359–361, Jul. 2000.

[4] R. Mih, J. Harrington, K. Houlihan, H. K. Lee, K. Chan, J. Johnson, B. Chen, J. Yan, A. Schmidt, C. Gruensfelder, K. Kim, D. Shum, C. Lo, D. Lee, A. Levi, and C. Lam, “$0.18\ \mu$m modular triple self-aligned embedded split-gate Flash memory,” in *Symp. VLSI Tech. Dig.*, 2000, pp. 120–121.

[5] M. G. Mohammad and K. K. Saluja, “Electrical model for program disturb faults in nonvolatile memories,” in *Proc. 16th Int.Conf. VLSI Design*, 2003, pp. 217–222.

[6] D. Wellekens, J. Van Houdt, L. Haspeslagh, J. Tsouhlarakis, P. Hendrickx, L. Deferm, and H. E. Maes, “Embedded HIMOS Flash memory in 0.35 μm and 0.25 μm CMOS technologies,” *IEEE Trans. Electron Devices*, vol. 47, no. 11, pp. 2153–2160, Nov. 2000.