A Novel Fully CMOS Process Compatible PREM for SOC Applications

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***Abstract*—A novel nonvolatile memory cell named programmable resistor with eraseless memory (PREM) is proposed for system on chip applications for the first time. PREM combines a novel "eraseless" algorithm and the progressive breakdown of an ultrathin oxide. No or one extra mask is needed with a standard CMOS process. Multitime programming, multilevel cell, nonvolatility, and low-voltage operation are realized. Good reliability is demonstrated based on the result of a single cell.**

***Index Terms*—Eraseless, multilevel cell (MLC), nonvolatile, multitime programming (MTP), progressive breakdown, programmable resistor with eraseless memory (PREM), system on chip (SOC).**

I. Introduction

THE diode programmable read only memory [1], [2] has been published for one-time programmable, low-cost, and high-density applications. This memory utilizes an antifuse diode structure, and the breakdown of gate oxide serves as a storage node. A high electrical field will induce gate oxide breakdown of the memory cell and an increase of the leakage current through the oxide results [1]. Previous studies [3]–[7] show that the oxide breakdown behavior in an ultrathin oxide device (<2 nm) is quite different from that in a thicker oxide. Fig. 1 shows the breakdown evolution of an MIS diode with an oxynitride film of 1.4 nm. The oxide breakdown evolves in a progressive way, and the leakage current increases gradually with stress time.

II. PREM Cell Structure and Operation Algorithm

Programmable resistor with eraseless memory (PREM) utilizes an antifuse cell structure [1]. The progressive nature of oxide breakdown in an ultrathin oxynitride film is used for memory storage. Table I discloses the PREM cell structure and its operation parameters. Since the cell structure is simple, no or one extra mask is needed with CMOS standard process to realize a PREM cell.

Fig. 1 shows the program voltage dependence of the read current evolution. All the cells are stressed at a high program voltage while the read current is measured at a low read voltage of 1.3 V. The voltage stress will cause the oxide breakdown and the oxide current increases progressively. The onset of the breakdown event and the evolution of the oxide leakage current depend strongly on stress voltages. Since the breakdown evolves in a progressive way, the read current can be programmed to any desired level by repeating voltage stress and program verification. Accordingly, a PREM cell can realize multilevel cell (MLC) to increase memory density. Fig. 1 also shows an example of three-bits-per-cell storage with seven reference current levels and eight storage levels. To perform MLC operation, the stress voltage and the stress time interval need to be optimized to precisely control program speed and read current evolution. In Fig. 1, some noise is observed at a lower stress voltage, which may affect the control of MLC operation. In a thinner dielectric film, the noise is reduced, although the mechanisms are still not clear.

Fig. 2 shows the operation algorithm of a PREM cell to realize multitime programming (MTP). In the first program operation with reference current ref-1, the device is stressed that the

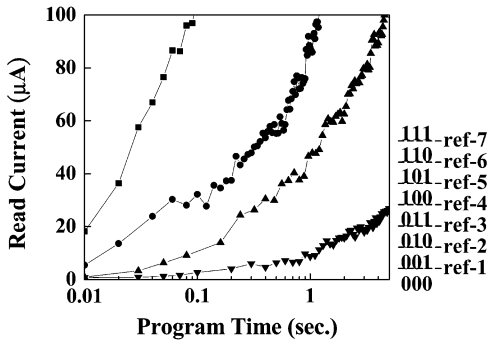
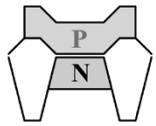


Fig. 1. Program voltage dependence of the read current evolution in a PREM cell. Four program voltages are compared: Vp-poly/Vn-diffusion $= 2.4/-2.4$ V (square), $2.2/-2.2$ V (circle), $2.0/-2.0$ V (up-triangle) and $1.8/-1.8$ V (down-triangle). The MLC operation (three-bits-per-cell) is also indicated. Ref-1, ref-2, ref-3, ref-4, ref-5, ref-6, and ref-7 represent seven reference levels in MLC operation.

TABLE I
PREM Cell Structure, Cell Parameters, and Program/Read Bias Conditions

Test pattern		MIS diode
Dielectric		Oxynitride 1.4nm
Area		2μm²
Program	P poly	0V~3V
	N diffusion	0V~-3V
Read	P poly	1.3V
	N diffusion	0V



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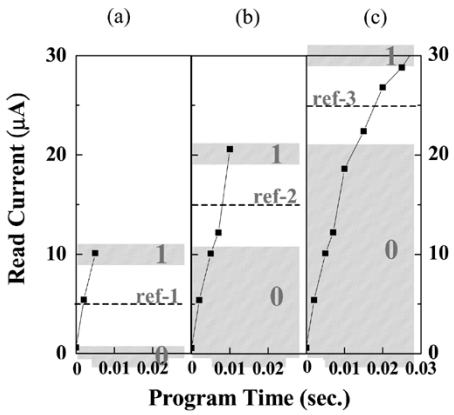

Fig. 2. Illustration of a PREM cell to realize MTP. (a), (b), and (c) are the schematic representations of the first, the second, and the third time program operations and ref-1, ref-2, and ref-3 are the reference currents for each program time.

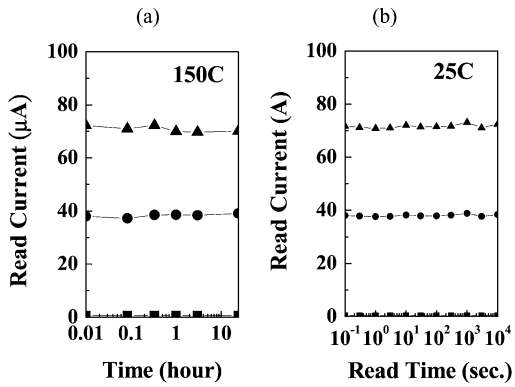

Fig. 3. (a) Cell retention behavior of three programmed levels. The storage temperature is 150 ° C. (b) The read disturbance behavior of three programmed levels. The disturbance condition is Vg-poly/Vn-diffusion = 1.3 V/0 V at a temperature of 25 °C.

read current reaches a desired level (higher than ref-1) where a bit is stored in [Fig. 2(a)]. To perform the second program operation [Fig. 2(b)], the reference level is switched to ref-2 that is higher than the read current of all cells (after the first program operation). All data are reset to "0" by changing/increasing the reference level. Subsequently, program voltages are applied to stress the selected cells to another specific read current level (higher than ref-2). The data of "1" are programmed in the selected cells while the others remain at "0" state. Fig. 2(c) shows the third program operation, which is repeated by increasing the reference level, resetting data to "0," and programming the selected cells to "1." The PREM cell utilizes a novel "eraseless" algorithm, which switches the reference level to reset the stored data instead of the "erase" operation in conventional flash memories (erase the V_t or the current back to the initial state). Since the pumping circuit can only supply limited operation power and the read current increases after each program operation, the PREM cell can only realize MTP.

The PREM cell can also combine the algorithms of MTP and MLC to meet the required applications. However, it is a tradeoff between the number of allowed programming times and the number of storage bits. If a higher storage density (more storage bits) is desired, the number of allowed programming times would reduce. The operation voltages of PREM cells are less than ± 3 V. PREM cells do not need high-voltage transistors and processes. General I/O CMOS devices can perform the operation.

III. PREM Cell Reliability and Its Applications

Fig. 3(a) shows the retention of a PREM cell at a temperature of 150 ∘ C. Three programmed levels are tested and no degradation is observed. Fig. 3(b) shows the read disturbance of three programmed levels and no read disturbance is observed under dc continuous reading for 10^4 s. PREM cells show good reliability, and the cell performance is better than conventional oxide-breakdown memory cells that can only perform one-time programming, and one-bit storage. The PREM cell is suitable for SOC applications due to its nonvolatility, low-voltage operation, simple cell structure, and fully CMOS process compatibility.

IV. Conclusion

We propose a novel nonvolatile memory cell named PREM. Instead of the conventional "erase" operation, the PREM cell adjusts the reference level to reset the data. By utilizing the progressive breakdown of an ultrathin oxide and the "eraseless" operation, a PREM cell can realize MTP and/or MLC and it can be easily integrated with advanced logic circuits and SRAM for SOC applications.

References

[1] C. de Graaf, P. H. Worelee, C. M. Hart, H. Lifka, P. W. H. de Vreede, P. J. M. Janssen, F. J. Sluijs, and G. M. Paulzen, "A novel high-density low cost diode programmable read only memory," *IEDM Tech. Dig.*, pp. 189–192, 1996.

[2] S. B. Herner, A. Bandyopadhyay, S. V. Dunton, V. Eckert, J. Gu, K. J. Hsia, S. Hu, C. Jahn, D. Kidwell, M. Konevecki, M. Mahajani, K. Park, C. Petti, S. R. Randigan, U. Raghuram, J. Vienna, and M. A. Vyvoda, "Vertical p-I-n polysilicon diode with antifuse for stackable field-programmble ROM," *IEEE Electron Device Lett.*, vol. 25, no. 5, pp. 271–273, May 2004.

[3] T. Wang, C. W. Tsai, M. C. Chen, C. T. Chan, and H. K. Chiang, "Negative substrate bias enhanced breakdown hardness in ultrathin oxide pMOSFETs," in *Proc. Int. Reliab. Phys. Symp.*, 2003, pp. 434–438.

[4] T. Hosoi, P. L. Re, Y. Kamakrura, and K. Taniguchi, "A new model of time evolution of gate leakage current after soft breakdown in ultrathin gate oxides," in *IEDM Tech. Dig.*, 2002, pp. 155–158.

[5] B. P. Linder, J. H. Stathis, D. J. Frank, S. L. Lombardo, and A. Vayshenker, "Growth and scaling of oxide conduction after breakdown," in *Proc. Int. Reliab. Phys. Symp.*, 2003, pp. 402–405.

[6] C. W. Tsai, M. C. Chen, S. H. Gu, and T. Wang, "Substrate bias dependence of breakdown progression in ultrathin oxide pMOSFETs," *IEEE Electron Device Lett.*, vol. 24, no. 4, pp. 269–271, Apr. 2003.

[7] F. Monsieur, E. Vincent, D. Roy, S. Bruyere, J. C. Vildeuil, G. Pananakakis, and G. Ghibaudo, "A through investigation of progressive breakdown in ultrathin, oxide. Physical understanding and application for industrial reliability assessment," in *Proc. Int. Reliab. Phys. Symp.*, 2002, pp. 45–54.