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Dielectric Degradation of $Cu/SiO_2/Si$ Structure during Thermal Annealing

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ABSTRACT

The impact of Cu on the dielectric SiO_2 layer was studied using a $Cu/SiO_2/Si$ metal oxide semiconductor capacitor and rapid thermal annealing (RTA) treatment. With the RTA treatment, no chemical reaction was observed up to 900°C; however, dielectric degradation occurred following RTA at 300°C for 60 s and became worse with the increase of annealing temperature. The interface-trap density at the SiO_2/Si interface also increased from 5×10^{10} to 5×10^{13} eV^{-1} cm^{-2} after 800°C RTA treatment. The RTA anneal introduced a large number of positive Cu ions into the dielectric SiO_2 layer. Under bias-temperature stress, Cu ions drift quickly in the SiO_2 layer and may drift across the SiO_2/Si interface and enter the Si substrate. With the use of 1200 Å thick TiN and TiW barrier layers, respectively, the dielectric strength of the Cu/(barrier)/SiO_2/Si structures was able to remain stable up to 500 and 600°C.

Introduction

Copper has been extensively studied as a potential metallization material in ultralarge scale integrated (ULSI) circuits because of its low resistivity (1.67 μΩ-cm for bulk) and high electromigration resistance. However, copper forms Cu-Si compounds at a relatively low temperature[1-4] and introduces deep level traps in Si.[5] In order to use Cu as a future ULSI interconnect metal, the thermal stability of Cu with the underlying materials and devices must be carefully evaluated.

In modern multilevel metallization structures, SiO_2 layers are usually employed as the interlayer dielectric; the dielectric layers not only isolate the interconnect lines of different levels, but also separate the active devices from the contacted metals. Therefore, no interaction between Cu and the enclosed dielectric layer is allowed during the post Cu-metallization thermal process. The penetration of Cu through the dielectric layer will not only degrade the dielectric layer, but will also introduce deep level traps in the Si substrate that harm device performance. Therefore, the influence of Cu contamination on the dielectric properties of SiO_2 becomes a major issue in the multilevel interconnect structure if Cu is to be used as the interconnect metal. It has been reported that Cu migrates into SiO_2 at temperatures as low as 250°C in the presence of an electric bias.[6] However, the influence of Cu on the degradation behavior of SiO_2 remains unclear.

In this study, we investigated the influence of Cu on the dielectric properties of SiO_2 layers as well as the reaction between Cu and SiO_2. The metal oxide semiconductor (MOS) capacitors of a $Cu/SiO_2/Si$ structure were fabricated and studied with regard to the electrical and metallurgical aspects. The dielectric degradation was characterized by capacitance-voltage (C-V) measurement and the dielectric strength was determined from the breakdown voltage measurement. The role of Cu in SiO_2 was investigated by interface trap density (D_{it}) and mobile ion meas-

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urements. To prevent Cu from penetrating into the oxide layer, barrier layers of TiN and TiW were applied, respectively, and their diffusion barrier effects were evaluated.

Experimental

The $Cu/SiO_2/Si$ MOS capacitors were fabricated on (100)-oriented phosphorus-doped n-type Si wafers with a resistivity of 4 to 7 Ω-cm. After standard cleaning, a 6000 Å field oxide was thermally grown in a pyrogenic steam atmosphere at 1050°C. Square active regions of various sizes were defined by a conventional photolithographic technique. A 250 Å thick SiO_2 layer was either deposited by the chemical vapor deposition (CVD) method or thermally grown in a dry oxygen atmosphere at 950°C. A Cu film of 2000 Å thickness was subsequently sputter deposited using a pure Cu target (99.99%) in Ar at a pressure of 5×10^{-3} Torr and with a deposition rate of 0.1 Å/s. The Cu layer was then patterned to the alignment of the square active area.

The samples were then treated with rapid thermal annealing (RTA) at various temperatures with a temperature ramping of 100°C/s in N_2 ambient. The back sides of the samples were metallized by Al deposition for electrical measurement. The dielectric breakdown behavior was measured by applying a staircase voltage ramp using an HP4145B semiconductor parameter analyzer with the MOS capacitor biased at accumulation polarity. The breakdown voltage was defined as the voltage at which an abrupt increase of current occurred. The area of the tested capacitors was 200×200 μm^2 and at least 15 capacitors were measured to construct the breakdown statistics. The midgap interface state density (D_{it}) was derived from the high frequency C-V (HFCV) and quasi-static C-V (QSCV) measurements on the 500×500 μm^2 capacitors using the Keithley measuring system.[7] The HFCV measurement was also used to determine the flatband voltage (V_{FB}) as well as to double check the oxide thickness and substrate doping concentration. For mobile ion measurement, the Cu layer was removed from the $Cu/SiO_2/Si$ MOS capacitors after RTA treatment and replaced by an Al electrode. Bias temperature stress was performed on the $Al/SiO_2/Si$ MOS capacitors at a temperature of 150°C and with a bias of 1 MV/cm electric field for a desired length of time. After the stress, the C-V characteristics were measured to determine the flatband voltage shift (ΔV_{FB}).

The effect of TiN and TiW layers as diffusion barriers in the structure of $Cu/(barrier)/SiO_2/Si$ was investigated. On one group of the samples, a TiN layer of 1200 Å thickness was deposited on SiO_2 by reactive sputtering using a Ti target (99.99%) in the N_2 + Ar mixture (N_2:Ar = 1:5) at a total pressure of 5×10^{-3} Torr and with a deposition rate of 1.65 Å/s. On the other group of the samples, a TiW layer of 1200 Å thickness was sputter deposited on SiO_2 using a TiW target [Ti 30 atom percent (a/o)] in Ar ambient at a pressure of 5×10^{-3} Torr and with a deposition rate of 1.72 Å/s. After the deposition of the barrier layers, the samples were exposed to air before Cu deposition. Unpatterned samples of $Cu/SiO_2/Si$ and $Cu/(barrier)/SiO_2/Si$ structures were also prepared for material analysis following the same processing sequence and annealing treatment. Glancing angle x-ray diffraction was used for phase identification. The layered structures and examined by cross-sectional transmission electron microscopy (TEM).

Results and Discussion

Metallurgical reaction.—The $Cu/SiO_2/Si$ structure was found to be metallurgically stable with respect to RTA treatment. Sheet resistance (R_s) of the structure showed no obvious changes up to 900°C, and no compound was detected by the glancing angle x-ray diffraction. Figure 1 shows the cross-sectional view of TEM micrograph for the 900°C annealed $Cu/SiO_2/Si$ sample; it revealed that the layer structure remained intact. To characterize the annealed SiO_2 dielectric layer, the Cu layer of the annealed sample was stripped off in HCl + H_2O_2 + H_2O (1:1:6) solution, and the SiO_2 layer was inspected by SEM and measured by an ellipsometer to determine the film thickness and index of refraction (n_i). No obvious changes in surface morphology, film thickness as well as index of refraction were found for the SiO_2 layer after the $Cu/SiO_2/Si$ sample was RTA annealed at 900°C.

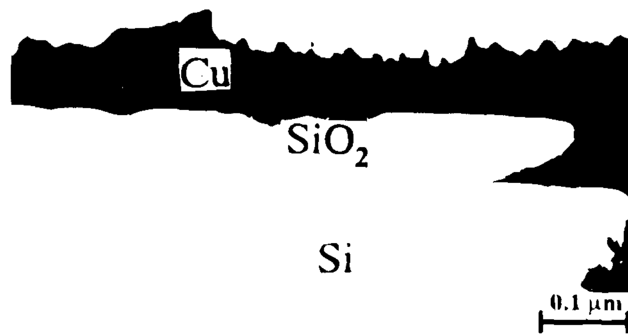

Fig. 1. Cross-sectional view of TEM micrograph for the RTA (in N_2 for 30 s) annealed thermal oxide Cu/SiO_2 (780 Å)/Si MOS capacitor at a temperature of 900°C.

Dielectric strength-E_{bd} degradation.—Electrical properties are usually more sensitive to the reaction which occurred within the structure than are metallurgical properties. The dielectric properties of SiO_2 layers were found to be severely degraded after RTA. The statistical distribution of E_{bd} for the 250 Å thick thermally grown and CVD-deposited SiO_2 layers, respectively, in the $Cu/SiO_2/Si$ structure annealed at various temperatures is illustrated in Fig. 2 and 3. The dielectric strength of the thermally grown SiO_2 is higher than that of the CVD SiO_2; however, both oxide layers degraded when annealed at 300°C and the degradation became worse with the increase of annealing temperature. In comparison with the oxide degradation induced by other metal contamination,[9,12,13]

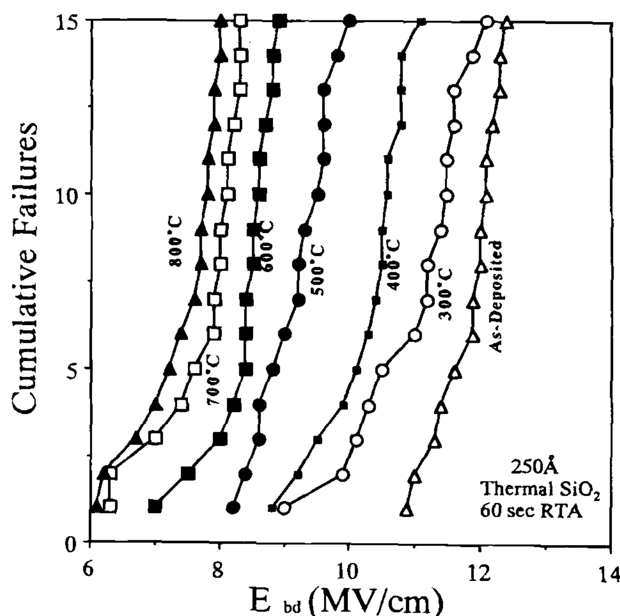

Fig. 2. Statistical distribution of E_{bd} for the $Cu/SiO_2/Si$ samples for 60 s RTA in N_2 ambient; the oxide layer was thermally grown and was 250 Å thick.

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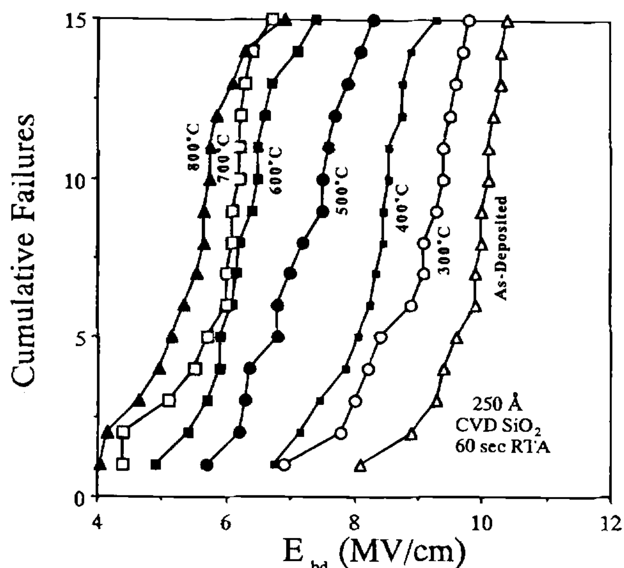

Fig. 3. Statistical distribution of E_{bd} for the $Cu/SiO_2/Si$ samples for 60 s RTA in N_2 ambient; the oxide layer was deposited by a CVD method and was 250 Å thick.

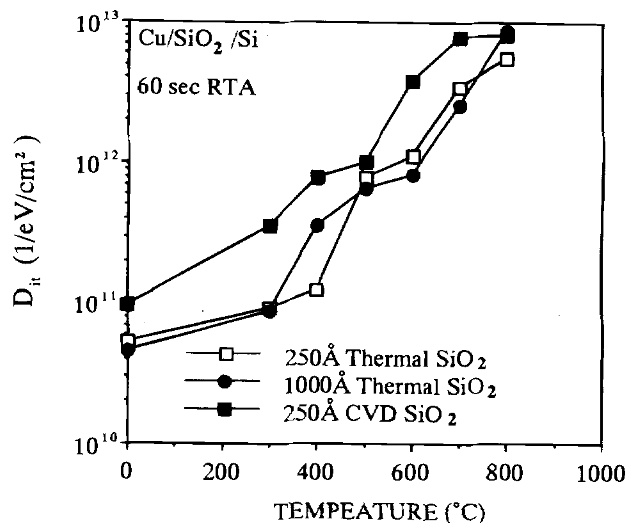

Fig. 5. Interface trap density of the $Cu/SiO_2/Si$ MOS capacitors after RTA annealing at various temperatures in N_2 ambient for 60 s.

Cu degrades the SiO_2 layer at a much lower temperature. Figure 4 shows the flatband voltage of the thermal oxide $Cu/SiO_2/Si$ MOS capacitors *vs.* annealing temperature of a 60 s RTA in N_2 ambient. It can be seen that the flatband voltage shifts toward the negative voltage with the increase of annealing temperature from −1 V (as grown) to −4 V (800°C.). The large flatband voltage shift implies that a large amount of positive Cu ions were present in the SiO_2 layer. Copper dissolution in SiO_2 is presumably responsible for the dielectric degradation since there is no evidence of metallurgical reaction between Cu and SiO_2.

Interface trap density-D_{it} degradation.—Annealing the $Cu/SiO_2/Si$ capacitors also resulted in the increase of the interface trap density (D_{it}) at the SiO_2/Si interface, as shown in Fig. 5. Generally, CVD SiO_2 produces a slightly higher D_{it} than that of the thermally grown SiO_2; however, dramatic D_{it} increase was observed on all the three $Cu/SiO_2/Si$ capacitors following RTA annealing. With RTA annealing at 800°C, D_{it} increases by two orders of magnitude (from 10^{11} to 10^{13} 1/eV/cm^2). The increase of D_{it} by Cu contamination is much higher than that induced by other metal contamination.[9] In addition, it can be seen that D_{it} of the thin oxide MOS capacitor nearly equals that of the thick oxide MOS capacitor. Clearly, from the above observation, the degradation of the dielectric strength and the increase of interface trap density at the SiO_2/Si interface can be attributed to the presence and diffusion of Cu ions in the SiO_2 layer resulting from RTA treatment on the $Cu/SiO_2/Si$ capacitors. Further study on the movement of Cu ions in the SiO_2 layer was conducted using the technique of bias-temperature stress. The Cu electrodes were removed from the RTA annealed $Cu/SiO_2/Si$ MOS capacitors followed by Al metallization to make them into the $Al/SiO_2/Si$ MOS capacitors.

Mobile Cu ion-BTS measurement.—The bias-temperature stress (BTS) was applied to the new Al-gated capacitors by setting the electrically biased samples on a thermal chuck heated to a temperature of 150°C for a given length of time. After the stress, the samples was cooled down to room temperature, and the *C-V* characteristic was measured to determine the flatband voltage. For the annealed

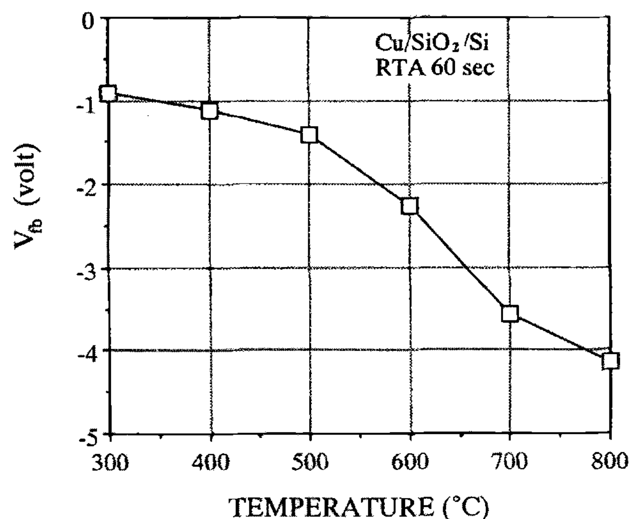

Fig. 4. Flatband voltage (V_{FB}) of the thermal oxide $Cu/SiO_2/Si$ MOS capacitor *vs.* annealing temperature of a 60 s RTA in N_2 ambient.

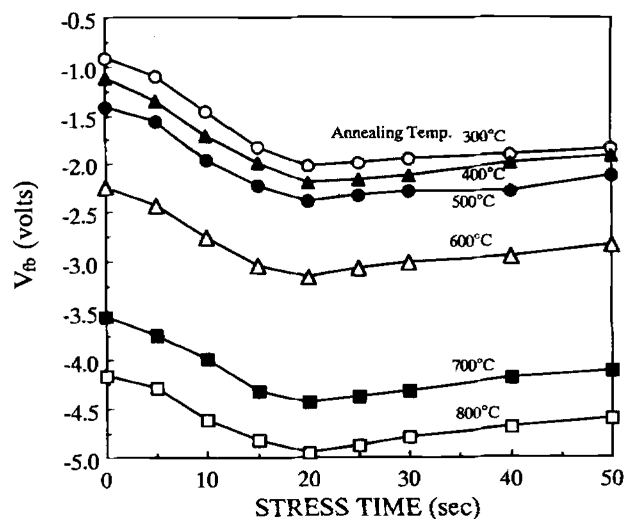

Fig. 6. Flatband voltage (V_{FB}) *vs.* bias-temperature stress time for $Cu/SiO_2/Si$ capacitors annealed at various temperatures; the bias-temperature stress was conducted at a temperature of 150°C with an applied electrical bias of 1 MV/cm.

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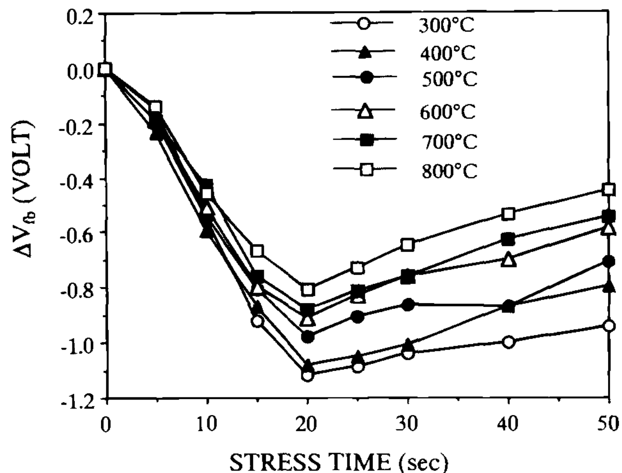

Fig. 7. Flatband voltage shift (ΔV_{FB}) vs. bias-temperature stress time for $Cu/SiO_2/Si$ capacitors annealed at various temperatures; the bias-temperature stress was conducted at 150°C with an applied electrical bias of 1 MV/cm.

Cu/SiO_2 (1000 Å)/Si capacitors, the flatband voltage as a function of BTS time with an electrical bias of 1 MV/cm is illustrated in Fig. 6. The flatband voltage shifted toward more negative voltage during the first 20 s and slightly shifted back afterward. Since the BTS was applied with positive voltage on the gate electrode, the negative V_{FB} shift implies that a large amount of Cu ions drifted quickly toward the SiO_2/Si interface, even at a low temperature of 150°C. To ensure that the samples were not contaminated by other mobile ions such as Na^+ ions, control samples were also fabricated following the same processing sequence of the $Cu/SiO_2/Si$ capacitors except that Al gate instead of Cu metallization was applied for the fabrication of MOS capacitors. For the control samples, no obvious flatband voltage shift with respect to BTS was observed, indicating that the sample process was free from Na^+ ion contamination. Figure 7 shows the flatband voltage shift ΔV_{FB} as a function of bias-temperature stress time, derived from the data shown in Fig. 6, for the samples annealed at various temperatures. It reveals an interesting feature that the ΔV_{FB} of higher temperature annealed samples are smaller than those of lower temperature annealed ones. Since the samples annealed at a higher temperature resulted in a larger amount of Cu ions in the SiO_2 layer, as indicated by a larger shift of V_{FB} shown in Fig. 4, they should also have a larger flatband voltage shift when these Cu ions drifted toward the SiO_2/Si interface. From the contrary results shown in Fig. 7, together with the observation that ΔV_{FB} started to decrease after 20 s BTS, it is reasonable to presume that a certain amount of Cu ions near the SiO_2/Si interface drifted into the Si substrate under prolonged BTS, especially for the samples annealed at higher temperatures.

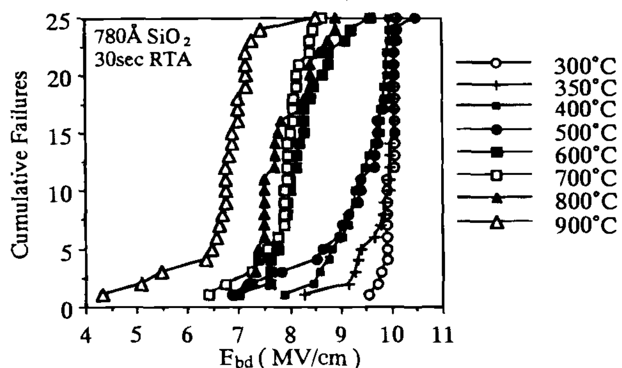

Fig. 8. Statistical failure cumulation of E_{bd} for the thermal oxide Cu/SiO_2 (780 Å)/Si MOS capacitor after 30 s RTA at various temperatures in N_2 ambient.

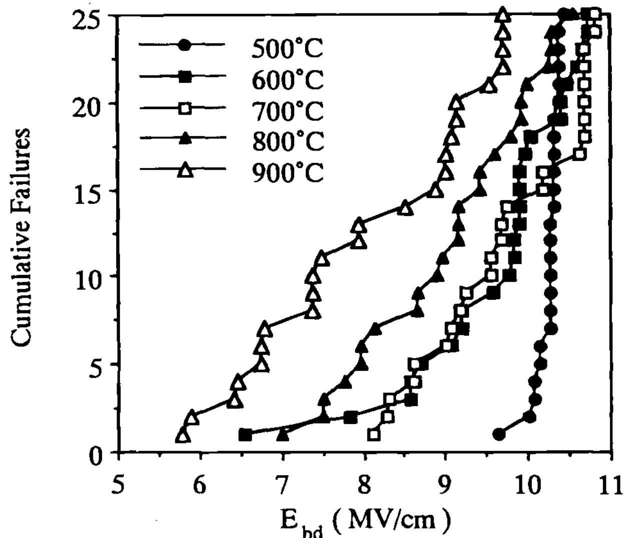

Fig. 9. Statistical failure cumulation of E_{bd} for the Cu/TiN (1200 Å)/SiO_2 (786 Å)/Si structure after 30 s RTA at various temperatures in N_2 ambient.

Dielectric degradation of the SiO_2 layer in the metal/SiO_2/Si structure after high temperature treatment mostly results from the chemical reaction between metal and SiO_2 as well as metal dissolution in the SiO_2 layer.[8-13] For example, Ti was reported to degrade the SiO_2 by the formation of Ti-rich silicide at the SiO_2/Si interface at a temperature as low as 400°C. [8] In the Pt/SiO_2/Si system, dielectric degradation caused by Pt dissolution was reported.[9] In Cu-related dielectric degradation, it was reported that the SiO_2 layer thermally grown from the Cu implanted Si substrate degraded due to the Cu precipitates at the SiO_2/Si interface.[14] It was also reported that contamination by scraping a piece of Cu wire over the back side of the Si wafer caused degradation to the thermally grown SiO_2 layer because of the formation of Cu-rich precipitates at

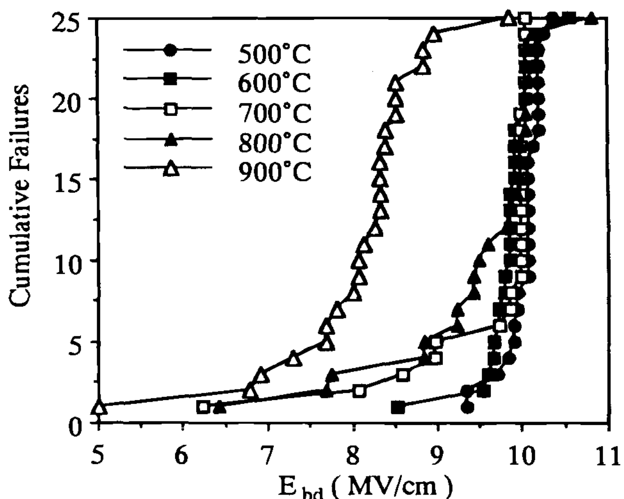

Fig. 10. Statistical failure cumulation of E_{bd} for the Cu/TiW (1200 Å)/SiO_2 (786 Å)/Si structure after 30 s RTA at various temperatures in N_2 ambient.

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the SiO_2/Si interface.[15] Both studies concluded that the dielectric degradation resulted from the SiO_2 thickness reduction caused by the Cu silicide formation at the SiO_2/Si interface. Since Cu diffuses quickly in Si and forms Cu-Si compounds at a low temperature of 200°C, the Cu, whether implanted in Si or scraped over the back side of an Si wafer, can easily diffuse and accumulate at the SiO_2/Si interface to form Cu precipitates during a subsequent thermal process. It was also observed that Cu_4Si phase appeared in the C/Cu/SiO_2/Si structure after annealing at 700°C for 72 h in an N_2 + H_2 ambient.[16] Recent study shows that Cu in the Cu/SiO_2/Si structure can diffuse into the SiO_2 layer to a concentration of 10^{17} cm^{-3} after thermal annealing at 300°C for 30 min without bias.[6] For the Cu/SiO_2/Si structure studied in this work, we observe no chemical reaction between Cu and SiO_2 up to 900°C of 30 s RTA. However, the mobile ion and D_{it} measurements indicated that a large number of Cu ions diffused into the SiO_2 layer. Furthermore, Cu ions drift very quickly in the SiO_2 layer and into the Si substrate under the bias-temperature stress at a temperature of 150°C. In addition to the presence of mobile Cu ions in the SiO_2 layer and the increase of interface trap density, dielectric properties of the SiO_2 layer were severely degraded when the MOS structure was RTA annealed at 300°. The role of Cu in the Cu/SiO_2/Si MOS structure is now clear. Copper is metallurgically stable with the enclosed SiO_2 dielectric, but it is an uncontrollable diffusion species penetrating almost freely in the SiO_2/Si system; the electric bias further accelerates the speed of penetration. Thus, the Cu metallization system must incorporate with an appropriate diffusion barrier, so that Cu could be possibly useful in ULSI applications.

Diffusion barrier effects.—We investigate the Cu/(barrier)/SiO_2/Si system with respect to the diffusion barrier effect of TiN and TiW layers, both of which are 1200 Å thick in this study. Without using the barrier layer, the breakdown field (E_{bd}) statistic distribution of the Cu/SiO_2 (780 Å)/Si samples annealed with 30 s RTA at various temperatures is illustrated in Fig. 8. It can be seen that dielectric degradation started to occur following the 30 s RTA at 350°C and became worse with the increase of annealing temperature. With the barrier layer, the E_{bd} statistic distributions of the Cu/TiN/SiO_2/Si and Cu/TiW/SiO_2/Si samples annealed at various temperatures are illustrated in Fig. 9 and 10, respectively. For the Cu/TiN/SiO_2/Si samples, obvious dielectric degradation was observed after RTA annealing at temperatures above 600°C. The failure distribution also indicates that the degradation which occurred was fairly nonuniform. For the Cu/TiW/SiO_2/Si samples, annealing at temperatures below 600°C did not cause obvious dielectric degradation, but some of the 25 randomly chosen samples started to show degradation after annealing at 700°C. By comparing the data shown in Fig. 9 and 10, we clearly observe that TiW serves as a better diffusion barrier than does TiN. This is consistent with the results from the studies done on the TiN and TiW diffusion barriers employed in the Cu/(barrier)/$CoSi_2$/p^+n junction diodes.[17,18]

Conclusion

Copper was found to be metallurgically stable with the dielectric SiO_2. However, Cu from the Cu/SiO_2/Si structure degrades the dielectric properties of SiO_2 at a temperature of 300°C; the higher the temperature, the more positive Cu ions migrate into the SiO_2 layer, thus leading to worse degradation of the MOS structure. In addition, Cu induces a large midgap interface trap density at the SiO_2/Si interface following RTA annealing. Under bias-temperature stress, Cu ions drift very fast in the SiO_2 layer and may drift across the SiO_2/Si interface and enter into Si substrate. Both TiN and TiW were shown to be effective diffusion barriers in the Cu/(barrier)/SiO_2/Si MOS structure. Without the diffusion barrier, the SiO_2 dielectric started to degrade following RTA at 300°C. With the use of 1200 Å TiN and TiW barrier layers, respectively, the dielectric strength of the MOS structures remained stable up to 500 and 600°C.

Acknowledgments

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