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A DESIGN STRATEGY FOR SHORT GATE LENGTH SOI MESFETs

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Abstract—A design strategy for short gate length, self-aligned Si-SOI MESFETs is proposed, in which the design considerations for the important device parameters of the SOI MESFET are studied by using a 2D numerical simulator. It is shown that the sub-threshold I_{ds}–V_{gs} characteristics can be used to determine the thickness of silicon film for a given channel doping level under a specified threshold voltage. Moreover, the 2D effect can be suppressed by reducing the thickness of buried oxide to improve the bottom-gate controllability over the channel charges. Moreover, it is shown the backgate bias is also an important controllable parameter for modulating the characteristics of the SOI MESFET in both sub-threshold and saturation regions. An example for designing a very short gate length (0.1 μm) SOI MESFET has been carried out to verify this strategy. It is shown that the proposed strategy does provide an effective procedure for designing an Si-SOI MESFET with high performance.

1. INTRODUCTION

The trend of modern VLSI technology demands miniaturized devices with high performance and high reliability. However, the further scaling of existing bulk MOSFET below 0.25 μm becomes difficult because it involves the technologies of high-quality thin gate oxide, high-density device isolation, and shallow junctions. Recently, MOS devices fabricated on SOI films have been readily investigated owing to efficient device isolation, elimination of latch-up path, and improved radiation hardness. The Si-MESFET device fabricated on thin SOI film will be of interest because it gains the benefit of SOI structure while bypassing the gate oxide related reliability issues of MOSFETs.

Si-MESFET devices have been fabricated on silicon-on-sapphire (SOS) film[1] and p–n junction Si-substrate[2–4]. MESFETs fabricated on SOS film have the advantages of reduced parasitic source (drain) capacitances, perfect device isolation, and better radiation hardness. However, the lattice mismatch and the difference in thermal expansion coefficient between sapphire and silicon produce a large built-in stress, and further cause serious defects in the grown film, resulting in the reduction of carrier mobility. Besides, owing to the lattice mismatch, the mobility degrades very rapidly if the film thickness is reduced, and this prevents the device from further scaling in depth direction. Moreover, silicon film grown on expensive sapphire is not cost effective for commercial applications. On the other hand, a MESFET fabricated on a junction substrate uses the LOCOS isolation technique, resulting in a serious bird's beak. Moreover, the planarization process needed becomes complicated, and channel-stop implantation is needed to eliminate the leakage current between adjacent devices. From the viewpoint of device physics, the source (drain) capacitance will hamper the device speed, and the device performance becomes very sensitive to channel thickness and doping profile. These factors will increase process complexity and make device scaling much more difficult. Recently, the characteristics of short gate length MESFETs fabricated on SOI film have been analysed, and an analytic threshold-voltage model has been developed to describe the short gate length effects[5]. It has been shown that the Si-SOI MESFET presents little short gate length effect and is the most promising device for tomorrow's ULSI technology. The possible challenges of Si-SOI MESFET devices are the feasibility for fabricating complementary-type circuits and gate leakage. The former can be overcome by impurity implantation to adjust the barrier height for the p-MESFET, and the latter can be avoided by appropriately choosing the doping level of silicon film.

In this paper, a 2D device simulator[6] is used to analyse the relationships between the structure parameters and the device characteristics. In Section 2, the basic characteristics and design considerations for a short gate length SOI MESFET will be discussed. A design strategy for short gate length SOI MESFETs is proposed in a step-by-step manner. Following the proposed design strategy, a design example is given in Section 3. It is shown that the designed SOI MESFET with very short gate length (0.1 μm) exhibits excellent performance and little

short gate length effect under an appropriate determination of structure parameters and bias conditions. Finally, a concluding remark is given in Section 4.

2. DESIGN CONSIDERATIONS AND STRATEGY

2.1. *Design considerations of Si-SOI MESFETs*

The basic structure of a Si-SOI MESFET is shown in the insert of Fig. 1. In this paper, we focus on the self-aligned MESFET structure in which a very small spacing between the gate and the source (drain) could be obtained, and no direct short between the gate and the source (drain) occurs. The self-aligned structure not only precisely defines the gate length but also minimizes the parasitic source (drain) series resistance. A 2D numerical simulator described in [5] and [6] is used to analyse the electrical behaviors of short gate length Si-SOI MESFETs for a wide range of structure parameters and applied biases. In this device simulator, the 2D Poisson's equation is solved by a new discretized Green's function method and a surface mapping technique is developed to treat arbitrary surface boundary conditions. The full set of semiconductor equations including Poisson's equation and current continuity equations can be solved self-consistently by a new SLOR non-linear iteration technique in which the matrix element can be updated for the potential change due to the linear response to the change of charge density. This simulator has been successfully applied to analyse GaAs MESFETs[7,8] and SOI MOSFETs[9]. Excellent computational efficiency and accurate physical models prove that this simulator is efficient for semiconductor device simulation.

It has been investigated[5] that the most important structure parameters of a Si-SOI MESFET are the doping level N_D (cm^{-3}), and the thickness of silicon film t_{Si} (nm), as shown in Figs 1 and 2, respectively. It is shown in Fig. 1 that the threshold voltage of a SOI MESFET with lower doping level is higher because the channel is inclined to be pinched-off while all the devices show a similar short gate length effect. On the other hand, as shown in Fig. 2, the SOI MESFET with thinner silicon film has a smaller threshold-voltage shift and thus exhibits smaller short gate length effect because the channel charges of this device are mainly controlled by the Schottky gate and the backgate, and the source (drain) to channel high–low junction has a reduced influence on channel charges. Therefore, the short gate length SOI MESFET with appropriate thin silicon film can offer

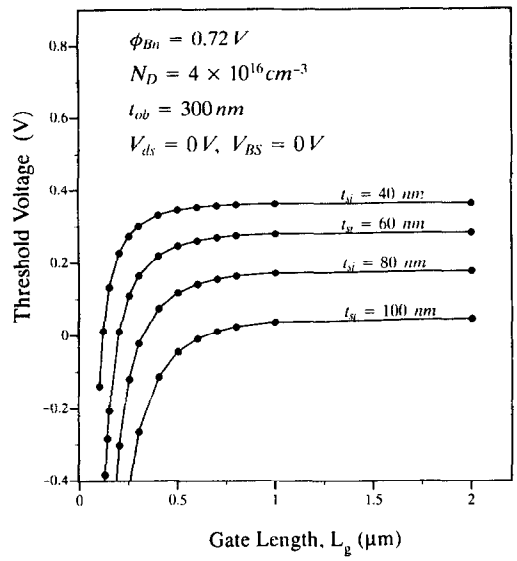

Fig. 2. Threshold voltage vs gate length with silicon film thickness as a parameter.

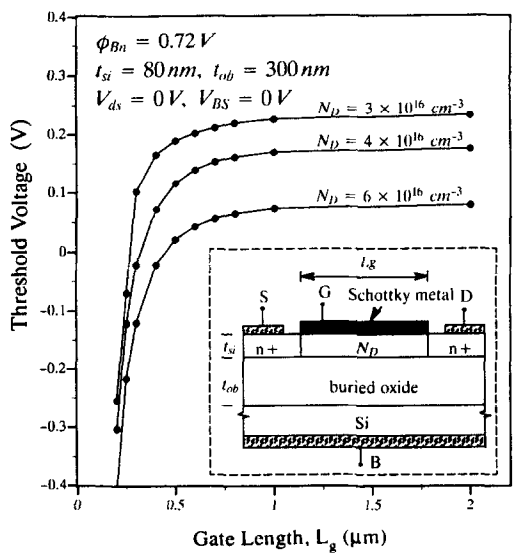

Fig. 1. Threshold voltage vs gate length with channel doping as a parameter. The insert is the basic structure of a Si-SOI MESFET.

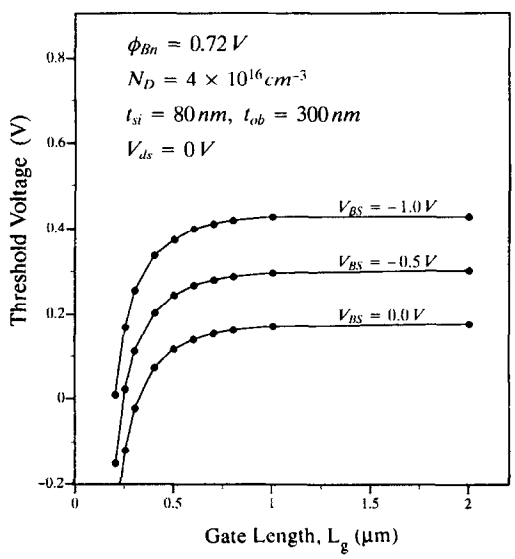

Fig. 3. Threshold voltage vs gate length for various backgate biases.

device behaviors quite similar to those of a long-channel device. The effect of backgate bias V_{BS} (V) on threshold voltage is shown in Fig. 3, in which backgate bias introduces an almost constant shift in the threshold voltage vs gate length L_g (μm) curve, suggesting that the backgate bias can help adjust the threshold voltage in addition to the structure parameters. Thus, the application of backgate bias makes the design of SOI MESFET devices more flexible.

It is known that the MESFET does not suffer from punch-through problems because the channel and the source (drain) are of the same conductivity type, and the built-in voltage across the source (drain) to channel high–low junction is only about 0.2 V (much smaller than the built-in voltage across the channel to source/drain p–n junction in a MOSFET). However, the drain-induced barrier lowering effect still exists. As the drain bias increases, the drain junction in fact draws more charges. The channel barrier of a short gate length SOI MESFET is substantially lowered when the drain bias is applied, and the position of potential minimum will move toward the source side.

2.2. Design strategy

A design strategy is proposed, based on the relationships between the basic characteristics and the structure parameters of the SOI MESFET discussed above, in a step-by-step manner to decouple the complex relationships among the parameters, as shown in Fig. 4. This strategy can be briefly described in a qualitative sense as follows:

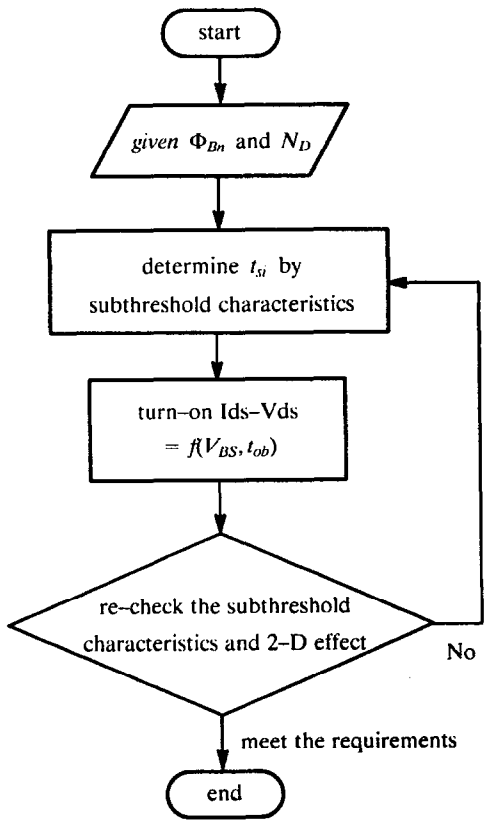

Fig. 4. Flowchart showing the design strategy for a SOI MESFET.

(i) For the given barrier metal and doping level of silicon film, the barrier height ϕ_{Bn} (V) and the built-in voltage of a metal–semiconductor contact could be known. The thickness of silicon film can be precisely controlled by oxygen implantation using modern SIMOX/SOI technology. The active channel can be assumed to be uniformly doped because the silicon film is very thin. This assumption eliminates several implantation parameters and makes the analysis easy; besides, the effect of junction curvature of the source (drain) island can be ignored because t_{Si} is usually smaller than the junction depth. Therefore, the source (drain) junction can be modelled by a constant built-in voltage of source (drain) to channel high–low junction along the depth direction.

(ii) The choice of t_{Si} is not fully free. For the desired L_g and ϕ_{Bn}, the acceptable range of silicon film thickness (ART) can be determined by checking the sub-threshold characteristics.The lower bound of ART is limited by ϕ_{Bn} to avoid forward conduction of the Schottky gate, while the upper bound of ART is determined by the specification of sub-threshold swing. The sub-threshold swing, indicating the gate controllability, should be as small as possible. The thickness of silicon film is then chosen within ART according to the specification of threshold voltage.

(iii) The turn-on I_{ds}–V_{ds} characteristics could be modulated by changing t_{ob} or applying V_{BS}. The 2D effect in the saturation region caused by the drain could be suppressed by reducing t_{ob} to increase the bottom-gate controllability over the channel charges. However, in some applications, the saturation drain current level is an important performance parameter which can be modulated by V_{BS}. Note that the application of V_{BS} will change sub-threshold characteristics, such as sub-threshold swing and threshold voltage, while the variation of t_{ob} has less influence on the characteristics in the sub-threshold and linear regions.

(iv) Once the specified turn-on saturation drain current level has been obtained in part (iii), the sub-threshold characteristics should be re-examined for checking the sub-threshold swing and the threshold voltage. To offer good gate controllability and a small 2D effect, parts (ii) and (iii) should be iterated to meet the specifications of sub-threshold swing, threshold voltage, and saturation drain current level.

The strategy described above is a theoretical principle, while the real device experiences reliability problems. However, the SOI MESFET is inherently immune to soft error and gate oxide related reliability issues. This is the major advantage of the SOI MESFET over the bulk MOSFET devices. The only oxide-related reliability problem for a SOI MESFET comes from the buried oxide substrate. However, the buried oxide for the SOI MESFET is thicker and the channel conducts in the undepleted region of the Si film, resulting in a smaller mobility degradation due to surface scattering.

3. A DESIGN EXAMPLE

It has been mentioned in the previous section that for a Si-SOI MESFET, the most important structure parameters are N_D and t_{Si}, and a certain interrelation exists between these two parameters. For the given ϕ_{Bn} and N_D, the choice of t_{Si} is not fully free, and the acceptable range of silicon film thickness (ART) will be limited. An example of a very short gate length (0.1 μm) SOI MESFET is shown in Fig. 5. It is clearly shown that the sub-threshold characteristics of a SOI MESFET are strongly dependent on t_{Si}. Therefore, the sub-threshold I_{ds}–V_{gs} characteristics can be used to examine the rule of ART. In this example, $\phi_{Bn} = 0.64$ V, $N_D = 4.0 \times 10^{17}$ cm^{-3}, and t_{ob} is about 300 nm. For the SOI MESFET device with $L_g = 0.1$ μm, ART ranges from about 25 to 40 nm. The lower bound of ART is limited by the threshold voltage, which should be lower than the built-in voltage of the Schottky gate to avoid the forward conduction of metal–semiconductor contact. For the device with silicon film thinner than the lower bound, the active channel is always depleted by the barrier height of the Schottky gate. In other words, the threshold voltage of this device is higher than the built-in voltage of the Schottky gate, and the device will never turn on in normal operation conditions. On the other hand, as the silicon film becomes thicker, the sub-threshold I_{ds}–V_{gs} curve shifts left along with the slope changes, resulting in lower threshold voltage and poor sub-threshold swing. For silicon film thicker than a certain value, the SOI MESFET device becomes a depletion mode device, i.e., a normally-on device. Therefore, the upper bound of ART is determined by the specification of sub-threshold swing. The device with silicon film thicker than the upper bound exhibits very poor sub-threshold characteristics and suffers serious leakage, which cannot be suppressed even when the negative gate bias is applied.

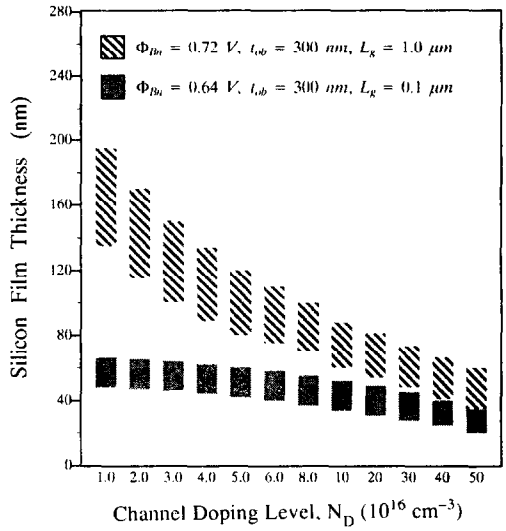

Fig. 6. Silicon film thickness vs doping level for $\phi_{Bn} = 0.64$ V and $L_g = 0.1$ μm, and $\phi_{Bn} = 0.72$ V and $L_g = 1.0$ μm. The thickness of the buried oxide is 300 nm.

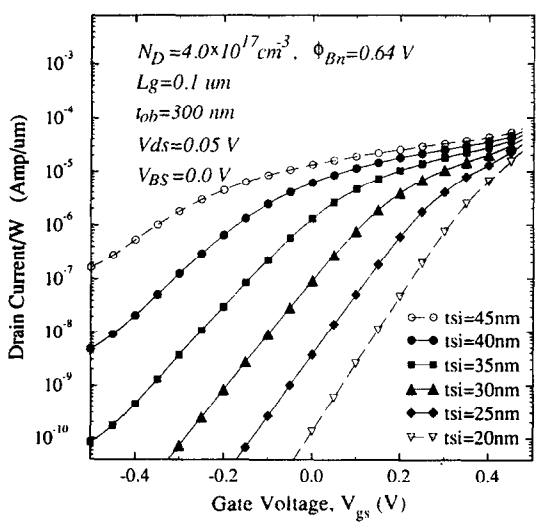

Fig. 5. Sub-threshold characteristics of a 0.1 μm Si-SOI MESFET with $\phi_{Bn} = 0.64$ V and $N_D = 4.0 \times 10^{17}$ cm^{-3} for different silicon film thicknesses.

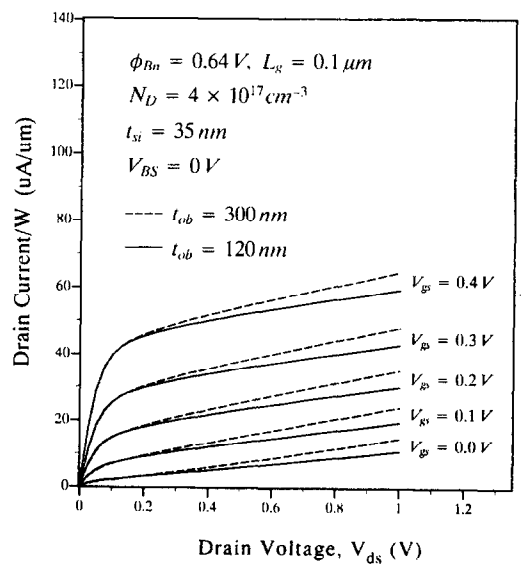

Fig. 7. Turn-on I_{ds}–V_{ds} characteristics of a 0.1 μm Si-SOI MESFET with $\phi_{Bn} = 0.64$ V, $N_D = 4.0 \times 10^{17}$ cm^{-3}, and $t_{Si} = 35$ nm, for $t_{ob} = 300$ and 120 nm.

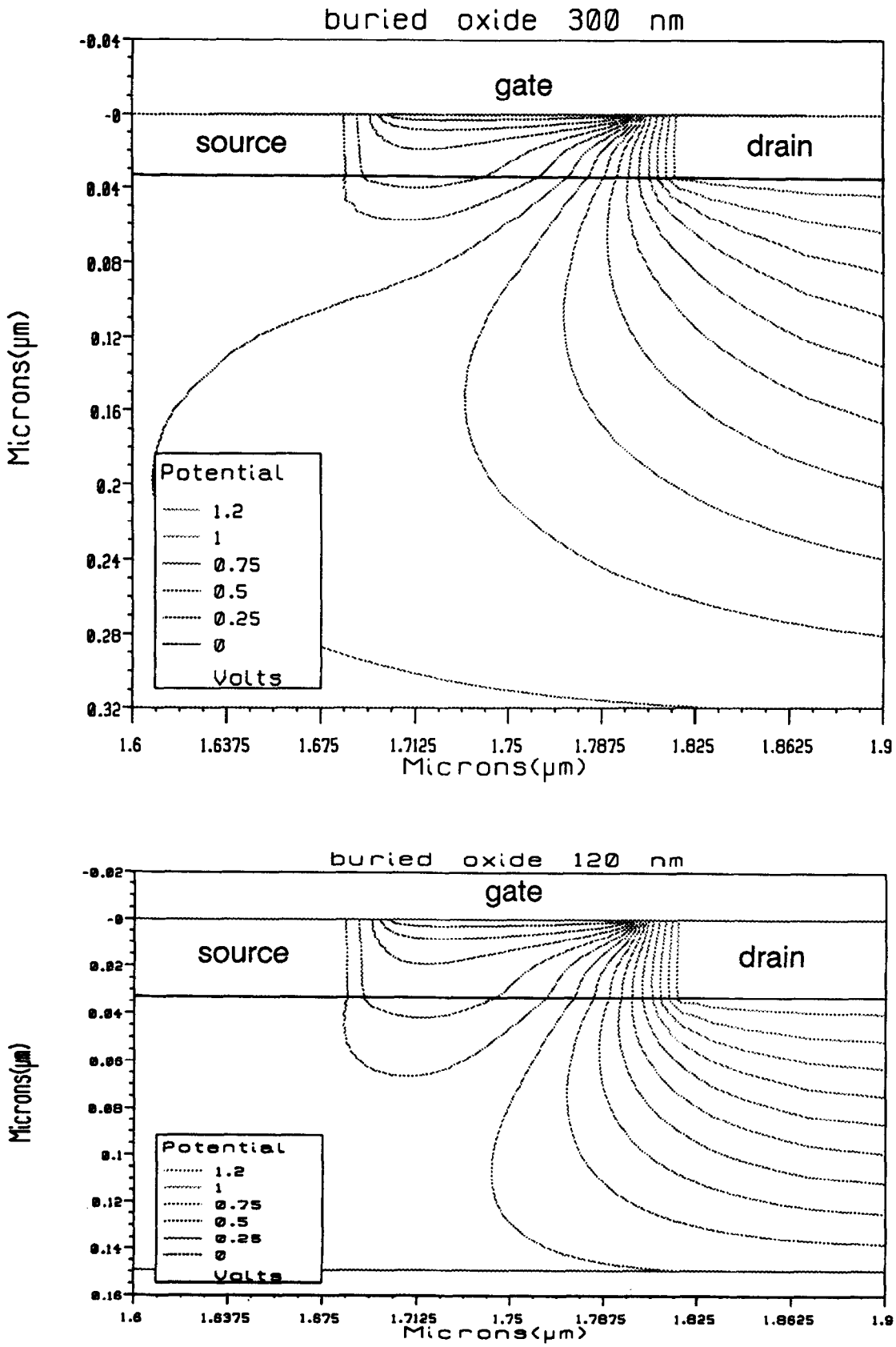

Fig. 8. 2D equipotential contours of a 0.1 μm Si-SOI MESFET operated in the saturation region with $\phi_{Bn} = 0.64$ V, $N_D = 4.0 \times 10^{17}$ cm^{-3}, and $t_{Si} = 35$ nm, for $t_{ob} = 300$ and 120 nm.

It should be noted that ART is a function of N_D. For different N_D, the corresponding pinch-off voltage is different, and then ART varies. Figure 6 shows ART as a function of N_D. The shadow region in Fig. 6 represents ART with $\phi_{Bn} = 0.64$ V, $L_g = 0.1$ μm and $t_{ob} = 300$ nm. The total range of ART is almost constant for different N_D, but shifts to the thicker level for lightly doped silicon film. However, as N_D is reduced to even less than 1.0×10^{16} cm^{-3}, ART tends to saturate. It is due to the fact that the Schottky gate with a fixed barrier height could not control charges too far away from the gate, and the device with too thick silicon film cannot be accepted. In addition to N_D, ART is also a function of ϕ_{Bn} and L_g. The twill region in Fig. 6 is ART with $\phi_{Bn} = 0.72$ V and $L_g = 1.0$ μm for comparison. In a short gate length device, the source and drain junctions take over the charges in their neighborhood originally controlled by the gate. So the required t_{Si} should be thinner to compensate for the influences of source and drain junctions. For a larger gate length device, the influences of source and drain junctions are much reduced. Then, ART for the 1.0 μm SOI MESFET shifts to a thicker level, with the total range wider than that of 0.1 μm device. The results shown in Fig. 6 give a first and simple guideline for determining t_{Si} and N_D, based on the sub-threshold characteristics of a SOI MESFET. In general, the short gate length device needs a higher doping level, and thinner silicon film can be easily obtained by modern SOI technology to suppress the short gate length effect. In addition to the sub-threshold characteristics, the turn-on characteristics must also be resolved.

The turn-on I_{ds}–V_{ds} characteristics of a 0.1 μm Si-SOI MESFET with $\phi_{Bn} = 0.64$ V, $N_D = 4.0 \times 10^{17}$ cm^{-3} and $t_{Si} = 35$ nm are shown in Fig. 7, for two values of t_{ob}, 300 and 120 nm. Note that the chosen $t_{Si} = 35$ nm locates within ART for $N_D = 4.0 \times 10^{17}$ cm^{-3}, as shown in Fig. 6. The applied gate bias is limited by the built-in voltage of the Schottky gate to avoid the forward conduction of semiconductor–metal contact, as discussed above. It is observed that the device with $t_{ob} = 300$ nm exhibits a considerable 2D effect in the saturation region, i.e., the drain current increases as the drain bias increases but does not saturate, while the device with $t_{ob} = 120$ nm shows greater improvement on the 2D effect. The 2D effect can be analysed in detail by plotting the equipotential contours of these devices. Figure 8 shows the 2D equipotential contours of the devices for $t_{ob} = 300$ and 120 nm at $V_{ds} = 0.5$ V and $V_{gs} = 0.4$ V (in the saturation region). The drain flux lines (defined by the normal gradient of equipotential contours) for the $t_{ob} = 300$ nm case extend into the channel and further approach the source side. This means that a large amount of channel charges are controlled by the drain. As t_{ob} is reduced to 120 nm, the bottom-gate controllability over the channel is increased, and the drain flux lines extend less. It is important to point out that the drain current in the linear region and the current level at the saturation point are kept unchanged, and the 2D effect in the saturation region is effectively suppressed by reducing the thickness of the buried oxide.

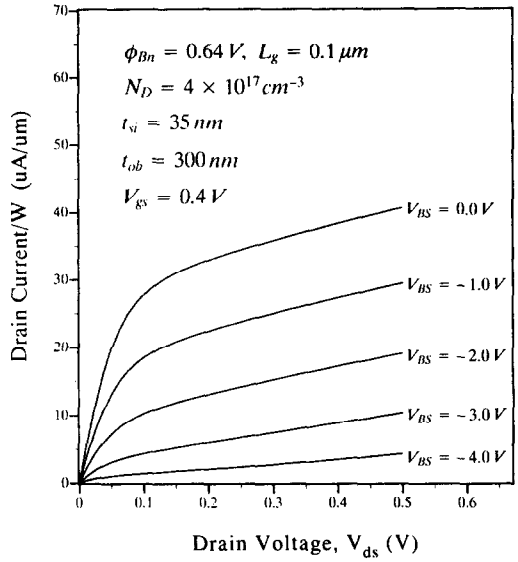

Fig. 9. I_{ds}–V_{ds} characteristics of a 0.1 μm Si-SOI MESFET with $\phi_{Bn} = 0.64$ V, $N_D = 4.0 \times 10^{17}$ cm^{-3}, $t_{Si} = 35$ nm, and $t_{ob} = 300$ nm for different backgate biases.

Another important parameter of the SOI MESFET is the backgate bias. The backgate bias keeps the equipotential confinement along the bottom surface of the buried oxide, and prevents the drain flux from extending into the channel. As discussed in Section 2, the backgate bias causes a constant threshold-voltage shift, and also modulates the turn-on I_{ds}–V_{ds} characteristics, as shown in Fig. 9, in which V_{BS} varies from 0.0 to -4.0 V, with $V_{gs} = 0.4$ V and the other parameters kept the same as in Fig. 7. In some applications, the saturation drain current level is an important performance indication, which can be easily controlled by the backgate bias, in addition to the structure parameters discussed above. Therefore, the backgate bias increases the design flexibility in the circuit level. For example, V_{BS} is kept zero for complementary-type circuits, while it can be applied to logic circuits using all SOI n-MESFETs.

4. CONCLUSION

A 2D numerical simulator is used to analyse the basic characteristics of a self-aligned MESFET fabricated on the modern SOI thin film. The design considerations and the important parameters have been discussed, based on the 2D numerical analysis of the SOI MESFET. Moreover, a design strategy for the Si-SOI MESFET has been proposed in a step-by-step manner, and an example for designing a very short gate length (0.1 μm) device has been given. The thickness of silicon film for a desired doping level and specified threshold voltage is determined by means of

the rule of ART, which is obtained by examining the sub-threshold I_{ds}–V_{gs} characteristics. The turn-on I_{ds}–V_{ds} characteristics can be adjusted by reducing the thickness of the buried oxide or applying the backgate bias. The former suppresses the 2D effect in the saturation region efficiently, while the latter modulates the characteristics in both the sub-threshold and saturation regions. Hence, the backgate bias is an important parameter in addition to the structure parameters. Compared with a MOSFET or GaAs MESFET, the design of a Si-SOI MESFET is relatively simple, and a very short gate length SOI MESFET with high performance and high flexibility can be easily obtained.

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