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One bipolar transistor selector - One resistive random access memory device for cross bar memory array

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A bipolar transistor selector was connected in series with a resistive switching memory device to study its memory characteristics for its application in cross bar array memory. The metal oxide based p-n-p bipolar transistor selector indicated good selectivity of about 10^4 with high retention and long endurance showing its usefulness in cross bar RRAM devices. Zener tunneling is found to be the main conduction phenomena for obtaining high selectivity. 1BT-1R device demonstrated good memory characteristics with non-linearity of 2 orders, selectivity of about 2 orders and long retention characteristics of more than 10^5 sec. One bit-line pull-up scheme shows that a 650 kb cross bar array made with this 1BT1R devices works well with more than 10 % read margin proving its ability in future memory technology application. © *2017 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution (CC BY) license (http://creativecommons.org/licenses/by/4.0/).* [http://dx.doi.org/10.1063/1.4994948]

Resistive random access memory (RRAM) is one of the emerging non-volatile memory technology due to its simple structure, high density, low operating power read/write operations, fast read and write speeds, etc.[1–6] However, the sneak path current is the major problem which restricts this technology from making high density cross bar memory array.[7] Using a selector device connected in series with the RRAM device is the best solution to overcome this challenge and fabricate high density, large size cross bar memory array. Various types of selectors were under investigation like Transistors, diodes, threshold selectors, field assisted super linear threshold selector, mixed ionic-electron conduction selector etc.[8–15] However, each type of selector has their own disadvantages like high current density, low switching speed, wide spread of operating voltages, higher deposition temperatures etc. This results in the search of selectors made of different materials or working on new phenomena to overcome these problems and obtain a selector that fits well with the RRAM devices to make high density memory array. Metal-oxide based bipolar selector is one of the best devices to investigate for obtaining high non-linearity, high endurance selector device due to its advantages like variable doping concentration by easy doping methods, controllable electrical characteristics by varying the doping and good compatibility with current complementary metal oxide semiconductor (CMOS) technology. Various types of p-type semiconductors like NiO, CoO, CuO and various types of n-type semiconductors like ZnO, GZO, IGZO can be used to design p-n-p or n-p-n bipolar hetero-junction transistors to obtain high non-linearity selectors compatible to be connected with RRAM in series to obtain high density cross bar array. Bae et al.,[16] investigated a p-n-p bipolar transistor selector using p-CoO and n-IGZO semiconductors which has shown a good selectivity of about 10^4 with high retention. This work shows the pathway to study more bi-polar transistor based selectors for obtaining higher selectivity and to fabricate large size 1S1R cross bar structure for future non-volatile memory devices application. In this paper, we investigated the memory characteristics of the p-n-p bipolar transistor selector (BT) made of p-NiO and n-GZO metal-oxide semiconductors connected in series with Al_2O_3 based RRAM device (1R) for its application in cross bar memory array.

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The selector device with high selectivity and good endurance was demonstrated. The possible conduction mechanism in the selector device causing high selectivity was investigated and proposed a model to explain its tunneling mechanism. The 1BT1R structure with high non-linearity, good memory window and large retention was demonstrated.

The TaN/p-NiO/n-GZO/p-NiO/TaN bipolar transistor is fabricated on a SiO_2/Si substrate. The bottom TaN electrode is deposited by using dc sputtering technique. Then, a 5 nm P-NiO semiconductor thin film is deposited by rf sputtering method in Ar and O_2 atmosphere with Ar to O_2 ratio of 1:5. and 3 nm n-GZO semiconductor thin film is deposited with Ar to O_2 ratio 2:1. The top TaN electrode is again deposited by dc sputtering method. For the fabrication of TaN/Al_2O_3/TaN RRAM device, a 5 nm Al_2O_3 insulating thin film is deposited by rf sputtering method in Ar and O_2 atmosphere with Ar to O_2 ratio of 1:11. Figure 1 illustrates the schematic structure of the fabricated 1BT1R device with TaN/NiO/GZO/NIO/TaN p-n-p bipolar transistor selector connected in series with TaN/Al_2O_3/TaN RRAM device by making TaN bottom electrode of selector and top electrode of the RRAM as common electrode for both the devices. The electrical characteristics of bipolar selector, RRAM and 1BT1R devices are measured using Agilent B1500A semiconductor parameter analyzer.

Figure 2(a) depicts the I-V characteristics of the p-NiO/n-GZO/p-NiO bipolar transistor selector indicating that the selector device shows symmetrical I-V characteristics for both positive and negative bias. The selectivity of the BT selector calculated using half-bias read scheme is found to be about 8×10^3 at a read voltage of -1.6 V. The dc endurance characteristics of the BT device at voltages of -1.6 V and -0.8 V is shown in Fig. 2(b). The device possesses a clear half-bias selectivity of more than 8×10^3 up to more than 10^4 cycles. Figure 2(c) indicates the retention characteristics of the BT device measured at -1.6 and -0.8 V read voltages, respectively. A long retention for more than 10^5 s is observed for the selector. These electrical characteristics of the BT device makes it a good selector to employ with RRAM to make a cross bar array with reduced sneak path current. To understand the current conduction mechanism in the selector device, temperature dependent I-V characteristics are measured. Figure 3 (a) shows that the turn-on voltage of the selector decreased with increasing the temperature from 300 to 400 K. In a BT, the current conduction will take place either due to avalanche tunneling mechanism or Zener tunneling mechanism that happens after applying a voltage bias which is higher than the barrier height of the p-n junction. The negative temperature coefficient observed from the I-V characteristics in Fig. 3(b) confirms that the Zener tunneling mechanism is the dominant possible mechanism for the current conduction through the selector device. So, the current through the selector is highly increased after the increasing the bias voltage above the turn on voltage. By choosing the read voltage such that V_{read} is above the turn on voltage and $V_{read/2}$ is below the turn on voltage, the selector shows a high selectivity calculated according to the half-bias read scheme. Hypothetically, a bipolar hetero junction transistor shows non-linear I-V characteristics which are symmetrical in both forward and reverse bias due to Zener tunneling.[17,18] Therefore, based on this hypothesis and the confirmation from the temperature dependent measurements, we propose a possible physical model using energy band structure of the p-n-p structure as illustrated in Fig. 4 indicating the energy band diagram of the p-n-p bipolar selector at equilibrium condition. From this

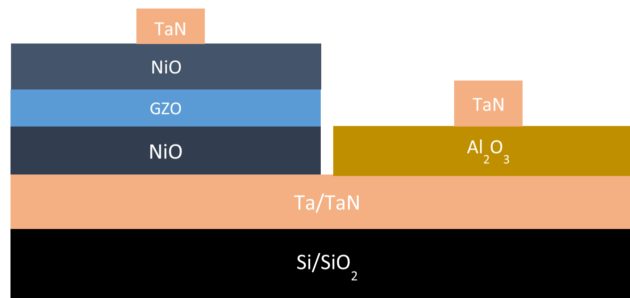

FIG. 1. Schematic structure of the 1BT1R p-n-p bipolar transistor selector – RRAM structure with bottom electrode of the selector and top electrode of the RRAM as common.

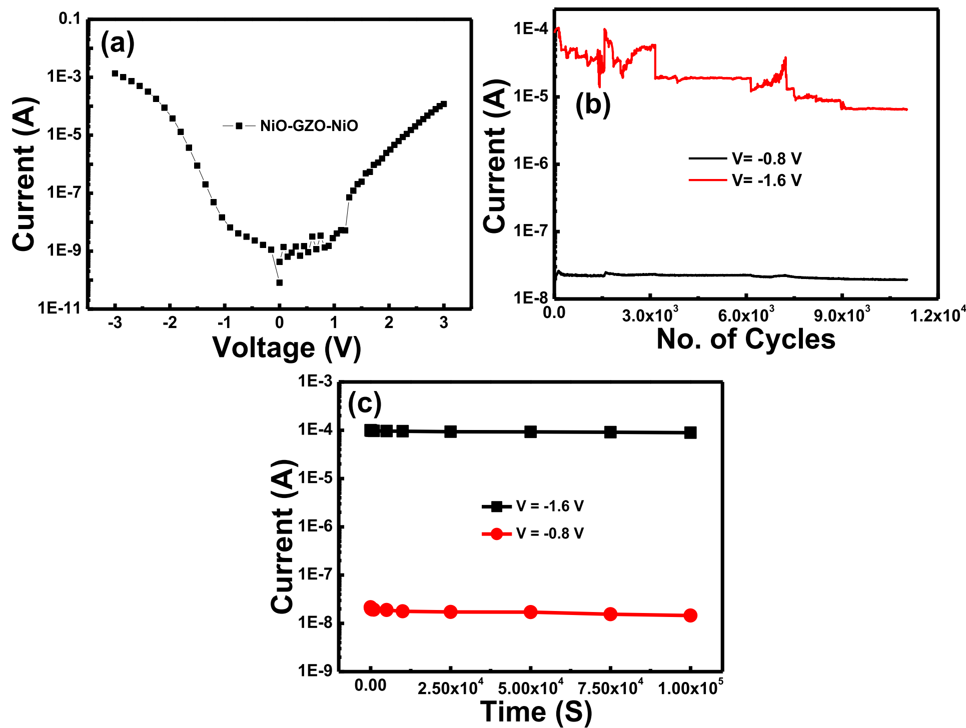

FIG. 2. (a) Current-Voltage characteristics of the TaN/p-NiO/n-GZO/p-NiO/TaN bipolar transistor selector device. (b) DC endurance characteristics of the bipolar transistor selector (c) Retention characteristics of the bipolar transistor selector device.

figure, the barrier height at the NiO/GZO junction at equilibrium is found to be about 1 eV. When a voltage bias less than turn on voltage is applied, the current flowing through the device is minimum as the p-n-p device has an inherent reverse bias junction for both the applied bias voltages. As the applied bias voltage is increased above the turn on voltage, the electrons will tunnel through the reverse bias junction due to the Zener breakdown at the reverse junction as shown in Fig. 4(b) and a large current flows through the device resulting in a high selectivity of the selector device.

To observe the performance of the bipolar selector in connection with a RRAM, TaN/Al_2O_3/TaN RRAM device is used. Figure 5(a) shows the I-V characteristics of the RRAM device showing a forming free, highly stable memory characteristics with set and reset voltages below ±0.5 V and on/off resistance ratio of about 2 orders at read voltage of -0.1 V. The presence of large amount of

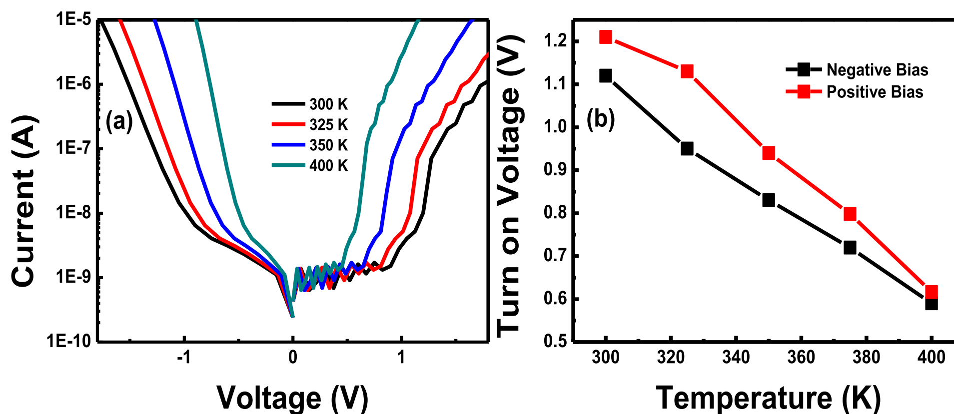

FIG. 3. (a) Temperature dependent current-voltage characteristics of bipolar transistor selector device (b) Dependence of turn-on voltage on the temperature of the device during both positive and negative bias conditions.

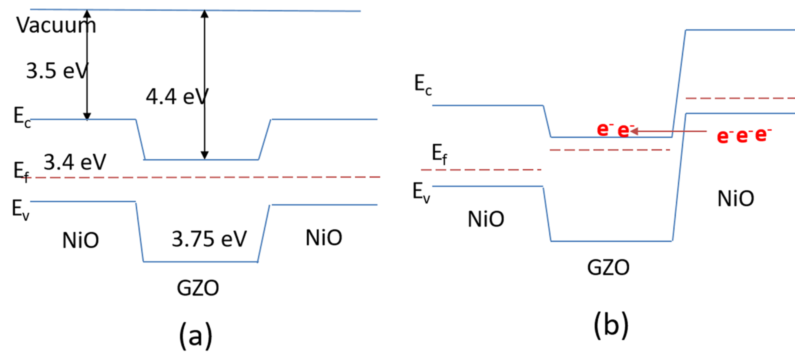

FIG. 4. (a) Schematic energy band diagram of the NiO/GZO/NiO p-n-p bipolar transistor selector in equilibrium condition. (b) Energy band diagram of the bipolar transistor selector after applying a positive voltage bias representing the tunneling of the electrons at the reverse bias junction due to Zener break down.

O_2 gas during the sputtering has controlled the oxygen vacancy density throughout the Al_2O_3 film, obtained a suitable amount of oxygen vacancies and reduced the intermediate state resistance of the fresh RRAM device. So, for a small applied bias voltage, the oxygen vacancies already present in the Al_2O_3 film were used in the formation of the conduction filament path and the device changed to LRS state. This made the device forming free and more suitable for its integration with the BT selector to form the 1BT1R crossbar arrays. The current compliance during the set process is set to 1 mA to restrict the device from the breakdown. The fluctuation of the set voltage is very small with variation less than ±0.1 V and that of the reset voltage is little higher of the range ±0.2 V. Figure 5(b) depicts the endurance characteristics of the RRAM device with on/off resistance ratio of 2 orders for more than 10^4 dc voltage cycles. Retention characteristics of the RRAM shown in

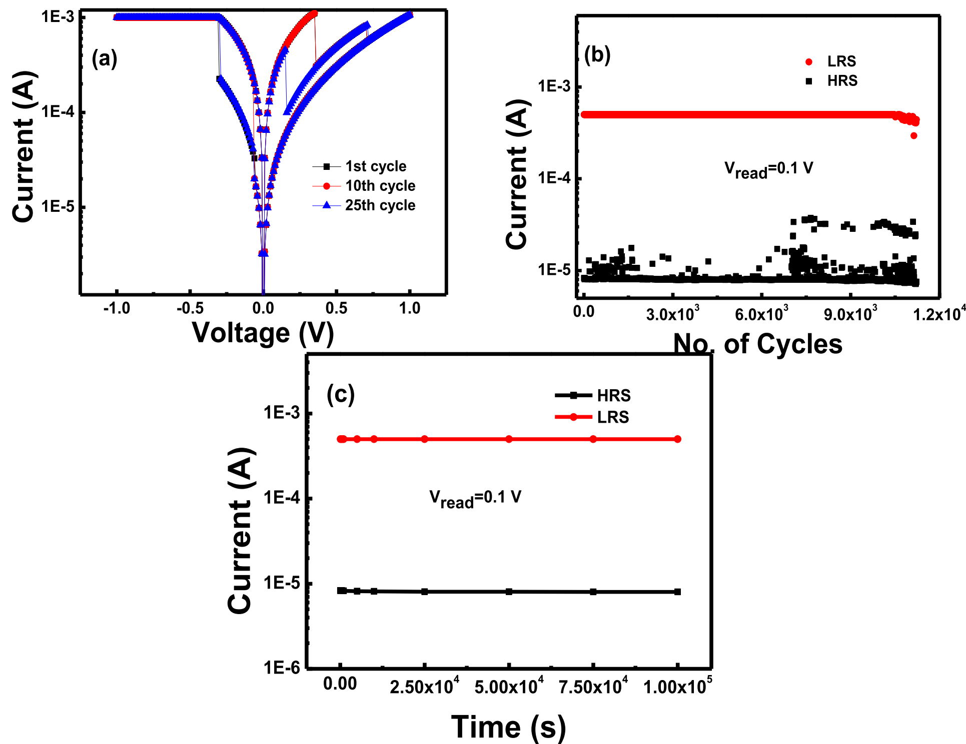

FIG. 5. (a) Current-Voltage characteristics of the TaN/Al_2O_3/TaN resistive memory device. (b) DC endurance characteristics and (c) Retention characteristics of the RRAM device.

Fig. 5(c) indicate that the RRAM device has stable retention characteristics for more than 10^5 s proving its good performance as the memory device.

Finally, the memory characteristics of the 1BT1R device are measured by applying bias voltage on the top of the selector device and grounding the top electrode of the RRAM device. Figure 6(a) shows the I-V characteristics of the 1BT1R device indicating set and reset of the RRAM device with high non-linearity ratio. The set and reset voltages of the 1BT1R device are increased to -2.3 and 2.1 V, respectively as compared with those of RRAM device. The voltage drop across the selector device can be attributed to these increased set and reset voltages of the 1BT1R device. The device possesses a good on/off resistance ratio of about 50 at the read voltage of -1.6 V and the non-linearity of about 10^2in half-bias read scheme at voltages of -1.6 and -0.8 V. Figure 6(b) shows the dc endurance characteristics of the 1BT1R device measured for 500 cycles at -1.6 V and -0.8 V which are read and half-read voltages. The device has stable non-linearity and on/off ratio with no variation up to the 500 dc sweep cycles making it attractive for the fabrication of cross bar memory array. Figure 6(c) shows the retention characteristics of the 1BT1R device measured at read voltage of -1.6 V. The device demonstrates excellent retention characteristics for more than 10^5 s with stable on/off resistance ratio of about 50. The non-linear factor of the 1BT1R device during the low resistance state measured at the voltages of -1.6 and -0.8 V is about 5×10^3 which is comparable to the other selector devices making it a good competitor for making 1BT1R crossbar memory array for the real time device application.[10,19,20]

In case of cross bar memory array, the cross talk between the adjacent memory cells restricts the maximum possible size of the array. Especially when all the memory cells in the array are in low resistance state, the sneak path leakage problem will be highly predominant in the array. Therefore, to obtain the maximum possible cross bar array size, the worst case read scheme is utilized to measure the number of possible word lines with read margin of more than 10 % which is called the one-bit pull-up scheme.[10,21–24] In this model, the bit line of the selected cell is biased to the read voltage, the word line of the selected cell is grounded and all the other word and bit lines are left floated as shown

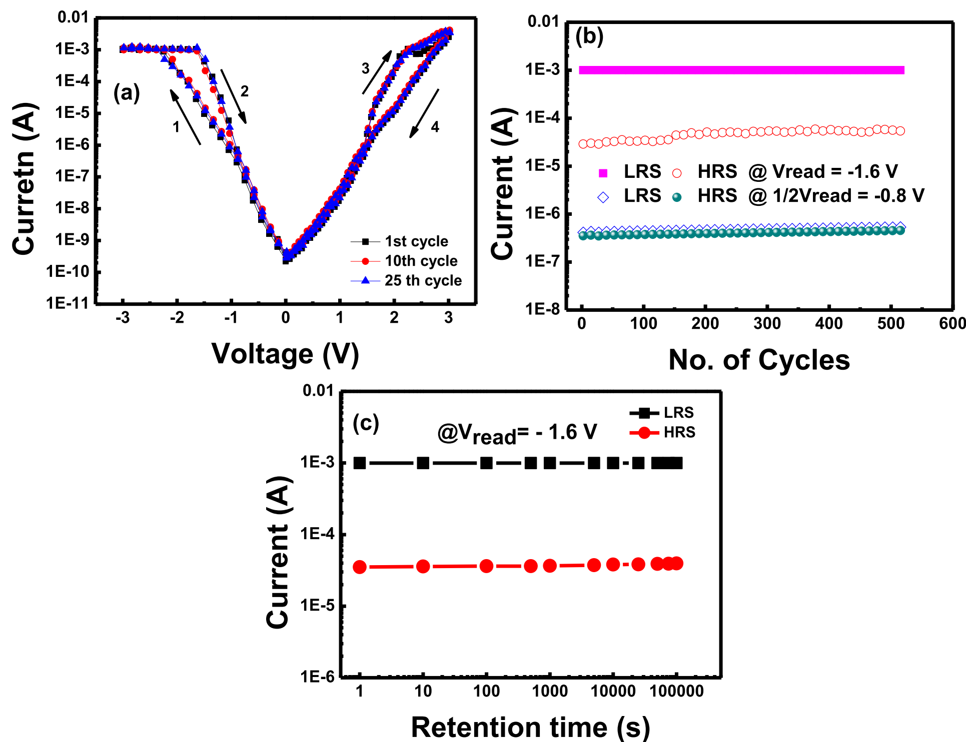

FIG. 6. (a) Current-Voltage characteristics of the 1BT1R device. (b) DC endurance characteristics and (c) Retention characteristics of the 1BT1R device.

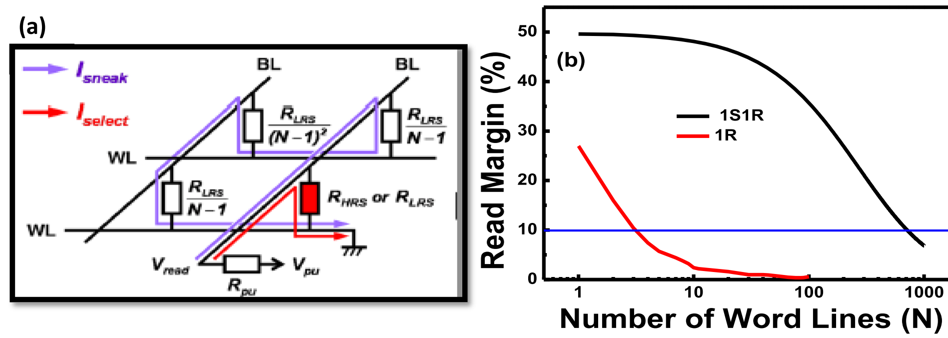

FIG. 7. (a) Schematic diagram representing the circuit of N×N cross bar memory array during one bit-line pull-up scheme. Reprinted with permission from Liu *et al.*, Appl. Phys. Lett. 100, 153503 (2012). Copyright 2012 AIP publishing LLC[24]. (b) Dependence of the read margin on the cross bar line number for both RRAM and 1BT1R structures.

in Fig. 7(a). The resistance state of the selected cell will be found by measuring the output voltage across the pull up resistor, R_{pu}. To obtain the best result during the measurement the pull up resistor value will be set to the resistance during the low resistance state ($R_{pu}= R_{LRS}$).[21] The read margin normalized to the pull up voltage is calculated by solving the Krichhoff equation

$$\frac{\Delta V}{V_{pu}} = \frac{R_{pu}}{\left(R_{LRS}\left(V_{read}\right) \parallel \left(\frac{2R_{LRS}\left(\frac{V_{read}}{2}\right)}{N-1} + \frac{R_{LRS}\left(\frac{V_{read}}{2}\right)}{(N-1)^2}\right)\right) + R_{pu}} - \frac{R_{pu}}{\left(R_{HRS}\left(V_{read}\right) \parallel \left(\frac{2R_{LRS}\left(\frac{V_{read}}{2}\right)}{N-1} + \frac{R_{LRS}\left(\frac{V_{read}}{2}\right)}{(N-1)^2}\right)\right) + R_{pu}}.$$

Figure 7(b) shows the calculated read margin for both the RRAM device and 1BT1R device for different number of word lines. From the Fig., it is clear that the read margin reduced drastically for RRAM devices and the number of word lines with at least 10 % read margin is found to be 3 only. In case of 1BT1R device, the non-linearity of the device resulted in increased number of word lines to 806 for 10 % read margin, making a 600 kb possible cross bar array fabrication with good working possibility. Enhancing the selectivity of the selector can result in further increase of the cross bar array size to get a high density and large size cross bar memory array.

In conclusion, p-n-p bipolar selector has shown a good selectivity of about 10^4 and the device performed well up to 10^4 dc sweep cycles. Temperature dependent I-V characteristics has confirmed the Zener tunneling is the possible conduction phenomena resulting in high non-linearity of the selector device. The bipolar p-n-p selector connected in series with RRAM device has shown excellent memory characteristics with non-linearity factor of more than two orders and on/off resistance ratio of about 50. The calculations made by using one bit-line pull-up scheme shows that the maximum possible cross bar memory array size using 1BT1R device is about 600 kb which makes it attractive for the future cross bar memory technology.

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