The Effect of Preheating Treatment on Anodic Al_2O_3 Formed on Sputtered Al Thin Films

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ABSTRACT

Al_2O_3 layers were grown by anodizing Al films sputtered on borophosphosilicate glass/SiO_2/Si substrates and subsequently characterized by transmission electron microscopy, and by current-voltage and capacitance-voltage measurements using a metal/insulator/metal structure. Amorphous anodic oxide is formed on nonpreannealed Al film but a complex oxide film generally consisting of five sublayers (designated as amorphous I, porous I, crystalline, porous II, and amorphous II) is formed on preannealed Al film. Freshly formed anodic oxide is always amorphous in both preannealed and nonpreannealed Al thin films. The growth of the crystalline layer in preannealed samples is due to the amorphous-to-crystalline transition of the amorphous II layer. The porous I layer is formed well before the crystalline layer. The voids in this layer are probably due to the trapping of oxygen at the sites of crystalline oxide. The voids in the porous II layer are small and their formation can be attributed to the volume shrinkage associated with the amorphous-to-crystalline transition of the amorphous II layer. The amorphous oxide films exhibit excellent dielectric properties. The dielectric properties of the complex oxide are much inferior and vary significantly due to structural variation.

Introduction

The propensity of hillock formation in thin film Al metal on SiO_2 substrate during thermal process has, until recently, prevented its application in thin film transistors (TFT)/liquid crystal display (LCD). However, a recent report of using anodic aluminum oxide as a protective coating against hillock formation has prompted renewed interest in Al metallization for TFT/LCD. [1] The primary advantage of Al over the conventional Cr or Ta metallization in TFT/LCD is its low resistivity that results in reduced gate pulse delay and wave form distortion,[2,3] a necessity for making large size, high resolution LCD. Additionally, the well-established process technology and integrated circuit (IC) compatibility of Al metallization is also welcome from processing point of view.

The anodic Al_2O_3 oxide for IC applications is typically an impervious barrier film produced by a nonsolvent electrolyte that does not dissolve oxide.[4,5] The structure of the barrier-type anodic Al_2O_3 oxide film may be either amorphous, crystalline, or a mixture of both, depending on the anodizing conditions.[6-8] The properties of anodic oxide is significantly affected by its structure, and generally the amorphous Al_2O_3 films exhibit better dielectric properties than the crystalline and mixed films.[8,9] The surface condition of the Al metal prior to anodizing is one of the important factors in determining the anodic oxide structure.[5,10] Aluminum is easily oxidized in air so that a thin air-formed native oxide is often present on the surface.[10,11] Deliberate thermal treatment of Al, especially at temperatures higher than 400°C, can induce crystalline Al_2O_3 nuclei to form on the surface.[6,11-14] The nature of the crystalline nuclei is not yet clear, but the spinel γ-phase has been suspected.[11] The nuclei grown into isolated lenticular clusters frequently accompanied with voids during subsequent anodizing and thier crystal structure has been confirmed to γ'-Al_2O_3.[11-14] Both γ- and γ'-Al_2O_3 have a closed-packed oxygen lattice, their structures differ only in the degree of ordering in the positions of the aluminum atoms.[8] Since the growth of barrier anodic Al_2O_3 oxide occurs at both electrolyte/oxide and oxide/metal interfaces,[15] the lenticular γ'-crystallites are always observed to be dispersed near the centerline of the oxide film where the original top surface is located. Prolonged anodizing caused the γ'-crystallites to grow laterally and eventually a crystalline layer sandwiched betwen amorphous oxide may be formed.[6,14] In contrast, crystalline Al_2O_3 grown by thermal oxidation of Al metal at elevated temperature (400 to 600°C), either in air[16] or in vacuum,[16,17] is predominantly the γ-phase. The morphology varies with the orientation of the underlying Al substrate, being elongated platelets on (110),[16] triangular-hexagonal platelets on (111)[16] and square[17] or trianglular-hexagonal platelets on (100).[16] Voids are not observed with the crystalline oxide formed by thermal oxidation.

While most of the previous studies were made on aluminum sheets, it is of great interest to study the anodizing of Al thin films used for IC applications. In previous papers we have studied the effects of 1% Si and 0.5% Cu doping[14] and of electrolyte temperature[18] on the structure and properties of anodic oxide films formed on sputtered thin Al metal films. In this paper the effect of pretreatment is studied in detail.

Experiment

The substrates for the present study were 4 in. diam p-type, <100>, Si wafers. To simulate a typical glass substrate used for LCD, a 550 nm thermal oxide was first grown on the substrate and a 600 nm thick borophosphosilicate glass (BPSG) was subsequently deposited by chemical vapor deposition at 720°C. A 300 nm thick Al film was deposited in a dc magnetron sputtering deposition machine from a pure Al target on top of the borophosphosilicate glass (BPSG) SiO_2/Si substrates. To investigate the effect of preannealing on the anodic oxide formation, two series of samples were prepared. For the first series, the wafers were anodized directly after the metal deposition. For the second series, the wafers were annealed at 410°C for 30 min in a nitrogen (99.99995%, oxygen content 0.1 ~ 0.2 ppm) ambient prior to anodizing. For both series, the Al_2O_3 dielectric layer was grown by anodizing the wafers, one at a time, at room temperature in an acid-glycol-water (AGW) electrolyte that is a mixture of 3% aqueous solution of tartaric acid and propylene glycol at a volume ratio of 2:8. The cathode was plain stainless steel and typically about 90% of the wafer was immersed in the electrolyte while the exposed region was connected to the anode through a Cu clamp. Anodization was controlled by a programmable Keithley 237 current/voltage source-measure unit interfaced to a personal computer. Anodization was conducted in constant current mode (current density = 0.4 mA/cm^2) initially and was switched

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to constant voltage mode automatically when the voltage reached 100 V. To investigate the structure of the oxide films formed at different stages of anodization specimens were anodized for different duration varying from 3.5 to 40 min and characterized subsequently by transmission electron microscopy (TEM). TEM samples were prepared by ion milling in the usual fashion[19] and examined within a Philips CM20 microscope operating at 200 kV. High resolution TEM work was performed with a JEOL 4000 microscope operating at 400 kV. The thickness of the anodic films was measured both by TEM and by ellipsometry using a Rudolph Research Auto EL-ILL ellipsometer with He-Ne laser at the wavelength of 632.8 nm. The dielectric properties of the anodic oxide films formed on both preannealed and nonpreannealed wafers after 40 min anodization were also studied by current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements using a metal/insulator/metal (MIM) structure. To fabricate the MIM capacitors, a 400 nm thick Al film was further deposited by dc magnetron sputtering on the anodized wafers. The capacitor electrodes, 200 × 200 μm squares, were defined using standard lithography and reactive ion etching. The *I-V* measurements were carried out with a HP 4145B semiconductor parameter analyzer and the high frequency (1 MHz) capacitance measurement was performed using a Keithley 82 C-V system.

Result and Discussion

The variations of the anodizing voltage and anodizing current with time are shown in Fig. 1 and 2, for the preannealed and nonpreannealed samples, respectively. The initial rise of voltage in Fig. 1 corresponds to the constant current anodization. The initial zero-time voltage is sensitive to the process history prior to anodizing. The fact that the preannealed sample requires a lower voltage during the constant current anodization indicates that patches of thin oxide regions had already formed on the metal surface during preannealing thus reducing the clean metal area so that a lower applied voltage is required relative to the nonpreannealed sample in order to maintain the same current density. The rate of increase in voltage (defined as voltage growth rate) during the constant current period varies slightly for the two samples, being 0.206 V/s for the nonpreannealed sample and 0.214 V/s for the preannealed one. In Fig. 2, the sudden drop of the anodic current at 30 mA signifies the onset of constant voltage mode (*i.e.*, the voltage has reached 100 V). Apparently, for the preannealed sample the anodizing voltage reaches 100 V at a later time, but the current decreases more sharply and

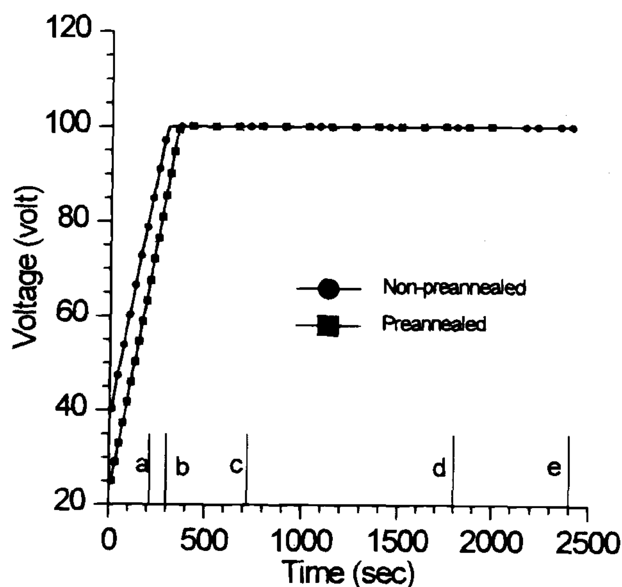

Fig. 1. The variation of anodizing voltage with time.

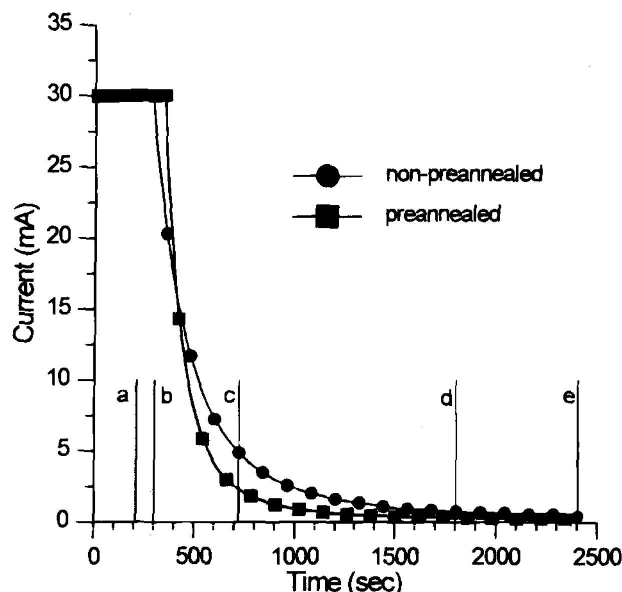

Fig. 2. The variation of anodizing current with time.

eventually reaches a lower minimum residual current in this sample than the nonpreannealed sample. The total electrical charge consumed during anodizing is equal to the area under the *I-t* curve and is 15.8 and 17.4 C for the preannealed and nonpreannealed sample, respectively. The amount of oxide formed on the sample is proportional to the quantity of charge consumed; assuming equal current efficiency this implies that the capacitance of the preannealed sample may be lower than the nonpreannealed sample.

The current efficiency for the anodizing process may be estimated from the total charge consumed and the volume of the oxide formed. The total electrical charge consumed can be calculated from the area under the *I-t* curve in Fig. 2 and the volume of the oxide layer can be measured from the TEM micrographs shown in Fig. 3 and 4. (For oxide films containing voids the volume of the voids is subtracted from the total volume of the oxide film.) An oxide density of 3.1 and 3.6 g/cm^3 is assumed for the amorphous[20] and crystalline[21] anodic aluminum oxide, respectively. The calculated current efficiency for the oxide formation is 97% for the nonpreannealed sample and 87% for the preannealed sample. The lower efficiency for the preannealed sample is not unexpected in view of the large amount of defects, such as voids and crystallites, formed in the oxide films.

The cross-sectional TEM (XTEM) micrographs of the nonpreannealed oxide films anodized for different durations are shown in Fig. 3. These oxide films are basically featureless implying an amorphous structure. the microstructure of the preannealed oxide films anodized for 210, 300, 720, 1800, and 2400 s are shown in Fig. 4a, b, c, d, and e, respectively. (These samples are corresponding to the vertical lines marked as a, b, c, d, and e in Fig. 1 and Fig. 2, respectively.) In contrast to the oxide films formed in the nonpreannealed samples the oxide films in the preannealed samples are much more complex. Generally speaking they are composed of five layers designated, from the top to the bottom, as amorphous I, void I, crystalline, void II, and amorphous II layers as labeled in Fig. 4d. It is well known that anodic aluminum oxide grows at both electrolyte/oxide and oxide/metal interfaces due to the outward transport of Al ions and the inward transport of oxygen ions.[10,22,23] The fact that the oxide structure at these two interfaces (*i.e.*, the amorphous I and amorphous II layer, respectively) is amorphous all the time indicates that the freshly formed anodic Al oxide is always amorphous. The void I layer contains many small voids initially (Fig. 4a) and

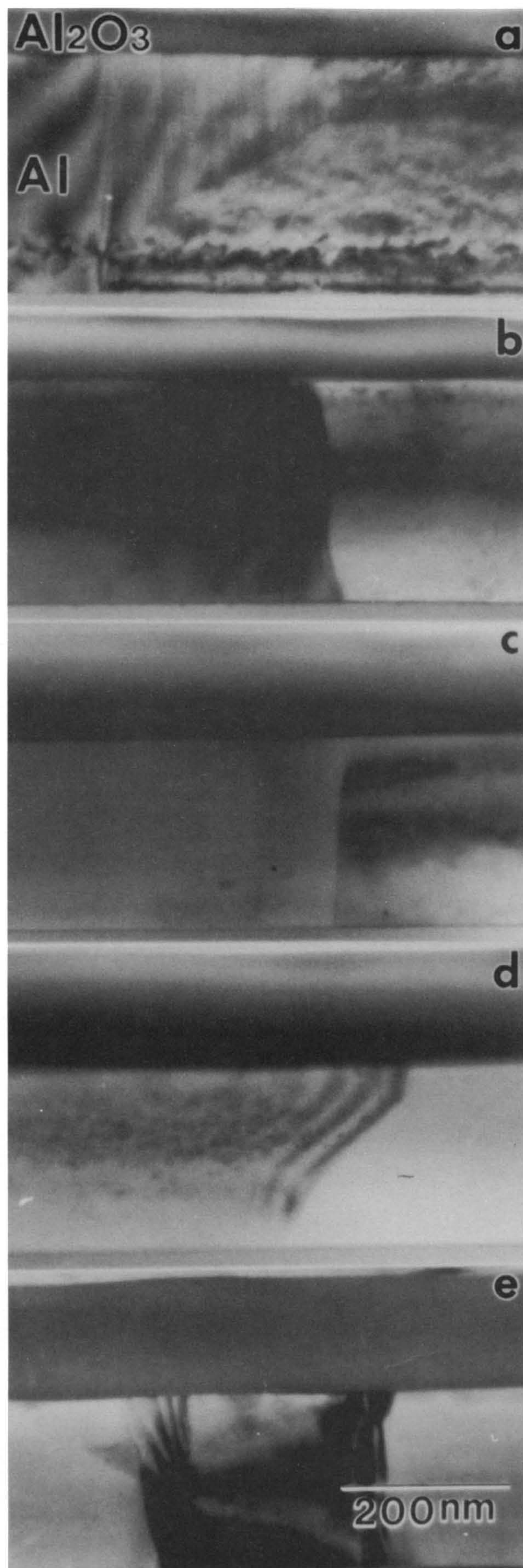

Fig. 3. Cross-sectional TEM micrographs of Al_2O_3 films formed on nonpreannealed Al metal films. The anodizing time was (a) 210, (b) 300, (c) 720, (d) 1800, and (e) 2400 s.

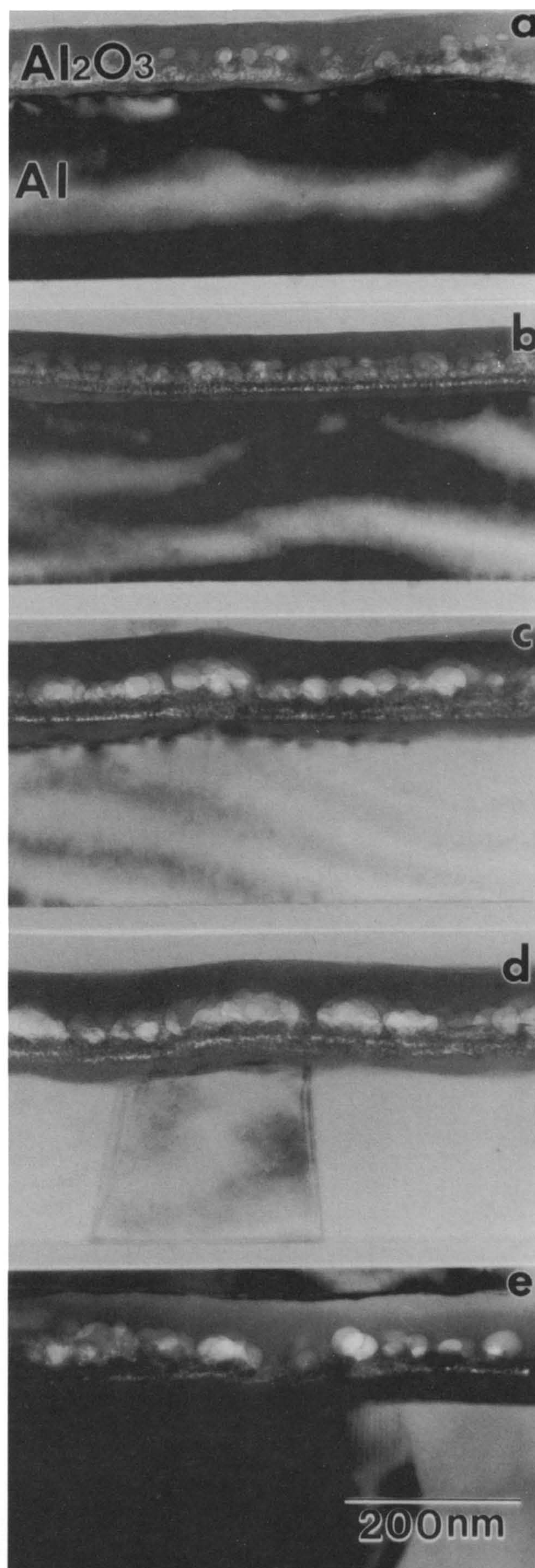

Fig. 4. Cross-sectional TEM micrographs of Al_2O_3 films formed on preannealed Al metal films. The anodizing time was (a) 210, (b) 300, (c) 720, (d) 1800, and (e) 2400 s.

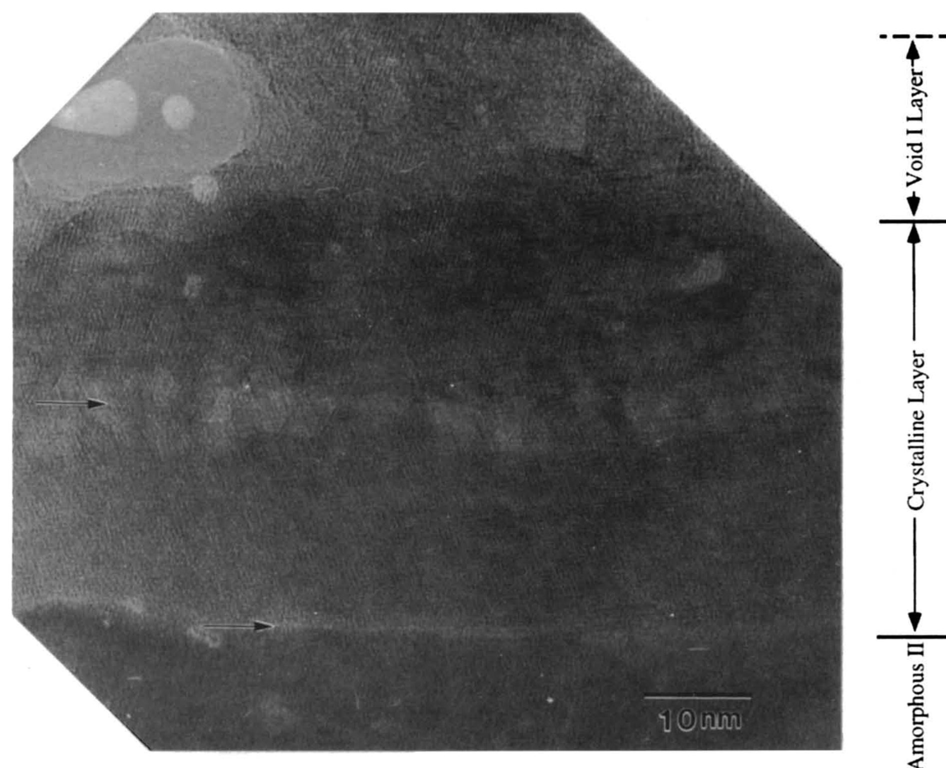

Fig. 5. High resolution TEM micrographs of the Al_2O_3 layer shown in Fig. 4e. Both γ'-Al_2O_3 crystallites and amorphous patches are discernible.

the number of voids increases on further anodizing under constant current condition (Fig. 4b). Significant void coalescence is observed under constant voltage condition (Fig. 4c, d, and e). Figure 5 shows a cross-sectional high resolution TEM (HRTEM) micrograph of the oxide film taken from the same TEM specimen shown in Fig. 4d. The crystalline layer is marked in this micrograph and its crystallinity is confirmed by the faint lattice fringes revealed. Our previous study[14] has identified the crystallites as γ'-Al_2O_3. A large void belonging to the void I layer is observed in contact with the crystalline layer in Fig. 5. The area neighboring this void appears to be amorphous but lattice fringes are visible further to the right of the void. This suggests that the void I layer is a mixed amorphous + crystalline layer laden with voids. The micrographs in Fig. 4 show clearly that the crystalline layer is always formed beneath the void I layer, but its relative position with respect to the void II layer varies. Initially the crystalline layer is on top of the void II layer as shown in Fig. 4b, but as the crystalline layer grows thicker the void II layer becomes either at the bottom or inside of the crystalline layer as revealed clearly in Fig. 4d (as well as in Fig. 4c and e). The two lighter bands in Fig. 5, one near the center and the other at the bottom of the crystalline layer (marked by arrow), correspond to the voids in the void II layer in Fig. 4d.

It should be emphasized that voids are formed only in the preannealed samples but not in the nonpreannealed samples in the present investigation although exactly the same anodizing conditions were used for both cases. Similar voids have also been reported in anodic aluminum oxide formed on preannealed Al-1 weight percent (w/o) Si-0.5 w/o Cu thin films[14] and on preannealed aluminum foils anodized in various electrolytes such as tartaric acid,[14] ammonium pentaborate,[7,12] and ammonium borate,[24] etc. The formation of voids in anodic aluminum oxide is apparently independent of anodizing electrolytes and substrate composition but depends on preannealing treatment and electrolyte temperature.[18] It has been shown convincingly[6,10,13] that preannealing causes crystalline γ-Al_2O_3 nuclei to form on the surface of aluminum which eventually develop into a crystalline layer during subsequent anodic growth. Since the void I layer is fully developed even before the formation of the crystalline layer (comparing, for example, Fig. 4a and 4b), the origin of the voids in the void I layer in our preannealed samples cannot be ascribed to the volume shrinkage associated with the amorphous to crystalline transition of the existing amorphous oxide.[6] These voids are most likely the result of oxygen trapped near the γ'-$Al_2 0_3$ crystallites which eventually form gas bubbles.[7]

The nature of void II layer is quite different from void I layer. In Fig. 4a we see that this layer has not formed yet. It forms only after the appearance of the crystalline layer in Fig. 4b, and the voids in this layer are much smaller compared with those in the void I layer. The voids in the void II layer may be due to the volume shrinkage accompanied the amorphous to crystalline transition.

The thickness of each individual layer in Fig. 4 can be measured directly off the micrographs and the data are summarized in Table I. It is worth pointing out that, in order to eliminate any error in the thickness measurement, the TEM specimens were tilted such that the <110> zone axis of the substrate silicon is aligned to the incident beam direction. This ensures that the oxide layers shown in Fig. 3 and 4 are viewed in the end-on fashion. Also, the magnifications of TEM micrographs were calibrated against a standard specimen.

It should be borne in mind in discussing Table I that the anodizing process in the present study consists of two regimes, a constant current regime followed by a constant voltage regime. Figure 6 shows the variation of the total thickness of the oxide layer (the data shown in the last row of Table I) as a function of anodizing time. The switch-over from the constant current mode to the constant voltage mode is marked by the vertical dashed line in Fig. 6. Despite the vast difference in the microstructure of the preannealed and nonpreannealed, the thickness variation of the oxide films formed on these two types of samples are quite similar as shown in Fig. 6. The initial portions of the two curves in Fig. 6 (corresponding to the constant current regime) are practically indistinguishable. Only at the end of the anodizing the oxide thickness in the nonpreannealed samples appears slightly higher than those in the preannealed samples. The growth rate of the anodic aluminum oxide is aobut 0.34 nm/s initially

Table I. Layer thickness of the Al_2O_3 films anodized for different time.

Preannealed Films		Thickness (nm)				
		Const. current		Const. voltage		
Layer	Type	210 (s)	300 (s)	720 (s)	1800 (s)	2400 (s)
1	Amorphous I	32	32	42	44	46
2	Void I	24	24	27	29	30
3	Crystalline	7	8	17	21	21
4	Void II	0	5	6	7	7
5	Amorphous II	12	14	23	24	26
Total thickness		75	83	115	125	130
Nonpreannealed films		69	79	125	133	135

during the constant current regime as determined from the slope of the curves in Fig. 6. The growth continues though at an ever decreasing rate even after switching over to the constant voltage mode and eventually comes to a halt as indicated by the plateau of the curves.

It is of particular interest to know how each of the five individual layers in the anodic oxide film varies with anodizing time in order to better understand the structural evolution during anodizing. For this purpose, the individual layer thickness is plotted as a function of time in Fig. 7. Close examination of this figure reveals the following.

1. The amorphous I, amorphous II, and crystalline layers exhibit similar growth behavior, namely, fast growth at roughly the same rate (0.024 nm/s) initially up to 720 s followed by very slow growth thereafter when anodizing is well into the constant voltage regime.

2. The void II layer is not formed initially (even after 210 s), but it grows very rapidly to 5 nm in 90 s (from 210 to 300 s). The thickness is not changed much subsequently, saturating at about 7 nm eventually. Note that the growth of this layer occurs mostly during constant current regime.

3. The void I layer exhibits somewhat different behavior from other layers. This layer grows to 24 nm thick after 210 s and then its thickness increases only slightly thereafter. In other words, the growth of the void I layer starts at a very early stage of the constant current regime and does not show a significant increase in thickness during the initial stage of the constant voltage regime as in the case of amorphous I, amorphous II, and crystalline layers. We have shown earlier in reference to Fig. 5 that void I layer is actually a mixed layer containing amorphous + crystalline oxide and voids. Although the thickness of void I layer does not change significantly as anodization proceeds, the amounts of voids in the layer do increase as clearly revealed in Fig. 4.

4. In terms of growth rate Fig. 7 shows clearly that void I > amorphous I > amorphous II > crystalline > void II. In terms of layer thickness, however, the most dominant features in the anodic Al oxide films are amorphous I and void I layer.

The thickening of the crystalline layer during anodizing may be caused by either or the combination of the following three mechanisms: (*i*) the gradual crystallization of the already formed amorphous I layer, (*ii*) the gradual crystallization of the already formed amorphous II layer, and/or (*iii*) the reaction of indiffusing oxygen and out-diffusing Al inside the crytalline layer.

In view of the fact that the crystalline layer and the amorphous I layer are always separated by a void I layer (see Fig. 4) the first mechanism seems to be unlikely to operate. For otherwise one should have observed the crystalline layer outgrows the void I layer so that the void I layer is inside the crystalline layer. The third mechanism, although attractive, is nevertheless inconsistent with the well-established theory of anodic aluminum oxide growth, namely, the oxide is grown at two interfaces (electrolyte/oxide and oxide metal interfaces) but not inside of the existing oxide layer.[15] This leaves us with no choice but to look at the second mechanism. First, it is interesting to point out that this mechanism is consistent with the results of other studies that crystallization of amorphous anodic aluminum oxide tends to occur at the bottom half of the oxide layer.[10] This phenomenon has been shown to be related to the anion incorporation from the forming electrolyte. The incorporated anions are typically found only at the top half of the oxide layer and

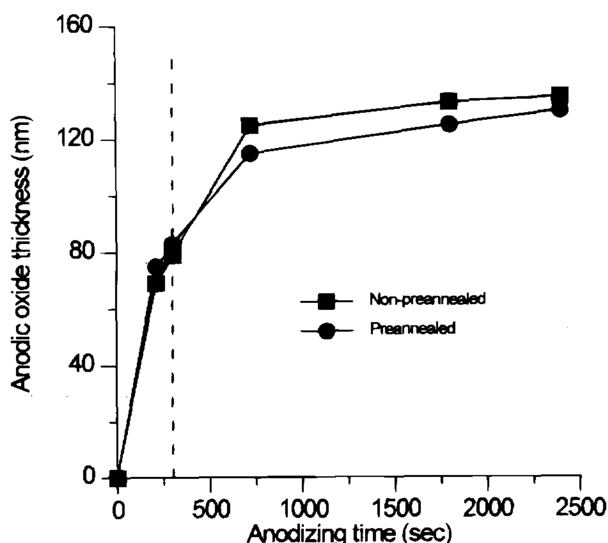

Fig. 6. The variation of total thickness of oxide layer as a function of anodizing time.

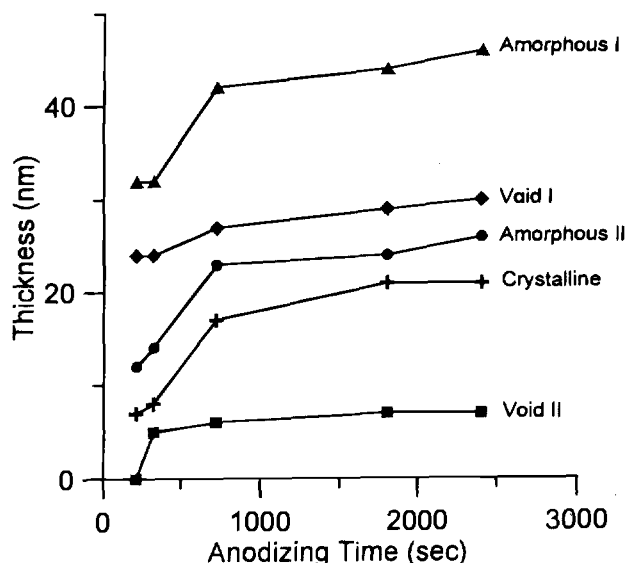

Fig. 7. The variation of individual layer thickness as a function of anodizing time for the preannealed samples.

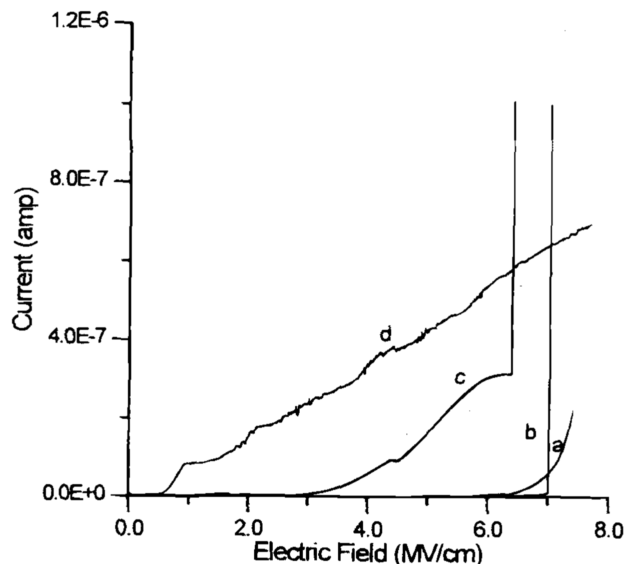

Fig. 8. *I-V* **characteristics of the anodic oxide films formed on nonpreannealed (curve a) and preannealed (curves b, c, and d) Al metal films.**

their presence hinders the amorphous-to-crystalline transition. Thus crystallization of amorphous anodic oxide initiates at the relatively pure inner region of the oxide film. We have shown in an earlier study that when Al is anodized in the AGW electrolyte as we did in the present study, carbon is indeed incorporated into the top portion of oxide layer.[18] If this mechanism is operative one would then expect the void II layer to be gradually trapped inside the crystalline layer as the latter thickens toward the oxide/metal interface. This is indeed observed as we have pointed out earlier in the discussion of Fig. 5. On the basis of the forgoing discussions we believe that the thickening of the crystalline layer is due to the crystallization of the amorphous II layer. It is probable that crystallization of amorphous anodic oxide is due to a local heating effect associated with the inhomogeneous field strength near the crystalline oxide.[13]

The *I-V* characteristics of the anodic aluminum oxide formed on sputtered Al metal in the present study are shown in Fig. 8. Curve a is typical of nonpreannealed films while curve b, c, and d represent three typical characteristics observed in the preannealed films. The probability of occurrence for the three cases in the preannealed samples is about 40, 20, and 40% for type b, c, and d, respectively. Curve a indicates that the anodic oxide formed on nonpreannealed Al films is highly insulating with extremely low leakage current and no breakdown before 7.4 MV/cm. This is not unexpected in view of the uniform, imperious, and amorphous structure of the oxide films observed in the nonpreannealed samples (see Fig. 3). The leakage current is only 2.3×10^{-7} A at 7.4 MV/cm in this case. The more complex microstructure of the oxide films formed on preannealed samples resulted in a large variation in their *I-V* characteristics. Curve b exhibits good insulating behavior up to 7.1 MV/cm then breakdown sets in suddenly, possibly caused by the onset of ionic conduction. In curve c the current starts to increase steadily when the field strength is greater than 3.2 MV/cm and dielectric breakdown occurs at 6.4 MV/cm. Curve d shows a very poor insulating characteristic, and the current is increased approximately linearly with field strength from a very early stage (~0.6 MV/cm). The current is also oscillating with the applied field strength over the entire range, and is probably due to multilevel trap levels (*Et*) and high trap density (*Nt*) in the oxide layer. As voltage is applied to oxide layer, the quantity of trap charge was not in equilibrium with the emission charge which result in current oscillation.

Table II summarizes the dielectric properties of the oxide films studied. Here, the leakage current is defined as the current at 7 MV/cm and the breakdown field is the electric field corresponding to the current of 1 μA. The oxide thickness was measured directly off the cross-sectional TEM micrographs and the dielectric constant was calculated from the capacitance and thickness data. As expected, the dielectric properties of the anodic oxide formed on the nonpreannealed films are excellent, but the preannealed films exhibit lower capacitance, lower dielectric constant, much larger leakage current, and a lower breakdown field. The dielectric constant of the amorphous nonpreannealed oxide film is 9.2 which is consistent with the published data of 8.2 to 10.2.[22]

Conclusion

1. Amorphous anodic oxide is formed on nonpreannealed Al films but a complex oxide film consisting of a crystalline layer sandwiched between two porous layers which in turn are sandwiched between two amorphous layers is formed in Al films preannealed at 410°C for 30 min.
2. Freshly formed anodic oxide layers at the electrolyte/oxide and oxide/metal interfaces are always amorphous in both preannealed and nonpreannealed Al thin films.
3. A crystalline layer is formed near the centerline of the anodic oxide layer in the preannealed samples. It grows in thickness during anodizing due to the amorphous-to-crystalline transition of the bottom amorphous layer.
4. A large porous layer (porous I) is formed well before the crystalline oxide layer in the preannealed samples. The voids in this layer are not due to volume shrinkage resulting from the amorphous-to-crystalline transition of the amorphous layer, but are probably due to the trapping of oxygen at the sites of crystalline oxide.
5. A small porous layer (porous II) is developed beneath the crystalline oxide layer in the preannealed samples. The voids in this layer are small, and their formation can be attributed to the volume shrinkage associated with the amorphous-to-crystalline transition of the bottom amorphous layer.
6. The amorphous oxide films exhibit excellent dielectric properties. The dielectric properties of the complex oxide are much inferior and vary significantly even in the same sample due to large structural variation.

Acknowledgments

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Table II. Dielectric properties of the anodic films.

Material	Capacitance (pf)		Leakage current (nA)		Oxide thickness	Dielectric	Breakdown field
	Mean	s.d.[a]	Mean	s.d.[a]	(mm)	constant	(MV/cm)
A	24.46	0.594	70.8	10.9	135	9.2	>7.4
B	20.87	4.351	>1000	N.A.	130	7.7	6.6

[a] Standard deviation.
Material A, nonpreannealed; B, preannealed.

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Dielectric Degradation of $Cu/SiO_2/Si$ Structure during Thermal Annealing

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ABSTRACT

The impact of Cu on the dielectric SiO_2 layer was studied using a $Cu/SiO_2/Si$ metal oxide semiconductor capacitor and rapid thermal annealing (RTA) treatment. With the RTA treatment, no chemical reaction was observed up to 900°C; however, dielectric degradation occurred following RTA at 300°C for 60 s and became worse with the increase of annealing temperature. The interface-trap density at the SiO_2/Si interface also increased from 5×10^{10} to 5×10^{13} eV^{-1} cm^{-2} after 800°C RTA treatment. The RTA anneal introduced a large number of positive Cu ions into the dielectric SiO_2 layer. Under bias-temperature stress, Cu ions drift quickly in the SiO_2 layer and may drift across the SiO_2/Si interface and enter the Si substrate. With the use of 1200 Å thick TiN and TiW barrier layers, respectively, the dielectric strength of the Cu/(barrier)/SiO_2/Si structures was able to remain stable up to 500 and 600°C.

Introduction

Copper has been extensively studied as a potential metallization material in ultralarge scale integrated (ULSI) circuits because of its low resistivity (1.67 $\mu\Omega$-cm for bulk) and high electromigration resistance. However, copper forms Cu-Si compounds at a relatively low temperature[1-4] and introduces deep level traps in Si.[5] In order to use Cu as a future ULSI interconnect metal, the thermal stability of Cu with the underlying materials and devices must be carefully evaluated.

In modern multilevel metallization structures, SiO_2 layers are usually employed as the interlayer dielectric; the dielectric layers not only isolate the interconnect lines of different levels, but also separate the active devices from the contacted metals. Therefore, no interaction between Cu and the enclosed dielectric layer is allowed during the post Cu-metallization thermal process. The penetration of Cu through the dielectric layer will not only degrade the dielectric layer, but will also introduce deep level traps in the Si substrate that harm device performance. Therefore, the influence of Cu contamination on the dielectric properties of SiO_2 becomes a major issue in the multilevel interconnect structure if Cu is to be used as the interconnect metal. It has been reported that Cu migrates into SiO_2 at temperatures as low as 250°C in the presence of an electric bias.[6] However, the influence of Cu on the degradation behavior of SiO_2 remains unclear.

In this study, we investigated the influence of Cu on the dielectric properties of SiO_2 layers as well as the reaction between Cu and SiO_2. The metal oxide semiconductor (MOS) capacitors of a $Cu/SiO_2/Si$ structure were fabricated and studied with regard to the electrical and metallurgical aspects. The dielectric degradation was characterized by capacitance-voltage (C-V) measurement and the dielectric strength was determined from the breakdown voltage measurement. The role of Cu in SiO_2 was investigated by interface trap density (D_{it}) and mobile ion meas-

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