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Evaluation and Reliability Assessment of GaN-on-Si MIS-HEMT for Power Switching Applications

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Abstract: This paper reports an extensive analysis of the physical mechanisms responsible for the failure of GaN-based metal–insulator–semiconductor (MIS) high electron mobility transistors (HEMTs). When stressed under high applied electric fields, the traps at the dielectric/III-N barrier interface and inside the III-N barrier cause an increase in dynamic on-resistance and a shift of threshold voltage, which might affect the long term stability of these devices. More detailed investigations are needed to identify epitaxy- or process-related degradation mechanisms and to understand their impact on electrical properties. The present paper proposes a suitable methodology to characterize the degradation and failure mechanisms of GaN MIS-HEMTs subjected to stress under various off-state conditions. There are three major stress conditions that include: V_{DS} = 0 V, off, and off (cascode-connection) states. Changes of direct current (DC) figures of merit in voltage step-stress experiments are measured, statistics are studied, and correlations are investigated. Hot electron stress produces permanent change which can be attributed to charge trapping phenomena and the generation of deep levels or interface states. The simultaneous generation of interface (and/or bulk) and buffer traps can account for the observed degradation modes and mechanisms. These findings provide several critical characteristics to evaluate the electrical reliability of GaN MIS-HEMTs which are borne out by step-stress experiments.

Keywords: DC stress; degradation; GaN HEMT; GaN MIS-HEMT; reliability; failure mechanisms; trapping

1. Introduction

AlGaN/GaN high electron mobility transistors (HEMTs) have attracted a lot of attention for both switching and radio frequency (RF) power applications [1–3]. The Schottky-gate-controlled heterojunction two-dimensional electron gas (2DEG) channel, which is widely used for high-frequency RF applications [4] is not desirable for next generation power electronics for the following reasons. Firstly, HEMTs are struggling to achieve high breakdown voltage, low on-state resistance and fast switching at the same time. Since the Schottky barrier layer suffers from possible damage in the subsequent processing steps, the large gate leakage current increases the off-state loss and reduces power supply efficiency [5,6]. Secondly, the 2DEG of conventional HEMT structures cannot be easily depleted under the gate for normally-off (E-mode) operation [7,8]. E-mode field-effect transistors (FETs) are essential in power electronics applications for avoiding circuit burnout and realizing great

simplicity in circuit design. Finally, the long-term stability and reliability of the Schottky gate HEMT remains problematic. If the devices are stressed for a sufficiently long time, the gate leakage current increases and becomes noisy, and degradation occurs even below the critical voltage [9–12].

Different approaches are proposed to reduce the gate-leakage current and enlarge the gate voltage swing. One straightforward solution is to insert a dielectric layer between the gate metal and the AlGaN layer to block the leakage current path [13,14]. The frequently-used dielectrics are Al_2O_3 and Si_3N_4, due to the large band gap and high breakdown field, and the ability to deposit high quality films by ALD (Atomic Layer Deposition), plasma enhanced CVD (PECVD) or other conventional means. However, several studies report that the Al_2O_3/nitride heterogeneous interface contains a high density of deep states that result in threshold voltage hysteresis when the transistor is used as a switching device [15,16]. For this reason, source-side breakdown mechanism in metal-insulator-semiconductor (MIS)-HEMTs is an important reliability concern [17,18]. The Si_3N_4 film could be a promising alternative candidate as a gate dielectric for GaN power MIS-HEMTs. Si_3N_4-based MIS devices can be both D-mode and E-mode. The challenge of making E-mode transistors is to maintain low on-resistance (R_{on}) with a large gate swing. D-mode MIS devices are widely used for power electronics applications in a cascode configuration with a low voltage Si-based metal-oxide-semiconductor field-effect transistor (MOSFET) in series [19–21]. Compared to the conventional HEMT structure with Schottky-gate, relatively few studies on the degradation of HEMT structure with MIS-gate are presented in the literature [22–24]. More detailed investigations are needed to identify symptoms of different degradation mechanisms and to understand how it impacts the device's electrical characterization in detail.

A method to evaluating device reliability through the short-term step-stress measurements of several figures of merit (I_{DMAX}, I_{GOFF}, R_D, R_S and V_{th}) was proposed for Schottky-gate HEMTs [25]. The voltage at which significant electrical degradation takes place is called the critical voltage (V_{CRI}) [26,27]. Within this context, the aim of this paper is to contribute to the understanding of device early failures and associated structural degradation for power electronic device designers. The impact of short-term step-stress on gate leakage current (I_{Goff}), stress gate current (I_{G_stress}), device on-resistance (R_{on}), and threshold voltage (V_{th}) are measured, statistics are studied, and correlations are investigated under several different off-state conditions.

A flow chart of a typical step-stress test is shown in Figure 1. The analysis is carried out in an on-wafer probe station equipped with thermal chuck that allows device characterization through external test equipment (two Keithley 2636B SourceMeters). The devices are kept for a long time under the different off-state stress conditions at a base plate temperature T_{base} (25 °C); in each stage, the variation in DC figures of merit (Table 1) are evaluated by switching the devices to the ON-state by means of short voltage pulses. The quick characterization techniques are used to acquire a complete description of the degradation process. Self-heating effects are not taken into account in the measurements due to the off-state stress where there should be negligible current flow and heating. In the first set of conditions, the gate-to-source voltage ($|V_{GS}|$) is increased at a constant drain-to-source voltage (V_{DS}) of 0 V; a harsh stress condition relative to the targeted normal conditions for these GaN MIS devices. The second set of experiments involves the step stressing of V_{DS} with V_{GS} biased at −20 V (off-state condition). Furthermore, the source terminal of the GaN based cascode switch is connected to the gate terminal of the D-mode MIS GaN transistor, so the voltage difference should be 0 V. In contrast to the large number of papers reporting on issues for a GaN HEMT under off-state V_{DG} stress, there are few publications focusing on reliability issues for the GaN cascode switch under off-state stress (with the gate shorted to ground) for long periods of time. In the third experiment, the source-to-gate voltage (V_{SG}) is increased at a constant drain-to-gate voltage (V_{DG}) of 20 V (off-state condition). Furthermore, 3-terminals I-V characterization techniques are also employed to identify degradation mechanism in the heterostructure.

This present paper proposes a methodology for the analysis of failure modes and mechanisms of GaN MIS HEMTs. A series of step-stress experiments are performed to investigate the degradation mechanism of D-mode MIS-HEMTs.

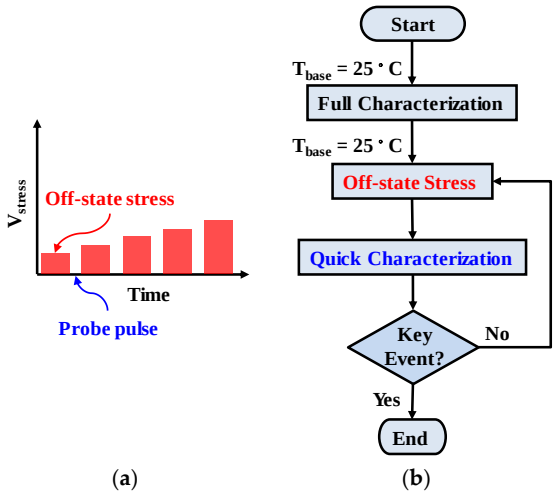

Figure 1. (**a**) Control voltages for step-stress experiments performed in this study. The device is stressed for a length of time: step-stress on gate and source (30 s) and step-stress on drain (3 min); bias is repeatedly switched to the ON-state for short intervals to evaluate the change in DC figures of merit induced by the OFF-state bias; (**b**) flow chart of a typical experiment. The device is stressed and regularly characterized in the process. The measurement loop is executed before reaching the critical voltage (key event), wherein irreversible damage to the device occurs.

Table 1. Device electrical parameters monitored during characterization.

Parameters	Definition
I_{Goff}	Gate leakage current. Measured at $V_{GS} = -20$ V and $V_{DS} = 0$ V.
I_{Doff}	Drain leakage current. Measured at $V_{GS} = -20$ V and $V_{DS} = 0$ V.
I_{Soff}	Source leakage current. Measured at $V_{GS} = -20$ V and $V_{DS} = 0$ V.
I_{G_stress}	Gate stress current. Measured at the 29th second (step-stress on gate and source) or 179th second (step-stress on drain).
I_{D_stress}	Drain stress current. Measured at the 29th second (step-stress on gate and source) or 179th second (step-stress on drain).
I_{S_stress}	Source stress current. Measured at the 29th second (step-stress on gate and source) or 179th second (step-stress on drain).
I_{Dlin}	Linear-regime drain current. Measured at $V_{GS} = 0$ V and $V_{DS} = 1$ V.
I_{Dmax}	Maximum drain current. Measured at $V_{GS} = 0$ V and $V_{DS} = 10$ V.
V_{th}	Threshold voltage. Defined as V_{GS} at $I_{DS} = 1$ mA/mm for $V_{DS} = 1$ V.
R_{on}	Device's on-resistance. Defined as the inverse of I_{Dlin}.

2. Device Structure and Experimental Setup

A schematic of the AlGaN/GaN MIS-HEMT is shown in Figure 2. This device was fabricated using a complete complementary metal oxide semiconductor (CMOS)-compatible process for GaN-based MIS-HEMTs on Silicon. The AlGaN/GaN heterostructure epilayer was grown on a silicon substrate (thickness, 900 µm) by metalorganic chemical vapour deposition (MOCVD). The epitaxial structure consisted of a 3.9 µm-thick GaN/AlGaN buffer layer, on which was deposited a 2.1 µm-thick GaN layer, a 20 nm-thick $Al_{0.23}Ga_{0.77}N$ barrier layer and, finally, a 4 nm-thick GaN capping layer.

To fabricate this device, Mesa isolation was performed with an ICP-RIE system with Cl_2 as the etching gas. Source/drain Ohmic contacts were formed with e-beam evaporation and lift-off of Ti/Al/Ni/Au (20 nm/120 nm/25 nm/100 nm) metal stack, followed by rapid thermal annealing at 800 °C in N_2 for 60 s. After removing the photoresist and carrying out a surface cleaning process to remove impurities and reduce surface dangling bonds, a 50 nm-thick Si_3N_4 film was immediately grown by plasma-enhanced chemical vapor deposition (PECVD) and deployed as the gate insulator.

The gate electrode was formed with Ni/Au (50 nm/450 nm) deposited upon the top of the dielectric stack. Finally, the device was covered with a 450 nm-thick PECVD Si_3N_4 film. The device geometry consists of L_{GD} = 16 µm, L_{GS} = 3 µm, gate length = 1 µm and gate width = 50 µm. Before starting with the step-stress experiments, the various static characteristics (Figure 3) such as I_{DS}-V_{DS}, I_{DS}-V_{GS}, G_m-V_{GS}, and leakage current for both the devices were evaluated and sorted to obtain well matched degradation characteristics; we verified that devices belonging to the same wafer presented consistent and reproducible behavior. The devices belonging to the center region of a wafer were cut out and divided into three groups (n = 10/group) for this study; a total of approximately 40 devices were tested [28].

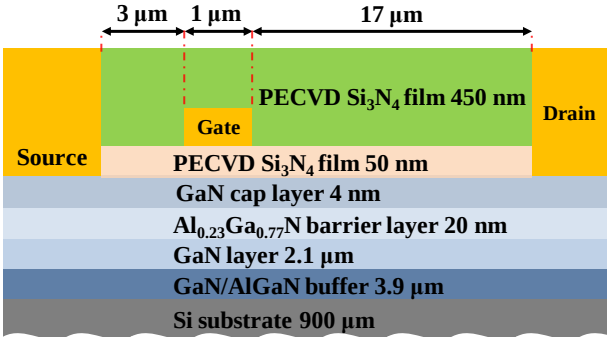

Figure 2. Schematic structure of the AlGaN/GaN high electron mobility transistors (HEMTs) grown on 4-inch Si substrate.

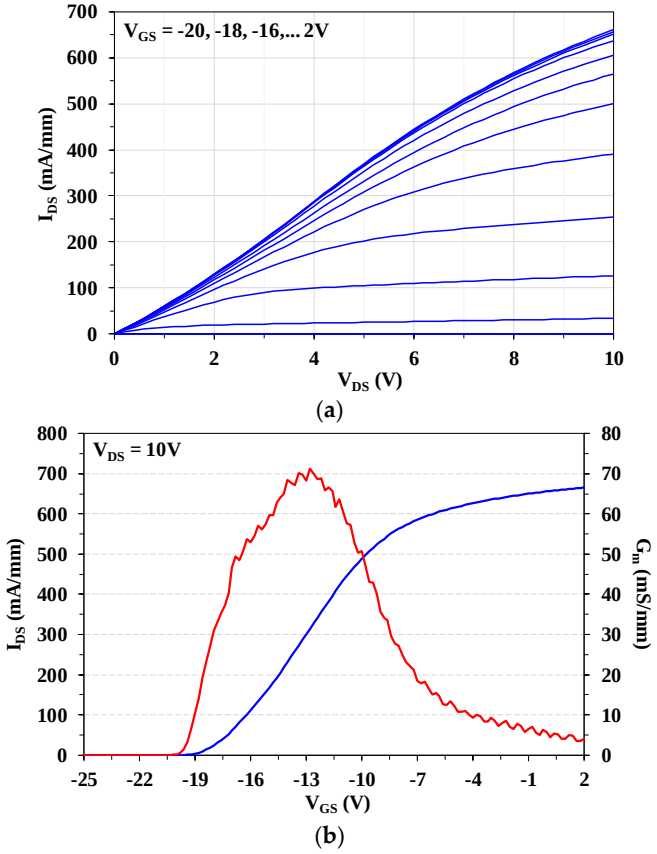

Figure 3. Representative device characteristics of AlGaN/GaN metal-insulator-semiconductor (MIS)–HEMTs used in this work. (**a**) Output characteristics (I_{DS}-V_{DS}) measured at V_{GS} from −20 to 2 V; (**b**) Transfer and transconductance characteristics (I_{DS}-V_{GS}, G_m-V_{GS}) measured at V_{DS} = 10 V.

The devices are mounted on AlN substrate (180 W/m·K) to ensure that no electrons diffuse into channels. All the experiments are performed in a probe station with a thermally controlled stage, and Fluorinert™ (FC-40) is applied on the device surface to avoid arcing and water-assisted electrochemical reactions caused by environmental conditions. For devices that are soldered into the substrate, a thin attachment layer of sintered nano-silver is applied to the bottom of the substrate to ensure that the least amount of contact resistance exists between the substrate and the lead-frame. Thermal grease is also used at the interface between the ceramic-attached lead-frame and the stage.

This study focuses on the impact of gate leakage current in reverse bias I_{Goff}, the degradation of the on-resistance R_{on}, the bias gate current I_{G_stress} obtained at the 29th second (step-stress on gate and source) or 179th second (step-stress on drain) for each stress cycle, and the shift in threshold voltage V_{th}. However, the degradation in I_{Dmax} is found to be recoverable and related to thermally-assisted electron de-trapping. This has been suggested to be resulting from the device reaching a new steady-state as trapping and de-trapping reach equilibrium. Using step-stress methods of the terminals of gate, drain and source terminal; a detailed study is performed to observe device degradation that limits safe operation in the off-state.

3. Short-Term Step-Stress Experiment

Under high reverse gate bias conditions, crystallographic defects and even cracking occur as a result of the inverse piezoelectric effect [29,30]. The presence of a strong electric field in the piezoelectric GaN and AlGaN leads to additional mechanical stress that is concentrated at the gate edge across the AlGaN barrier [31]. The change in AlGaN elastic energy can produce dislocations (extended defects). By inserting an insulator under the gate metal such as ALD Al_2O_3 and PECVD Si_3N_4, MIS-gate HEMTs are highly preferred over Schottky-gate HEMTs for high-voltage power switches. The MIS-gate structure is effective for suppressing the gate leakage current and thus improving long-term reliability. However, this MIS-gate technology still remains challenging in terms of obtaining low and stable gate leakage characteristics and achieving sufficient long-term robustness simultaneously.

To study the impact of negative gate-bias (V_{GS}) stress on the performance of Si_3N_4 gate dielectric, the device is step-stressed at V_{DS} = 0 V (shorted source and drain) with increasing values of $|V_{GS}|$ from 25 V to 135 V for harsh bias condition, as shown in Figure 4a. At each step, the device is stressed for 30 s. Since the voltage across the drain and source is constant throughout the experiment, both the drain and source sides of the gate are stressed with increasing electric fields over time.

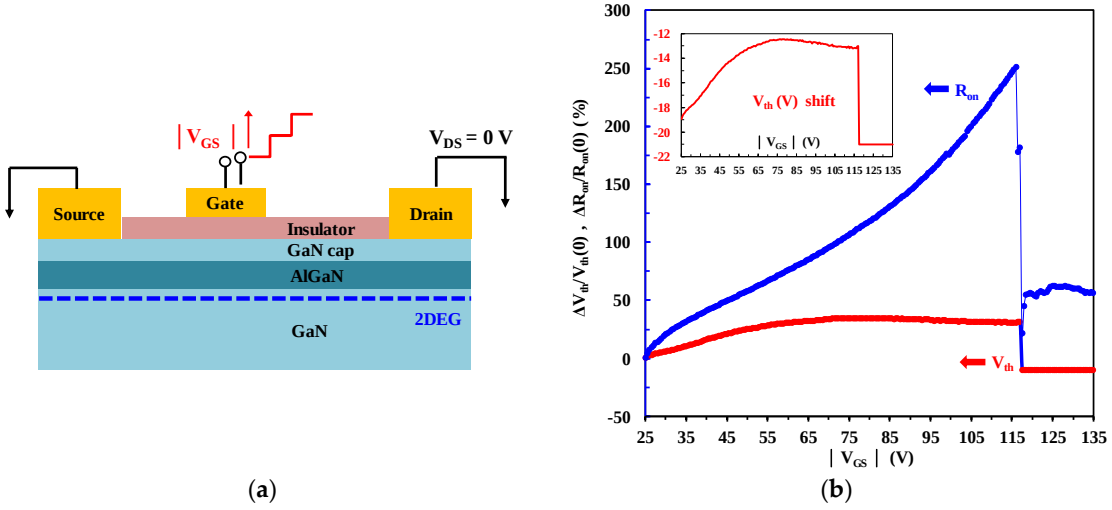

Figure 4. *Cont.*

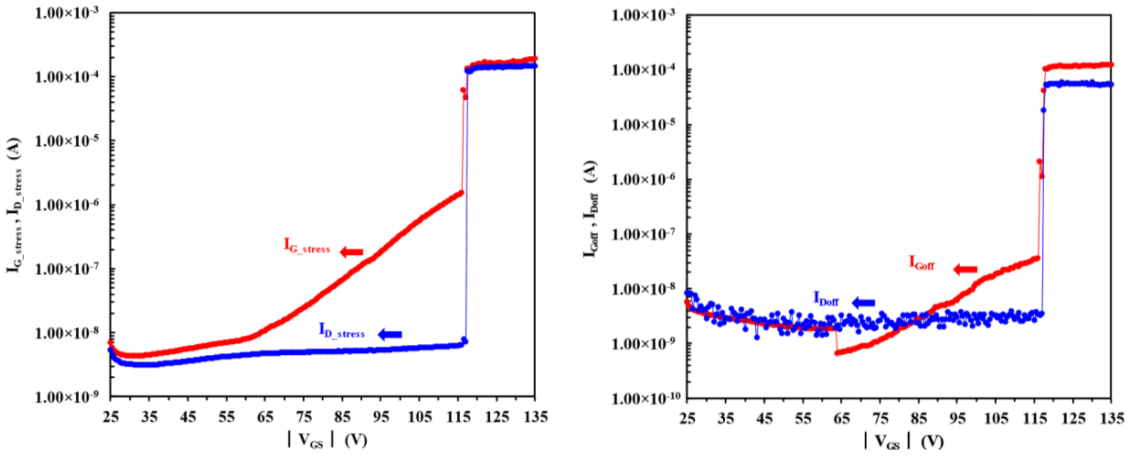

Figure 4. (**a**) Sketch of MIS-HEMT under step-stress of the gate reverse bias at V_{DS} = 0 V from $|V_{GS}|$ = 25 to 135 V in 0.5 V. A high-field appears at the gate edges on both the drain and source sides; (**b**) Electrical figures of merit as a function of $|V_{GS}|$: percent increase in dynamic R_{on} (drain current degradation) and percent positive shift in V_{th} (left scale). The inset in (**b**) depicts that a large positive V_{th} shift is induced during stress, changing it from −18.95 to −12.45 V; (**c**) 2-terminals I-V characteristics acquired during stress. A sudden increase of gate current (I_{G_stress}) is measured at $|V_{GS}|$ = 65 V; (**d**) 2-terminals leakage currents acquired after stress.

Figure 4b–d shows a positive shift in threshold voltage V_{th} (up to 30%), a corresponding increase in dynamic R_{on} (up to 200%), and an increase in gate current (I_{G_stress}, and I_{Goff}) observed in a representative sample during the step-stress experiment with V_{DS} = 0 V. Starting with the step at 116 V, a sudden increase in I_{G_stress} is observed, as well as a permanent increase in both gate currents several orders of magnitude at the end of the 118 V step (burnout failure). Gate current (I_{G_stress}) first increases, following the increase in I_{Goff}, and then increases due to the creation of gate-edge degradation. In an experiment of this kind, the evolution of I_{Goff} during stress reveals that for low values of $|V_{GS}|$, I_{Goff} tends to drop with a given stress step. This can be attributed to trapping associated with defects at the gate edges, where the electric field is highest [32]. The defects promote the injection of electrons from the gate into the Si_3N_4 insulating layer and at the Si_3N_4/GaN interface. In the degraded device where localized vertical leakage paths exist under the gate electrode, a significant number of electrons is injected from the gate electrode to the Si_3N_4 insulating layer and the insulating layer is eventually driven into breakdown (from $|V_{GS}|$ = 65 V), due to tunneling and subsequent trapping within the dielectric over layer.

It is interesting to see evidence of stress-induced gate current (I_{G_stress} and I_{Goff}) at high gate voltage and a critical gate voltage ($|V_{GS}|$ = 65 V) beyond which I_{Goff} degrades suddenly. Figure 5 shows the trapping and degradation mechanisms in GaN-Based MIS-HEMTs [33]. The injection of electrons towards the AlGaN layer under the gate electrode induces an increase in R_{on} and a positive shift in threshold voltage V_{th} until the critical voltage is reached. The accumulation of negative charge in the AlGaN layer forms a virtual gate that depletes part of the channel. During the stress period (from $|V_{GS}|$ = 25 to 65 V), ΔV_{th} increases with $|V_{GS}|$ and eventually saturates. Stressing beyond the critical gate voltage creates interface traps at the SiN/AlGaN interface in the gate-source access region, while no significant changes are observed for both drain currents (I_{Doff} and I_{D_stres}), as shown in Figure 4c,d. The injection of electrons induces an increase in R_{on} and no obvious change in threshold voltage V_{th}. These traps become a pathway for electrons to flow from the gate to the source. During stress, when electrons refill the interface traps, both I_{Goff} and I_{G_stress} sharply increase. This indicated that the traps are mainly located at the SiN/AlGaN interface.

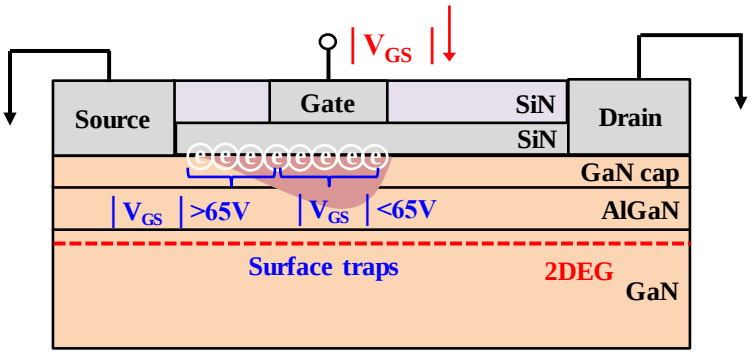

Figure 5. Schematic diagram of a device illustrates possible electron trapping that mainly depletes 2DEG in the channel under high voltage off-state gate stress and causes R_{on} degradation.

Also of interest is the fact that I_{G_stress} exhibits different degradation behavior before and after biasing to the critical gate voltage. To verify the origin of the observed degradation caused by high electric field, two possible off-state failure mechanisms are investigated. One is a vertical injection of electrons from the gate into the Si_3N_4 insulating layer, due to trap assisted tunneling, and the other is a lateral component, also due to tunneling, which involves injecting electrons directly into trap states at the SiN/AlGaN interface. The injection of electrons from the gate electrode into interface states present in the gate-source region extends laterally toward the source contact with increasing gate voltage. Degradation is detected as a non-recoverable increase in the gate current (step at $|V_{GS}|$ = 116 V and beyond). These results also indicated that electrons injected into surface states near the gate terminal form an extended virtual gate near the gate terminal edge extending the depletion region of the device channel. This is consistent with the positive V_{th} shift and corresponding increase in R_{on}.

Figure 6a shows the off-state step-stress experiments carried out under normal use conditions. Identical devices are also step-stressed at V_{GS} = −20 V (off-state) with increasing values of V_{DS} from 1 to 150 V, with a step size of 1 V (3 min at each step). To obtain enough degradation for a reasonable analysis of device reliability, limited by the instrument's capabilities (voltage rating 200 V), accelerated life testing involves applying the V_{DS} bias stress for an extended period of time (3 min). In this approach, the voltage across the gate and source (V_{GS}) is constant throughout the experiment and a high electric field peak appears at the drain side edge of the gate with the field penetrating deeply into the buffer.

Referring to Figure 6b, significant degradation takes place in V_{th} and R_{on} while a minor increase in I_{G_stress} is observed until the applied bias voltage (V_{DS}) exceeds 114 V. As the drain bias voltage (V_{DS}) increases, a significant increase of V_{th} and R_{ON} indicates that the applied electric field increases the probability for the trapped electrons both at the surface (high electric field between gate and drain) and in the buffer (high vertical field from the drain directed towards the substrate); these trap effects are due to the increased injection of electrons from the gate electrode toward the gate–drain surface (lateral trapping) and from the substrate to the buffer (vertical trapping) simultaneously [34]. In-situ passivation combined with buffer optimization is a necessary step toward the reduction of off-state stress-induced change in V_{th} and R_{ON} ratio. There is a significant degradation up to around V_{DS} = 114 V. At this critical degradation voltage, change in all figures of merit starts sharply and degradation increases as the stress experiment proceeds. Similar to a degradation mechanism in traditional Schottky gate HEMTs, a sharp increase of I_{G_stress} and I_{Goff} at a certain voltage has been observed in MIS-HEMTs.

The previous measurements were carried out starting from a negative gate voltage or from a high V_{DG} quiescent point; thus, it is possible to induce strong trapping both under the gate and in the gate-drain access region, observing the onset of electric field-induced degradation of selected DC figures of merit. Also of interest is the behavior of the GaN cascoded structure which needs to be considered during the high current turn-off condition. With this configuration, the gate-to-source

voltage of GaN MIS-HEMT is equal to the source-to-drain voltage of Si MOSFET. The interaction between the two discrete devices (Si MOSFET and GaN MIS-HEMT) may result in instability due to the unavoidable package parasitic inductance. The package influence during high current turn-off could be a significant internal parasitic ringing which may cause GaN device failure [35]. The gate isolation barrier of GaN MIS-HEMT will usually break before Si MOSFET reaches avalanche. This leads to an immediate damage of the GaN cascode. Considering the dynamic avalanche generation, the gate isolation barrier will easily break due to high voltage peaks on the GaN source-gate access region. The issue of avalanche robustness deserves special mention.

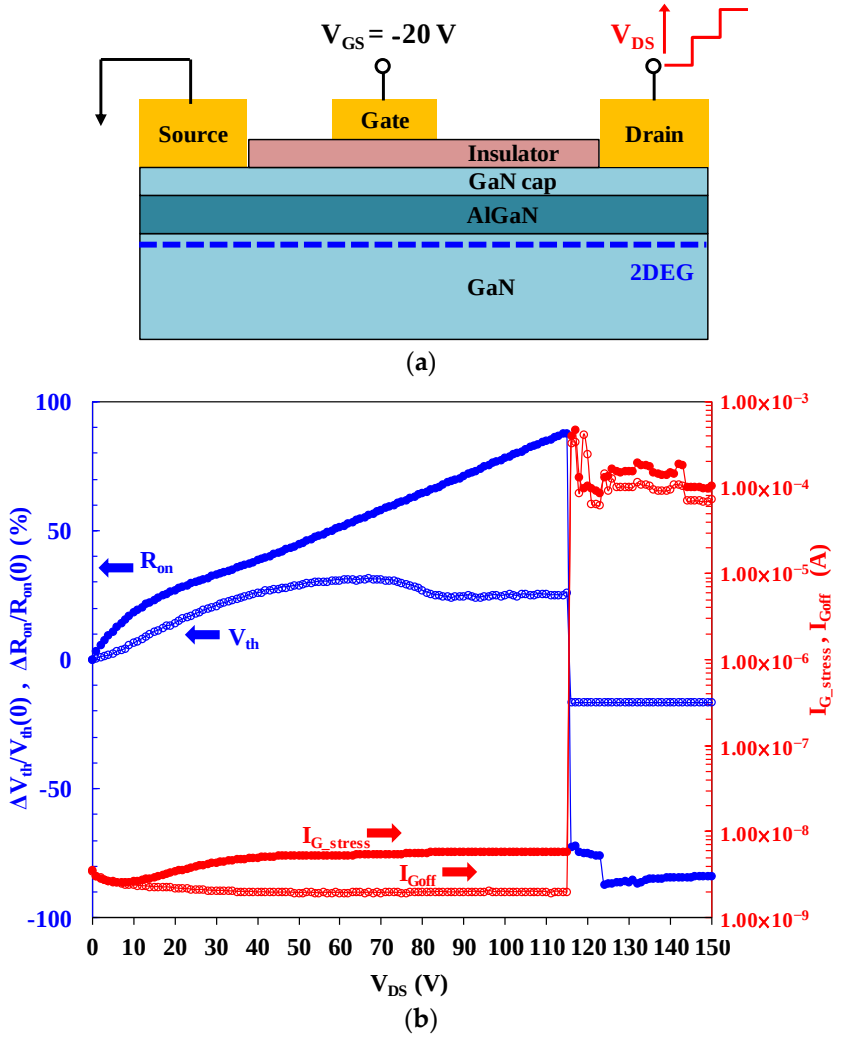

Figure 6. (**a**) Sketch of MIS-HEMT under drain voltage step-stress at off-state from V_{DS} = 1 V to 150 V in 1 V step (3 min per step). A high-field appears at the drain-side edge of the gate electrode; (**b**) Change in normalized R_{on}, V_{th}, I_{G_stress}, and I_{Goff} as a function of stress voltage. There is a negligible degradation up to around V_{DS} = 114 V. At this critical voltage, degradation in all figures of merit starts sharply and increases as the stress experiment proceeds.

In this work, a novel step-stress methodology is presented to study the potential failure mode of the cascode GaN device as shown in Figure 7a. To show that the gate degradation occurs solely in regions with high electric field, the devices are stressed by reversing the source/drain terminals. The gate terminal is grounded in this configuration. In this experiment, the V_{SG} is stepped in 0.5 V increments for 30 s per step from 22 V to 122 V while keeping V_{DG} = 20 V under pinched-off condition. In Figure 7b, failure occurred at a low voltage of 105 V. MIS devices are functional throughout the

stress. At V_{SG} = 105 V, the I_{G_stress} and I_{Goff} suddenly increase and V_{th} rapidly becomes more negative causing the device to turn-on. The V_{th} shift changes from positive to negative direction with off-state stress beyond a certain critical voltage of V_{SG} = 63 V.

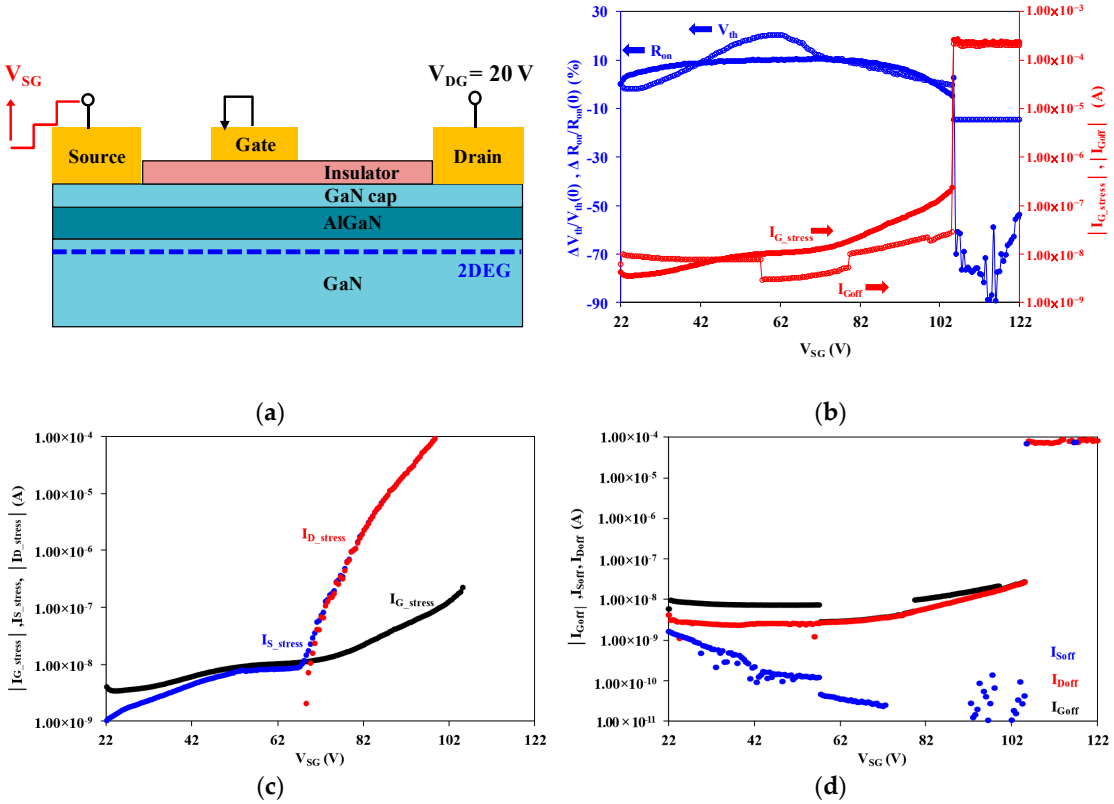

Figure 7. (**a**) Sketch of MIS-HEMTs under source voltage step-stressing at off-state from V_{SG} = 22 V to 122 V in 0.5 V step (measured at V_{DG} = 20 V); (**b**) Normalized V_{th}, R_{on} (left axis), I_{G_stress} and I_{Goff} (right axis) as a function of V_{SG} in a V_{DG} = 20 V step–stress experiment; (**c**) 3-terminals I-V characteristics acquired during stress. A sudden increase of drain (I_{D_stress}) and source (I_{S_stress}) current is measured at V_{SG} = 67 V; (**d**) 3-terminals leakage currents acquired after stress.

Figure 7c shows the degradation evolution of 3-terminal I–V characteristics of I_{D_stress}, I_{G_stress}, and I_{S_stress} during this stress experiment. It is interesting to show that both I_{D_stress} and I_{S_stress} exhibit a sharp rise around the same critical voltage denoted in Figure 7b, while I_{G_stress} presents a negligible change. This phenomenon implies that degradation takes place at dielectric/III-N barrier interface in the access region between the gate and source. Furthermore, 3-terminal I–V characteristics (I_{Doff}, I_{Goff}, and I_{Soff}), described in Figure 7d, show negligible change, which suggest SiN/AlGaN interface state generation early in the stress experiment in addition to electron trapping in the SiN passivation or the AlGaN barrier. The findings may explain by potential failure modes of the cascode GaN-based switch from internal parasitic ringing under hard-switching turn-off condition. Short-term stress is enough to produce significant structural degradation if the stress voltage (V_{SG}) is higher than the critical voltage (V_{CRI}). This reliability issue needs to be taken into consideration while D-mode MIS HEMTs are used in cascode-switch application.

4. Conclusions

Leakage-current reduction and breakdown voltage increase in GaN HEMTs are achieved by the incorporation of a suitable SiN gate dielectric layer. This paper reports on an extensive analysis of the reliability of experimental MIS-HEMTs submitted to off-state stress. A synchronized stress-characterization technique has been developed to investigate the degradation modes and

mechanisms under three off-state quiescent voltage stress conditions. Results provide information on the origin of the changes in key figures of merit occurring during stress time and on the critical stress voltage for the onset of prominent degradation, which is ascribed to a defect percolation process. The step-stress strategies provide some valuable insights for future design optimization of both depletion-mode and cascode configuration GaN-based power switches. A comprehensive investigation on the origin and underlying physical mechanisms of bulk and interface traps needs to be further carried out.

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Conflicts of Interest: The authors declare no conflict of interest.

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