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Theoretical Investigation of DIBL Characteristics for Scaled Tri-Gate InGaAs-OI n-MOSFETs Including Sensitivity to Process Variations

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ABSTRACT This paper investigates the intrinsic drain-induced barrier lowering (DIBL) characteristics of highly-scaled tri-gate n-MOSFETs with InGaAs channel based on ITRS 2021 technology node through numerical simulation corroborated with theoretical calculation. This paper indicates that, when studying short-channel effects in III-V FETs, one has to account for quantum-confinement, or else predictions will be pessimistic. Due to 2-D quantum-confinement, the DIBL of the InGaAs tri-gate devices can be significantly suppressed and be comparable to the Si counterpart. Besides, for highly-scaled InGaAs tri-gate NFETs, the impact of buried-oxide thickness on DIBL becomes minor, and the DIBL sensitivity to the fin-width and gate-length variations can also be suppressed by the quantum-confinement effect. This paper may provide insights for tri-gate device design using III-V high-mobility channel materials.

INDEX TERMS III-V channel, tri-gate MOSFET, quantum confinement, drain-induced barrier lowering (DIBL), process variation.

I. INTRODUCTION

Scaling of the supply voltage (V_{DD}) is an effective way to reduce the dynamic power for future CMOS. To attain sufficient drive current for nanoscale MOSFETs as V_{DD} scales down, high mobility III-V channel materials in particular $In_xGa_{1-x}As$ have attracted much attention [1]. However, short-channel effects (SCEs) are concerns for devices with III-V channel materials, and many studies [2]–[5] have focused on the impact of tunneling currents on III-V devices [6]–[12]. Recently, Lundstrom *et al.* [13] has concluded that the tunneling will not be an issue for InGaAs multi-gate n-MOSFETs with gate-length larger than 8 nm and effective bandgap larger than 1 eV.

Even so, nevertheless, the worsened drain-induced barrier lowering (DIBL) due to the high channel permittivity of III-V devices is still a big concern. Note that the DIBL is more than an issue regarding leakage power. It is also a performance issue. Skotnicki and Boeuf [14] has pointed out that with the same I_{ON} and I_{OFF}, the performance (e.g., inverter speed) of the technology having larger DIBL will be degraded due to the degraded effective drive current during circuit switching. In addition, the DIBL and DIBL variability also affect the stability of SRAM [15]. Therefore, for scaled InGaAs tri-gate devices, how might the quantum-confinement effect along the fin-width (W_{fin}) and fin-height (H_{fin}) directions impact the DIBL and DIBL variability is an important question and merits investigation.

In this paper, based on the ITRS 2021 spec. (with 10.4 nm gate length [1]), we examine the intrinsic DIBL characteristics for InGaAs-OI tri-gate n-MOSFETs including sensitivity to process variations through numerical simulation corroborated by theoretical calculation. This paper is organized as follows. In Section II, a quantum-mechanical subthreshold model for tri-gate devices is proposed and verified with numerical simulation. The wavefunction penetration into high-k gate-dielectric and buried-oxide (BOX) has been considered, and the impact of short-channel effects

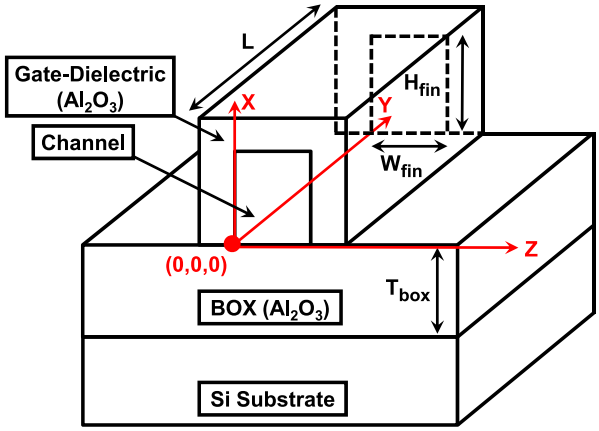

FIGURE 1. Schematic sketch of the tri-gate structure in this study. The doping concentration of the Si substrate is 1E20 cm^{-3} (p-type). The doping concentrations of source/drain and channel are 6E19 cm^{-3} and 1E17 cm^{-3}, respectively. The thicknesses of gate-dielectric for top gate and side gate are equal. Al_2O_3 is used as the high-k gate dielectric and the buried-oxide (BOX), and T_{box} denotes the BOX-thickness.

on the eigen-energy has also been included through perturbation. By using our quantum-mechanical subthreshold model together with numerical simulation, we investigate the intrinsic DIBL for highly-scaled tri-gate InGaAs-on-insulator n-MOSFETs in Section III. Benchmark with the Si counterparts has also been conducted. In Section IV, we further investigate the DIBL sensitivity to process variations for the InGaAs tri-gate devices using our scalable model. Section V draws the conclusion.

II. QUANTUM-MECHANICAL SUBTHRESHOLD MODEL

Figure 1 shows the schematic sketch of a tri-gate structure. Following the ITRS for 2021 year of production [1], III-V tri-gate devices with gate-length (L) = 10.4 nm, W_{fin} = 6.1 nm and equivalent oxide thickness (EOT) = 0.59 nm are investigated.

In our previous work [16], a subthreshold current model based on analytical solution of 3-D Poisson's equation was used to investigate the DIBL characteristics of tri-gate GeOI p-MOSFETs. However, the quantum-confinement effect was not considered in [16]. To consider the 2-D quantum-confinement effect along the W_{fin} (i.e., z) and H_{fin} (i.e., x) directions, the Schrödinger equation in the channel region can be expressed as

$$-\frac{\hbar^2}{2}\left(\frac{1}{m_x}\frac{\partial^2}{\partial x^2}+\frac{1}{m_z}\frac{\partial^2}{\partial z^2}\right)\psi_{i,j}(x,z)+E_C(x,z)\cdot\psi_{i,j}(x,z) = E_{i,j}(x,z)\cdot\psi_{i,j}(x,z) \quad (1)$$

where i and j are the principle quantum numbers for the electron quantization along the H_{fin} and W_{fin} directions, respectively. $E_{i,j}$ is the eigen-energy of the (i, j) state, $\Psi_{i,j}(x,z)$ is the corresponding wavefunction, and m_x and m_z are the channel electron quantization effective masses along the H_{fin} and W_{fin} directions, respectively. Under the assumption of flat well and the finite potential barrier height between the insulator and the channel, the eigen-energy and wavefunction can be derived [17]. The ground-state eigen-energy ($E_{0,0}$) can be expressed as

$$E_{0,0}=2\hbar^2\left(\frac{\eta_W^2}{m_z\times W_{fin}^2}+\frac{\eta_H^2}{m_x\times H_{fin}^2}\right) \quad (2)$$

where η_H and η_W can be solved from the following equations by iteration [17]:

$$\eta_W^2\left[1+\frac{m_{ox}}{m_z}\tan^2(\eta_W)\right]=\frac{m_z q V_b W_{fin}^2}{2\hbar^2} \quad (3)$$

$$\eta_H^2\left[1+\frac{m_{ox}}{m_x}\tan^2(\eta_H)\right]=\frac{m_x q V_b H_{fin}^2}{2\hbar^2} \quad (4)$$

with m_{ox} the electron effective mass inside the insulator and V_b the barrier height at the channel/insulator interface.

In addition to the structure confinement, the impact of electrical confinement also needs to be considered. A parabolic potential well along the W_{fin} and H_{fin} directions can be approximated by $E_C(x, z) = [\alpha_z(z-W_{fin}/2)^2] + (\alpha_x x^2 + \beta x + \gamma)$ with α_z, α_x, β, and γ the geometry-dependent coefficients. α_z can be derived from:

$$\alpha_z=\frac{-q}{2}\cdot\frac{\partial^2\phi_{ch}(x,y,z)}{\partial z^2}\bigg|_{(x,z)=\left(0,\frac{W_{fin}}{2}\right)} \quad (5)$$

where φ_{ch} is the channel potential solution of 3-D Poisson's equation [16] (see the Appendix). α_x, β, and γ can also be determined from the φ_{ch} at $z = W_{fin}/2$ along the H_{fin} direction. Using the perturbation theory [18] and treating the $[\alpha_z(z-W_{fin}/2)^2]+(\alpha_x x^2+\beta x+\gamma)$ terms as perturbations to the flat well, the first-order approximated ground-state eigen-energy ($E_{0,0}^1$) for a parabolic well can be expressed as

$$E_{0,0}^1 \cong E_{0,0}+\int_0^{W_{fin}}\alpha_z\left(z-W_{fin}/2\right)^2\cdot\psi_{0,0}^2(z)\,dz + \int_0^{H_{fin}}\left(\alpha_x x^2+\beta x+\gamma\right)\cdot\psi_{0,0}^2(x)dx \quad (6)$$

with $\Psi_{0,0}$ the ground-state wavefunction. Then, the electron density can be determined by the eigen-energy and wavefunction as

$$n(x,y,z)=N_{C,QM}\cdot\exp\left(-\frac{E_C-E_F}{kT}\right) \quad (7)$$

$$N_{C,QM}=\sqrt{\frac{2kT}{\pi\hbar^2}}\cdot\sum_{v,i,j}g_v\cdot\sqrt{m_d^v}\cdot\left|\psi_{v,i,j}\right|^2\times\exp\left(-\frac{E_{v,i,j}^1-E_C}{kT}\right) \quad (8)$$

with g_v the valley degeneracy and $m_d{}^v$ the density-of-states effective mass of valley v. In other words, the impact of

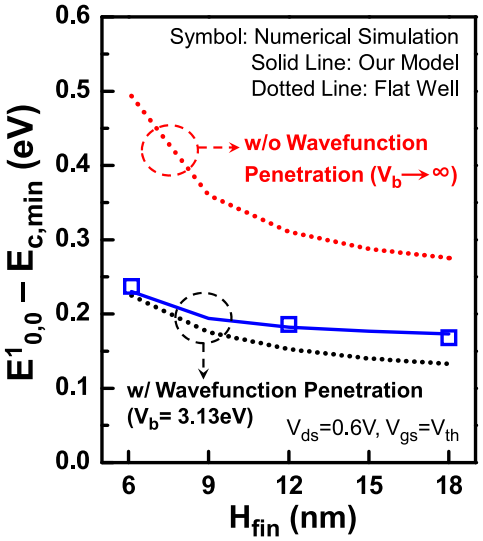

FIGURE 2. Comparison of the ground-state eigen-energy calculated from numerical simulation, our model, and flat-well approximation for InGaAs tri-gate NFETs with various fin-height (H_{fin}). V_b is the barrier height at the channel/insulator interface.

quantized eigen-energies and eigen-functions on the electron density is incorporated into the effective density-of-states for conduction band ($N_{C,QM}$) [19]. Based on the quantum correction for $N_{C,QM}$, the subthreshold drain current for each gate bias can be calculated by [16]

$$I_{ds} = \frac{q\mu_n \cdot \frac{kT}{q}\left[\frac{N_{C,QM}\cdot N_V \cdot \exp\left(\frac{-E_g}{kT}\right)}{N_{ch}}\right]\left[1-\exp\left(-\frac{qV_{ds}}{kT}\right)\right]}{\int_0^L dy / \int_0^{H_{fin}}\int_0^{W_{fin}} e^{q\phi_{ch}(x,y_{\min},z)/kT} dz dx} \quad (9)$$

where N_V is the effective density-of-states for valence band, E_g the bandgap of the channel, φ_{ch}(x, y_{min}, z) the highest potential barrier for carrier flow along the y (channel length) direction, and μ_n is the channel mobility. In Eqn. (9), $N_{C,QM}$, φ_{ch}(x, y_{min}, z), and y_{min} depend on V_{gs}.

We have verified our model using the numerical simulation that self-consistently solves the 3-D Poisson and 2-D Schrödinger equations [20]. An isotropic quantization effective mass (i.e., $m_x = m_z = 0.041m_0$) is used to assess the quantum-confinement effect along the W_{fin} and H_{fin} directions for the $In_{0.53}Ga_{0.47}As$ channel [21]. In the numerical simulation, ten subbands are included, while two subbands are considered in our analytical calculation. Fig. 2 shows the impact of wavefunction penetration on the ground-state eigen-energy of the InGaAs devices. It can be seen that after considering the wavefunction penetration, the ground-state eigen-energy substantially decreases. Fig. 2 also compares the ground-state eigen-energy calculated from numerical simulation, our model, and flat-well approximation for the tri-gate devices with various H_{fin}. It can be seen that as the H_{fin} increases, the eigen-energy obtained from numerical simulation (open square) is higher than that from the flat-well approximation (dotted line) due to the electrical-confinement effect, and our quantum-mechanical model (solid line) agrees well with the numerical simulation. Note that the short-channel effect increases as the fin-height increases, thus resulting in the more significant parabolic well and more significant electrical confinement.

In addition, Figs. 3(a)-(c) compare the subthreshold I-V for InGaAs tri-gate NFETs obtained from numerical simulation, our model, and flat-well approximation. It can be seen that while our model (solid line) shows satisfactory accuracy, the model with flat-well approximation (dotted line) cannot capture the H_{fin} dependence for the tri-gate devices with high fin aspect-ratio because it underestimates the eigen-energy. Compared with the numerical simulation, our model shows higher efficiency in determining the subthreshold current and threshold voltage of a given tri-gate device. More importantly, this theoretical framework provides more scalable results than numerical simulation does.

III. INTRINSIC DIBL OF THE InGaAs CHANNEL

By using the quantum-mechanical subthreshold model (including the wave penetration and the electrical confinement effects) together with the numerical simulation, Fig. 4(a) shows the impact of quantum-confinement on the DIBL [defined as ($V_{th}(V_{ds}$=0.05V)−$V_{th}(V_{ds}$=0.6V))/0.55V] characteristics of tri-gate NFETs with InGaAs and Si(100) [22] channel materials based on the ITRS 2021 technology node. The V_{th} is defined as the gate voltage at which the subthreshold current equals to 300nA × W_{total}/L where $W_{total} = 2H_{fin} + W_{fin}$ is the total width of the tri-gate device. It can be seen that under the classical condition, the DIBL of the InGaAs tri-gate NFETs is much worse than that of the Si counterparts. After taking into account the quantum-confinement effect, the DIBL of the InGaAs tri-gate devices can be significantly reduced and be comparable to the Si one. Under classical condition, the high channel permittivity and a positive built-in effective substrate-bias (0.3V) [23] are responsible for the large DIBL of the InGaAs tri-gate NFETs as demonstrated in Fig. 4(b). The built-in effective substrate-bias is intrinsic to the InGaAs NFETs with Si substrate. It stems from the discrepancy in the source-to-substrate work-function difference between the InGaAs and Si NFETs [23]. Both the high channel permittivity and positive built-in bias pull the carriers toward the channel/BOX interface (see Fig. 4(c)), thus degrading the DIBL. However, if the quantum-confinement is considered, the carrier centroid of the InGaAs device dramatically moves towards the channel center as shown in Fig. 4 (c). Therefore, the DIBL of the InGaAs tri-gate NFETs can be significantly improved after considering the quantum-confinement effect.

Figure 5 shows the impact of quantum-confinement on the subthreshold swing of tri-gate NFETs with InGaAs and Si channel. It can be seen that the trend is similar to the DIBL characteristics shown in Fig. 4(a).

Note that the source/drain doping concentration of III-V FETs is usually lower than the Si device (due to lower

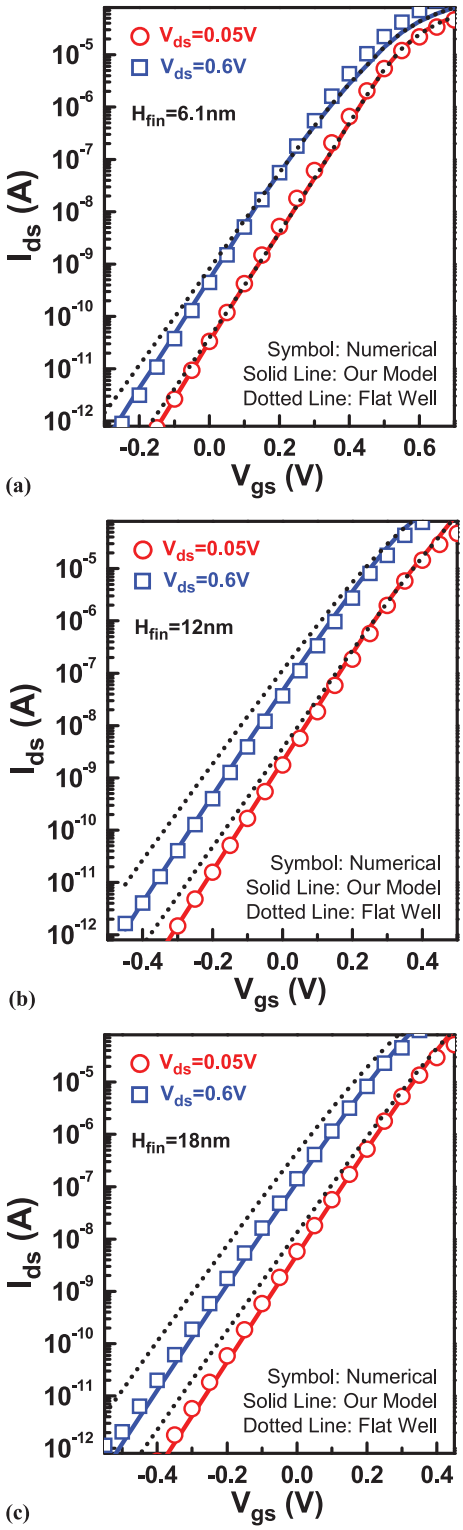

FIGURE 3. Verification of our quantum-mechanical subthreshold model for InGaAs tri-gate NFETs with (a) H_{fin} = 6.1nm, (b) H_{fin} = 12nm, and (c) H_{fin} = 18nm. The devices are designed with L = 10.4 nm, EOT = 0.59 nm, and W_{fin} = 6.1nm.

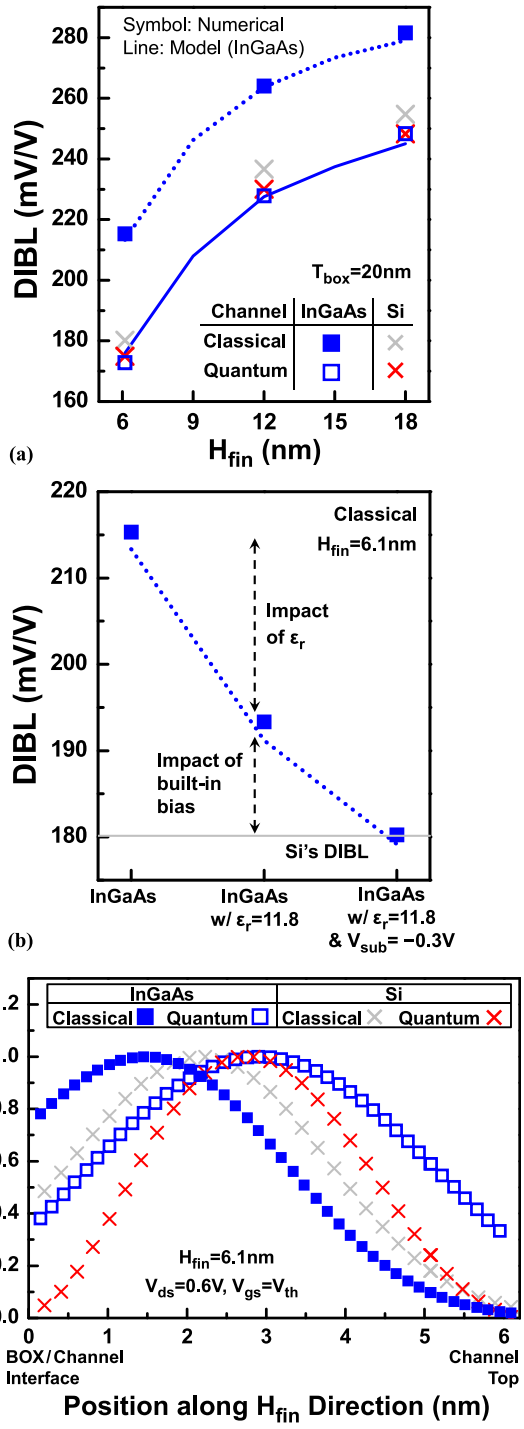

FIGURE 4. (a) Impact of quantum-confinement on the DIBL of tri-gate NFETs with InGaAs and Si channel materials. The classical model is from [16]. (b) Dissection of DIBL for the InGaAs tri-gate NFET under classical condition. (c) Comparison of the carrier profiles along the fin-height (H_{fin}) direction for InGaAs and Si tri-gate NFETs. The electron density distributions are extracted at the location where the highest potential barrier occurs along the channel-length direction and in the middle of the fin-width.

solid solubility), while DIBL has been known to increase with increasing source/drain doping concentration [24]. In this work, to compare the intrinsic DIBL between InGaAs and Si tri-gate NFETs, the doping concentration we used for the Si device is the same as that of the InGaAs device (6×19 cm^{-3}).

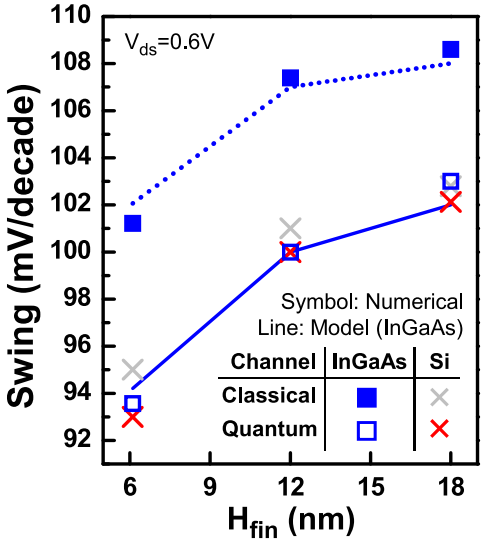

FIGURE 5. Impact of quantum-confinement on the subthreshold swing of tri-gate NFETs with InGaAs and Si channel materials.

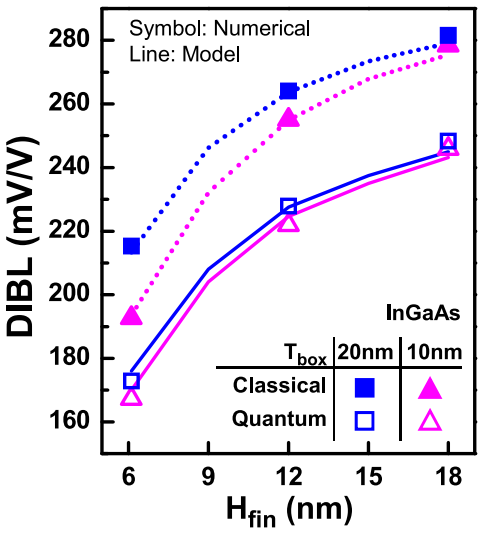

FIGURE 6. Impact of BOX-thickness (T_{box}) scaling on the DIBL characteristics of InGaAs tri-gate NFETs with and without considering the quantum-confinement effect.

IV. IMPACT OF QUANTUM-CONFINEMENT ON DIBL SENSITIVITY TO PROCESS VARIATIONS

Figure 6 shows the T_{box} dependence of DIBL characteristics for InGaAs tri-gate NFETs. It can be seen that after considering the 2-D quantum confinement, the discrepancy in DIBL between tri-gate devices with thick BOX and thin BOX is reduced. This is because under the classical condition, the carrier centroid of tri-gate devices with thick BOX is closer to the channel/BOX interface than that of the devices with thin BOX, and thus using thin BOX can significantly reduce the DIBL. Once the 2-D quantum-confinement effect is taken into account, however, the carrier centroid is almost in the middle of H_{fin} no matter what the T_{box} is. As a result, the sensitivity of DIBL to T_{box} for the InGaAs NFETs reduces.

The suppressed variation in the carrier profile due to quantum confinement may significantly impact the DIBL sensitivity to process variations for the InGaAs tri-gate devices. Fig. 7 compares the DIBL variations caused by the gate-length (L) variation between InGaAs and Si tri-gate NFETs. It can be seen that the DIBL sensitivity to L for the InGaAs tri-gate NFETs is significantly suppressed by quantum-confinement.

Figure 8(a) compares the DIBL variations due to the fin-width (W_{fin}) variation for InGaAs and Si tri-gate NFETs. It can also be seen that after considering the quantum-confinement effect, the DIBL sensitivity to W_{fin} for the InGaAs tri-gate NFETs is significantly reduced and becomes comparable to the Si counterpart. Note that while the DIBL sensitivity decreases with quantum-confinement, the V_{th} sensitivity to W_{fin} for the InGaAs tri-gate NFET is increased by quantum-confinement (Fig. 8(b)). The increased V_{th} sensitivity stems from the additional change in the effective bandgap, while the reduced DIBL sensitivity results from the suppressed variation in the carrier centroid. It can be seen from

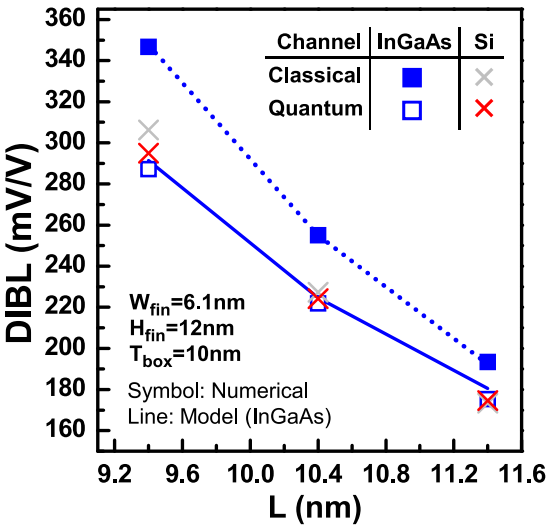

FIGURE 7. Impact of quantum-confinement on the DIBL sensitivity to gate-length (L) variations for InGaAs and Si tri-gate NFETs.

Fig. 8(c) that as the fin-width varies from 5.1 nm to 7.1 nm, classically the carrier centroid of the InGaAs tri-gate NFET shifts from 5.4 nm (the distance from the channel/BOX interface to the carrier centroid) to 4.6 nm, while quantum-mechanically the carrier centroid shifts merely from 5.8 nm to 5.65 nm, explaining the reduced DIBL sensitivity to fin-width for the InGaAs device in Fig. 8(a) after considering quantum-confinement.

Finally, it should be noted that our quantum subthreshold model does not include the direct source-drain tunneling and band-to-band tunneling currents [2]–[5], [25] that may significantly degrade the OFF-state leakage for InGaAs tri-gate devices with gate length smaller than 8 nm [13].

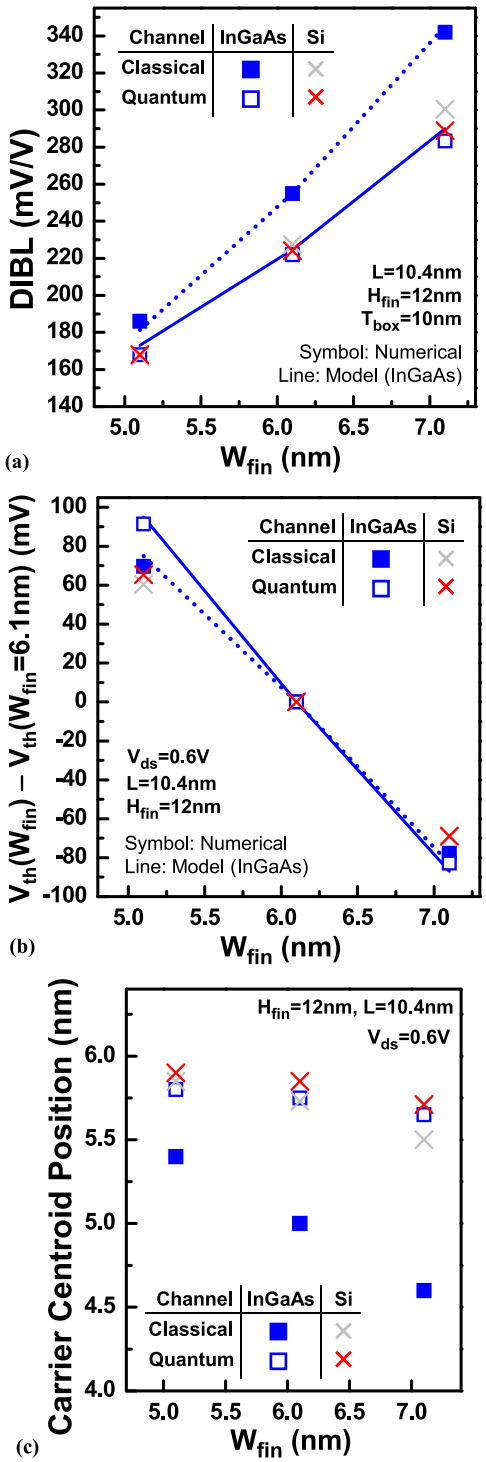

FIGURE 8. (a) Impact of quantum-confinement on the DIBL sensitivity to fin-width (W_{fin}) variations for InGaAs and Si tri-gate NFETs. (b) Impact of quantum-confinement on the threshold voltage (V_{th}) sensitivity to W_{fin} variations. (c) Reduced fin-width dependence in the carrier centroid position (the distance from the channel/BOX interface to the carrier centroid) for the InGaAs tri-gate NFETs due to quantum-confinement.

V. CONCLUSION

We have presented a quantum-mechanical subthreshold model for III-V tri-gate MOSFETs. Our theoretical model considers the parabolic potential well and wavefunction penetration through perturbation. By using our model corroborated with numerical simulation, we have investigated the intrinsic DIBL characteristics of highly-scaled tri-gate n-MOSFETs with InGaAs channel based on the ITRS 2021 technology node. We have found that, as compared with the classical model, the model including quantum-confinement predicts lower DIBL. In addition, our study indicates that, the DIBL of the InGaAs tri-gate devices can be significantly suppressed due to 2-D quantum-confinement and be comparable to the Si counterpart. Besides, with the strong 2-D quantum confinement, the impact of buried-oxide thickness on the DIBL of InGaAs tri-gate NFETs becomes minor, and the DIBL sensitivity to the fin-width and gate-length variations can also be suppressed.

APPENDIX

The channel potential distribution $\varphi_{ch}(x,y,z)$ of tri-gate MOSFET in the subthreshold regime can be obtained by solving the following 3-D Poisson's equation:

$$\frac{\partial^2\phi_{ch}(x,y,z)}{\partial x^2}+\frac{\partial^2\phi_{ch}(x,y,z)}{\partial y^2}+\frac{\partial^2\phi_{ch}(x,y,z)}{\partial z^2}=-\frac{qN_{ch}}{\varepsilon_{ch}} \tag{10}$$

where N_{ch} is the channel doping concentration, and ε_{ch} is the permittivity of the semiconductor fin. The complete channel potential solution is $\varphi_{ch}=\varphi_{ch,1}+\varphi_{ch,2}+\varphi_{ch,3}$ where $\varphi_{ch,1}$, $\varphi_{ch,2}$, and $\varphi_{ch,3}$ are solutions of the 1-D, 2-D, and 3-D sub-problems [16] in the channel, respectively. The 1-D solution can be expressed as

$$\phi_{ch,1}(x)=-\frac{qN_{ch}}{2\varepsilon_{ch}}x^2+Ax+B \tag{11}$$

The 2-D and 3-D solutions can be expressed as

$$\phi_{ch,2}(x,y)=\sum_{n=1}^{\infty}\left\{\begin{bmatrix}B_n\sinh\left(\frac{n\pi}{H_{eff}}y\right)\\+E_n\sinh\left(\frac{n\pi}{H_{eff}}(L-y)\right)\end{bmatrix}\cdot\sin\left(\frac{n\pi}{H_{eff}}x\right)\right\} \tag{12}$$

$$\begin{aligned}\phi_{ch,3}(x,y,z)=&\sum_{n=1}^{\infty}\sum_{m=1}^{\infty}\left\{\begin{matrix}\sinh\left[\sqrt{\left(\frac{n\pi}{H_{eff}}\right)^2+\left(\frac{m\pi}{L}\right)^2}\cdot z\right]\\+\sinh\left[\sqrt{\left(\frac{n\pi}{H_{eff}}\right)^2+\left(\frac{m\pi}{L}\right)^2}\cdot(W_{eff}-z)\right]\end{matrix}\right\}\\&\times B_{n,m}\sinh\left(\frac{n\pi}{H_{eff}}x\right)\cdot\sin\left(\frac{m\pi}{L}y\right)+\sum_{i=1}^{\infty}\sum_{m=1}^{\infty}H_{i,m}\\&\times\sinh\left[\sqrt{\left(\frac{i\pi}{W_{eff}}\right)^2+\left(\frac{m\pi}{L}\right)^2}(H_{eff}-x)\right]\\&\times\sin\left(\frac{i\pi}{W_{eff}}z\right)\cdot\sin\left(\frac{m\pi}{L}y\right)\end{aligned} \tag{13}$$

where

$$H_{eff} = H_{fin} + t_{ox}\frac{\varepsilon_{ch}}{\varepsilon_{ox}} \quad (14)$$

$$W_{eff} = W_{fin} + \frac{2\varepsilon_{ch}}{\varepsilon_{ox}}t_{ox} \quad (15)$$

where ε_{ox} is the permittivity of gate-dielectric, and t_{ox} the physical thicknesses of gate-dielectric. The values of A, B and series coefficients ($B_n, E_n, B_{n,m}, H_{i,m}$) can be found in [16]. Note that the channel potential depends on source/drain doping. As the source/drain doping concentration is changed, the built-in potential of the source/drain to the channel (φ_{ms}) will be changed. As a result, the boundary values of 3-D Poisson's equation and 3-D Laplace's equation are altered (see equations (2d), (2e), (4b), and (4c) in [16]), and the channel potential and carrier distribution will be affected.

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