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Fine-Feature Cu/In Interconnect Bonding Using Single Sided Heating and Chip-to-Wafer Bonding Technology

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ABSTRACT A submicron-thick Cu/In bonding by using single sided heating approach has been successfully demonstrated on chip-to-wafer-level without antioxidant metal coating. The single sided heating approach can successfully prevent oxidation of Cu metal on the wafer during bonding. As compared with double sided heating method, a lower specific contact resistance can be obtained in single sided heating method. In addition, post-bonding annealing can further improve the bonding quality. Excellent electrical performances of reliability tests show a great potential for future highly dense interconnect.

INDEX TERMS Three-dimensional integration, chip to wafer bonding, single sided heating approach.

I. INTRODUCTION

Three-dimensional (3D) integration becomes an attractive technology to overcome the bottleneck in interconnect and extend Moore's law [1]–[3]. Metal bonding plays an important role in obtaining the stacking structure with electrical interconnection. Among the different bonding technologies in 3D integration, chip-to-wafer (C2W) bonding appears to be the mainstream for the fabrication due to the consideration of yield [4]. Several approaches have been implemented in order to obtain fine-feature of metal interconnects. In Olympus research, 7.6-μm-pitch micro-bump bonding is processed under vacuum W2W tool [5]. On the other hand, Tohoku team used a unique film with Cu nano pillar (CNP) surrounded by anodized aluminum oxide (AAO) to bond together with Cu electrode, while Waseda team performed the hybrid structure using nonconductive film (NCF) [6], [7]. In the case of Zycube, the 5-μm-pitch interconnect bonding can be achieved through the C2C fabrication [8]. However, Au interconnect is required for anti-oxidation in the C2W scheme. Until now, various researches are still ongoing to realize metal interconnects with much smaller dimension. Development of metal film bonding is one of the important options [9]. In order to achieve fine-pitch metal interconnects (high dense), development of thin metal film bonding is essential.

Diffusion soldering is a well-known good option for the formation of thermally and mechanically stable bonds in stacking fabrication. Based on the consideration of metal film for C2W bonding, the bonding process should be performed at low temperature to avoid the oxidation of metal film. To achieve this goal, low-melting-point metals become potential candidates. In a previous work, Cu/In can be successfully developed at low temperature (170 °C) [10]. However, this experiment should only be performed in a vacuum environment, which is a feature of a wafer-to-wafer bonding facility.

In order to achieve successful metal film C2W bonding without antioxidant metal coating, heating approach needs to be changed. Generally, as shown in Fig. 1(a), there are two approaches for C2W bonding: double sided heating approach and single sided heating approach. For the double sided heating approach, it needs to perform double sided heating to ensure the uniformity of bonding temperature. However, this approach will induce the whole wafer to be heated causing the oxidation of metal film on the wafer. Therefore, in this letter, single sided heating approach is adopted, as shown in Fig. 1 (b). With optimized bonding parameter, the electrical

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performance is better as compared to double sided heating in C2W bonding. With the assistance of Cu/In low temperature bonding and single sided heating approach, a submicron metal C2W bonding is successfully developed.

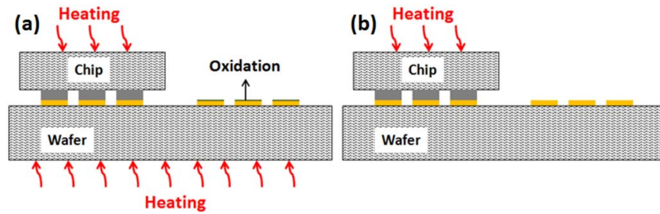


FIGURE 1. (a) Double sided heating approach, and (b) single sided heating approach.

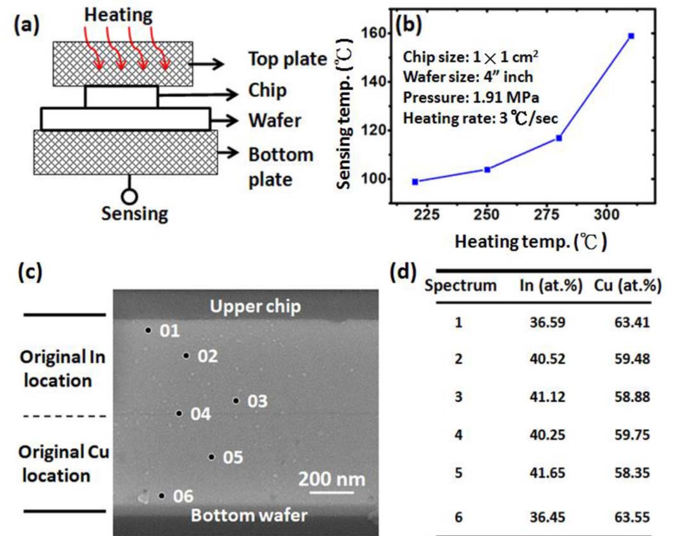
II. EVALUATION OF Cu/In BONDING AND OPTIMIZED PARAMETER

Cu/In chip to wafer bonding is performed to evaluate the effect of the heating approach in Fig. 1. Cu interconnects for bonding is prepared on one silicon wafer with 500-nm TEOS by sputtering 500-nm of Cu and 50-nm of Ti. On the other hand, Indium interconnects are prepared on one 1×1 cm^2 silicon chip with 500-nm TEOS by evaporating 500-nm of In and 50-nm of Ti. The two different interconnects are then bonded face to face at 1.91 MPa. In order to find the suitable bonding temperature for the single sided heating approach, the temperature of top/bottom plate in Fig. 2(a) is recorded, as shown in Fig. 2(b). Since both top plate and bottom plate are good thermal conductors, chip temperature and wafer temperature can be regarded as heating temperature and sensing temperature respectively.

The temperature has to be set in such that the temperature of the bonding interface is higher than 170 °C, which is the lowest bonding temperature used in double sided heating [10]. In the single sided heating approach, the setting temperature at the top plate depends on the temperature at the bonding interface, based on temperature distribution in the vertical direction. Since the thickness of chip/wafer (500 μm) is thin as compared to chip size (1 cm), the temperature distribution is described with only vertical direction. Therefore, the temperature relationship at stable state can be obtained in eq. (1)(2). Herein, $\mathbf{T_{top}}$, $\mathbf{T_{dwon}}$ and $\mathbf{T_{int}}$, are temperatures of top chip with thickness $\mathbf{t_1}$, bottom wafer with thickness $\mathbf{t_2}$ and bonding interface, respectively; $\mathbf{k_1}$ and $\mathbf{k_2}$ are thermal conductivities of top chip and bottom wafer, depending on the material used for substrates. In this study, chip and wafer are the same material with the same thickness thus eq. (2) can be written as $\mathbf{T_{int} = (T_{top} + T_{down})/2}$.

$$\frac{k_1}{k_2} = \frac{t_1}{t_2}\left|\frac{T_{\text{int}} - T_{down}}{T_{top} - T_{\text{int}}}\right| \tag{1}$$

$$T_{\text{int}} = \frac{T_{top}\frac{k_1}{k_2} + T_{down}\frac{t_1}{t_2}}{\frac{t_1}{t_2} + \frac{k_1}{k_2}} \tag{2}$$



Spectrum	In (at.%)	Cu (at.%)
1	36.59	63.41
2	40.52	59.48
3	41.12	58.88
4	40.25	59.75
5	41.65	58.35
6	36.45	63.55

FIGURE 2. (a) Schematic diagram of single side heating method in C2W bonding and its (b) relationship between heating temperature and sensing temperature. (c) Structure of Cu/In bonded interconnect by using 280 °C heating temperature and (d) its EDX analysis.

Therefore, in this study, 280 °C, which induces 117 °C at bottom plate, is chosen to obtain an average temperature of 198.5°C at the bonding interface in the single sided heating approach, as shown in Fig. 2(b). Material analysis is carried out in order to inspect the bonding feasibility. The cross sectional view of Cu/In bonding by using single sided heating approach is shown in Fig. 2(c). There is no sign of appearance of bonding interface due to the uniformity of inter-diffusion of copper and indium. According to EDX analysis, Cu and In are completely mixed and formed $Cu_{11}In_9$ phase intermetallic compounds without residual of In in the bonding region, as shown in Fig. 2(d). Therefore, the C2W bonding using 280 °C single sided heating method can achieve good metal bonding quality.

III. COMPARISON OF ELECTRICAL PERFORMANCE BY USING DIFFERENT HEATING APPROACH

Electrical performance of Cu/In interconnects with different heating methods is evaluated by Kelvin structure with 10×10 μm^2 contact area in Fig. 3(a). The bonding quality can be observed in the scanning acoustic tomography of Fig. 3(b). Fig. 3(c) shows the cross-section view of the contact area with EDX analysis. Cu and In are atoms successfully inter-diffused, and further formed $Cu_{11}In_9$ phase intermetallic compounds. This result is the same from blanked metal bonding test.

In order to identify the impact on different heating approaches, chip 1, chip 2, and chip 3 are bonded on the wafer sequentially using single and double sided heating approaches, as shown in Fig. 4(a) and Fig. 4(b). The measurement result in Fig. 4(c) and Fig. 4(d) show the first chip in C2W bonding has a specific contact resistance of $\sim 0.5 \times 10^{-8}$ Ω-cm^2 with no significant difference in

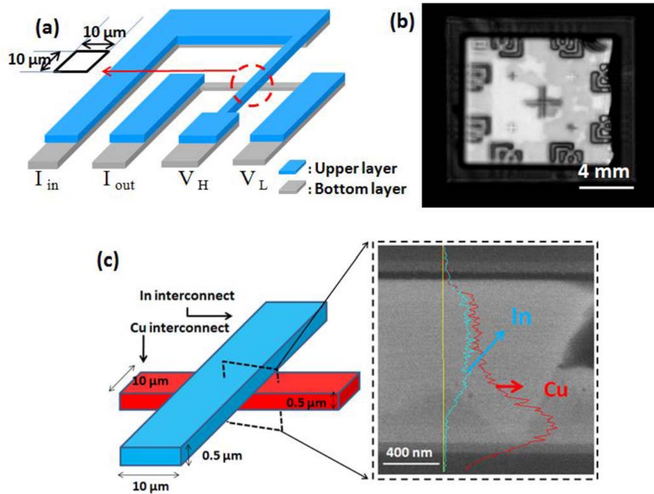


FIGURE 3. (a) Scheme of modified Kelvin structure for bonded interconnects and (b) its scanning acoustic tomography. (c) Cross-section view of bonded contact area in Kelvin structure by using single sided heating approach with its EDX analysis.

the two heating approaches. However, following bonded chips begin to have different electrical characteristic in different approach. On the side of single sided heating method, resistances of chip 2 and chip 3 have almost the same magnitude as chip 1. On the other hand, double sided heating method causes the resistance of following bonded chips to rise. As shown in Fig. 4(d), chip 2 has a specific contact resistance of $\sim 10^{-6}$ Ω-cm^2 while chip 3 has a specific contact resistance of $\sim 10^{-5}$ Ω-cm^2. It implies that the bonding quality of posterior bonded chips degrade in conventional C2W bonding with double heating approach. With the stable C2W bonding quality and excellent electrical characteristic by the usage of single sided heating approach, submicron metal bonded interconnect can be achieved.

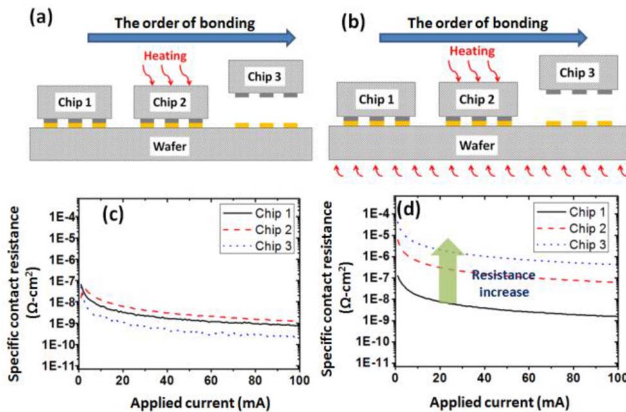


FIGURE 4. Different chips are sequentially bonded on the wafer by using (a) single sided heating approach and (b) double sided heating approach. (c) Electrical characteristic comparison of bonded Cu/In interconnects with three adjacent C2W bonding by using single heating approach at 280 °C/20 min and (d) double heating approach at 170 °C/20 min.

IV. QUALITY INVESTIGATION

In order to have high throughput, short bonding time is preferred. In this study, bonded samples using 5 min C2W bonding are fabricated and are compared with samples of 20 min C2W bonding. As shown in Fig. 5(a), although there is no resistance increment on posterior bonded chips, the average specific contact resistance in the case of 5 min is higher than the case of 20 min. The higher resistance is caused by incomplete formation of joints of full IMC [11]. To improve this situation, post-bonded annealing is applied. As shown in Fig. 5(b), the bad interconnects samples of first bonded chip (chip 1) and posterior bonded chip (chip 2 and chip 3), which has an approximate 10^{-7} Ω-cm^2 contact resistance are improved by annealing. After annealed at 170°C for 20 min, the contact resistance can be reduced to the order of 10^{-8} Ω-cm^2. Therefore, by using post-bonded annealing, single sided heating C2W bonding with 5 min bonding duration can achieve better quality.

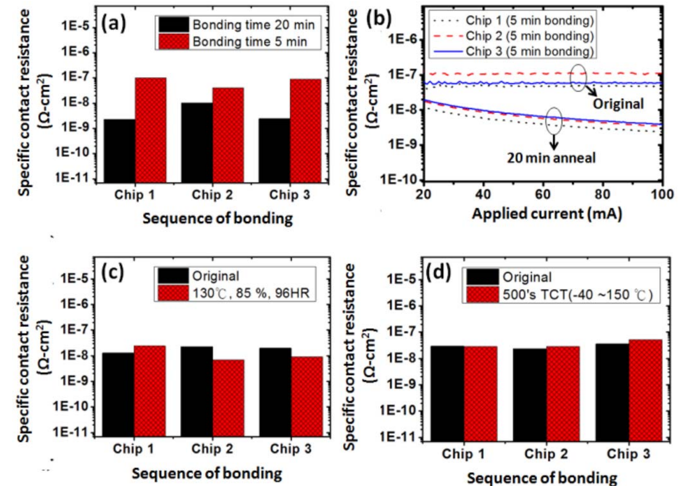


FIGURE 5. (a) Comparison of bonding time for 20 min and 5 min. (b) Improved bonded C2W by using 170°C/20min annealing; electrical performances of bonded structures after (c) humidity test and (d) thermal cycle test.

Reliability investigation of proposed method is evaluated. The bonded samples are tested with 96 hours un-biased humidity test (85 % RH, 130°C) and 500's thermal cycle test (-40°C ∼ 150°C) to investigate the feasibility of applying single sided heating approach in 3D integration. As shown in Fig. 5(c), there is no significant variation of the specific contact resistance before and after humidity test, which implies good bonding quality of Cu/In bonded interconnect against humidity and corrosion after 96 hours operation. Variation of resistance can be improved by guard ring or hybrid bonding, which can provide the protection against ambient influence. In addition, after thermal cycle test (TCT), the bonded interconnects can withstand large temperature variation without failure. There is only a slight increment in resistance after these tests, implying that interconnects

possess good durability against shrinkage and expansion, as shown in Fig. 5(d).

According to these results, submicron Cu/In bonded interconnects can be fabricated by using single sided heating and C2W bonding with post-bonded annealing. With its great electrical performance and reliability, it is competitive for 3D integration in the future.

V. CONCLUSION

In this letter, a single sided heating approach is proposed to obtain submicron bonded interconnect in C2W bonding of 3D integration. As compared to the conventional double sided heating approach, single sided heating approach can achieve 10^{-8} Ω-cm^2 specific contact resistance in a 10×10 μm^2 contact area without an increment of resistance. With the post-bonded annealing, the bonding time can be reduced while achieving high throughput and better quality. Moreover, the reliability results indicate that bonded interconnect using proposed method can endure ambient influence such as temperature variation and humidity impact. Based on experimental results, single sided heating approach can offer a good solution in future C2W interconnect bonding.

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