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Ge/IIIV fin field-effect transistor common gate process and numerical simulations

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Abstract. This study investigates the manufacturing process of thermal atomic layer deposition (ALD) and analyzes its thermal and physical mechanisms. Moreover, experimental observations and computational fluid dynamics (CFD) are both used to investigate the formation and deposition rate of a film for precisely controlling the thickness and structure of the deposited material. First, the design of the TALD system model is analyzed, and then CFD is used to simulate the optimal parameters, such as gas flow and the thermal, pressure, and concentration fields, in the manufacturing process to assist the fabrication of oxide–semiconductors and devices based on them, and to improve their characteristics. In addition, the experiment applies ALD to grow films on Ge and GaAs substrates with three-dimensional (3-D) transistors having high electric performance. The electrical analysis of dielectric properties, leakage current density, and trapped charges for the transistors is conducted by high- and low-frequency measurement instruments to determine the optimal conditions for 3-D device fabrication. It is anticipated that the competitive strength of such devices in the semiconductor industry will be enhanced by the reduction of cost and improvement of device performance through these optimizations. [DOI: 10.1117/1.JMM.16.2.024501]

Keywords: atomic layer deposition; transistors; numerical simulation; computational fluid dynamics.

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1 Introduction

The high mobility of oxide–semiconductors indicates their potential as alternatives to conventional Si-based complementary metal–oxide–semiconductor (CMOS) devices. Among them, Ge/III–V materials are important in the aggressive dimensional scaling of field-effect transistors (FETs) for use as channel materials. Recent studies suggest that high-performance Ge/III–V CMOS technology is feasible. This technology is attractive because of the intrinsic hole mobility of Ge (1900 $cm^2/V \cdot s$) and the high electron mobility of III–V materials (8500 $cm^2/V \cdot s$ for GaAs), as well as the compactness of CMOS devices [Ge-based *p*-channel and III–V *n*-channel metal–oxide–semiconductor FETs].[1,2] Subnanometer equivalent oxide thickness (EOT) gate stacks are required to maintain the intrinsically high performances of Ge and III–V elements. Research has focused on finding a suitable high-permittivity (k) dielectric ($k > 20$) to form a gate stack with a low interfacial state density and EOT. The most critical issue is the engineering of a high-quality interface between the Ge/III–V layer and the high-k dielectric, that is, the passivation of the Ge/III–V surface. An interfacial layer (IL), either intentionally or unintentionally formed during the deposition process of high-k dielectrics, is usually necessary to achieve high electrical performances in Ge and III–V element-based MOS devices, but the IL also significantly affects the desired EOT. The IL must be as thin as possible, preferably with the highest achievable permittivity.[3–6] Atomic layer deposition (ALD) is an important method for fabricating these proposed ILs, because it offers precise, monolayer-level thickness control.[7] Among the several dielectric materials approaches used to effectively passivate $In_xGa_{1-x}As$ surfaces, ultrahigh-vacuum-deposited $Ga_2O_3(Gd_2O_3)$,[8] and ALD Al_2O_3[9] have demonstrated low interfacial densities of states (D_{it}) and low electrical leakage current densities. However, other approaches using deposited Si and Ge inserted as ILs[10] between GaAs and gate dielectrics have also shown good electrical properties and device performances. For further scaling of CMOS technology, ALD-HfO_2 was recently employed to effectively passivate $In_{0.53}Ga_{0.47}As$ and to determine the energy-band parameters.[11] The threading dislocations present in the device can be guided to the edges of the active area of the transistor by elongating the misfit segments. However, the formation of defects increases the leakage current and subsequently degrades the transistor properties.[12] Although several techniques have been proposed to alleviate this problem, attempts to decrease the density of threading dislocations in Ge epitaxial layers have encountered difficulties. To further improve the properties of Al_2O_3/Ge and III–V interfaces, it is necessary to clarify the dominant factor determining the interfacial properties. Therefore, studies of the interface structures and electrical interface properties are necessary. In this study, we have investigated the correlation between the interface structures and properties. We discuss the possibility of fabricating various CMOS structures using Ge/III–V MOS capacitors with the help of computational fluid dynamics (CFD) simulations. Based on the proposed structure, a new type of

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three-dimensional (3-D) transistor with excellent gate control and electrical properties can be fabricated.

2 Experimental Methods

N-type Ge and *P*-type GaAs wafers with a (100) orientation and resistivity of 0.45 ~ Ω.cm were used in the experiments. After precleaning of the Ge and GaAs wafers by deionized water, acetone and HF aqueous solution, Al_2O_3 layers were deposited on them by the ALD method at 250°C, using Trimethyl aluminium [$Al(CH_3)_3$, TMA] and O_3 as precursors. Substantially, no GeO_2 IL exists between the germanium wafer and the phonon-screening layer. A high-K dielectric layer is located over the phonon-screening layer. A metal gate layer is located over the high-K dielectric layer. For the electrical measurements, TiN gate metal and back contact were formed by thermal evaporation to obtain the $TiN/Al_2O_3/n$-Ge and $TiN/Al_2O_3/p$-GaAs MOS capacitors. For computer-aided analysis to our experiment, the CFD software, Fluent, has been used for simulating the thermal flow field in the ALD chamber. Transient laminar flow modeled by the Navier–Stokes and energy equations was employed. The discretized equations were therefore solved by the SIMPLE algorithm with a highly accurate upwind scheme for the convective terms in the governing equations. Contours for relevant parameters are compared with experimental data to enhance the design process. The ALD CET thicknesses of the deposited Ge films were determined using transmission electron microscopy (TEM; thermal emission Schottky type, 0.5 to 30 kV). The surface compositions of the GeO_2 layers after the formation of the gate stack were analyzed using x-ray photoelectron spectroscopy (XPS; Thermo VG-Scientific). The XPS was taken on a Thermo Fisher Scientific Theta Probe photoelectron spectrometer using a monochromatic Al Ka with a photoenergy of 1486.6 eV under high-vacuum conditions. The XPS signals were calibrated on the basis of C1s (285 eV). For the fabrication of Ge gate-all-around (GAA) FinFETs, anisotropically dry etchings were performed in a transformer-coupled plasma reactor (Lam Research TCP 9600), which permitted separate control of the coil (top electrode) power and substrate (lower electrode) bias. Backside cooling using He allowed for more effective substrate temperature control. The samples were mounted on a 150-mm Si carrier wafer coated with vacuum grease before they were introduced into the etching chamber. HBr/Cl_2 plasma chemistry was used for the anisotropic etching; the process pressure was maintained at 1.33 Pa. To minimize the series resistance in electrical measurements, a $TiN/Al_2O_3/Ge/Au$ layer was deposited on the back sides of the Ge GAA FinFET as the back contact. The current–voltage ($I-V$) and capacitance–voltage ($C-V$) characteristics of the Ge GAA FinFETs were measured using Agilent 4156C and 4284A, respectively.

3 Results and Discussion

3.1 *Influence of Precursor Concentration Fraction*

The increase of the temperature accelerated the surface deposition in the ALD process. At higher temperatures, the decreased growth rate has been attributed to the enhanced desorption of the surface species.[13–15] Moreover, a temperature gradient between the walls improves the movement of gas molecules by the thermophoretic force, which generates longitudinal motions in gas molecules in dynamic processes. Figure 1 shows the numerical model for the ALD reactor with a rotating susceptor inside. In Fig. 1(a), the boundary and initial conditions for the CFD simulation are given. The precursors are input at the inlet at a constant velocity and temperature, and the outflow condition of zero property gradients is set at the outlet. The mesh system for computation is shown in Fig. 1(b); fine grids are imposed around the susceptor to depict the expected high-property gradient. Transient thermal flow fields at 0.5 s are obtained by the CFD simulation; the concentration contours of the precursors with velocity vectors are shown in Fig. 2. Figure 2(a) shows the O_3 concentration distribution at 0.5 s and the $Al(CH_3)_3$ concentration distribution is shown in Fig. 2(b). At the beginning of the reaction, the precursors are almost fully within the chamber at a low concentration at ~0.05 s. However, the precursor concentrations are increased near the susceptor surfaces at 0.5 s, as shown in Fig. 2. This quantitative model, combining surface chemistry and fluid dynamics, is informative for improving the ALD process, and is an effective replacement for massive experiment runs in production applications.

3.2 *Device Fabrication and Characterizations*

The poor native dielectric quality of Ge for gate insulators and field isolation has been a common problem that obstructs very-large-scale-integration CMOS device realization using Ge. The surface passivation of Ge has been achieved with high-permittivity (high-k) Al oxides. Al_2O_3 was deposited in a thermally enhanced ALD system at 250°C. Figure 3 shows the $C-V$ characteristics measured using different frequencies at room temperature for the $TiN/Al_2O_3/GeO_2/p$-Ge and n-Ge MOSCAP structures fabricated with ALD system. Typical $C-V$ behavior, including three distinct regions of accumulation, depletion, and inversion, is observed for all tested structures. A common feature observed in all $C-V$ curves is the "stretching out" appearing in the depletion region, which suggests that the interface traps are distributed at the interface between the dielectric film and the respective semiconductor.[13] The $C-V$ curves of the GeO_2 MOS devices have almost no frequency dispersion from 1 kHz to 1 MHz in the accumulation region at room temperature, which indicates that the bulk GeO_2 is of high quality, as shown in Fig. 3. Preliminary results for the $TiN/Al_2O_3/GeO_2/p$-Ge and n-Ge structures that underwent forming gas annealing reveal decreased EOT by a substantial decrease in the $C-V$ characteristics, indicating that ALD is a promising Al_2O_3 fabrication candidate for gate stacks.

The schematic process diagrams of $TiN/Al_2O_3/p$-GaAs and $TiN/Al_2O_3/n$-Ge (001) metal–insulator–semiconductor capacitors (MISCAPs) are shown in Fig. 4. After wet cleaning, p-GaAs and n-Ge surfaces were treated by NH_3/H_2 remote plasma treatment (RPT) prior to thermal ALD Al_2O_3 at 250°C, followed by postdeposition annealing (PDA) in forming gas (FG) at 400°C.

Figure 5 shows the $C-V$ characteristics of $TiN/Al_2O_3/n$-Ge and p-GaAs MISCAPs. To avoid the formation of unstable GeO_x layers during high-k dielectric deposition and the PDA process, nitride-based Ge_3N_4 is inserted as the IL instead of GeO_2 by a NH_3/H_2 RPT on Ge (001) and GaAs surfaces. However, the $C-V$ measurements showed

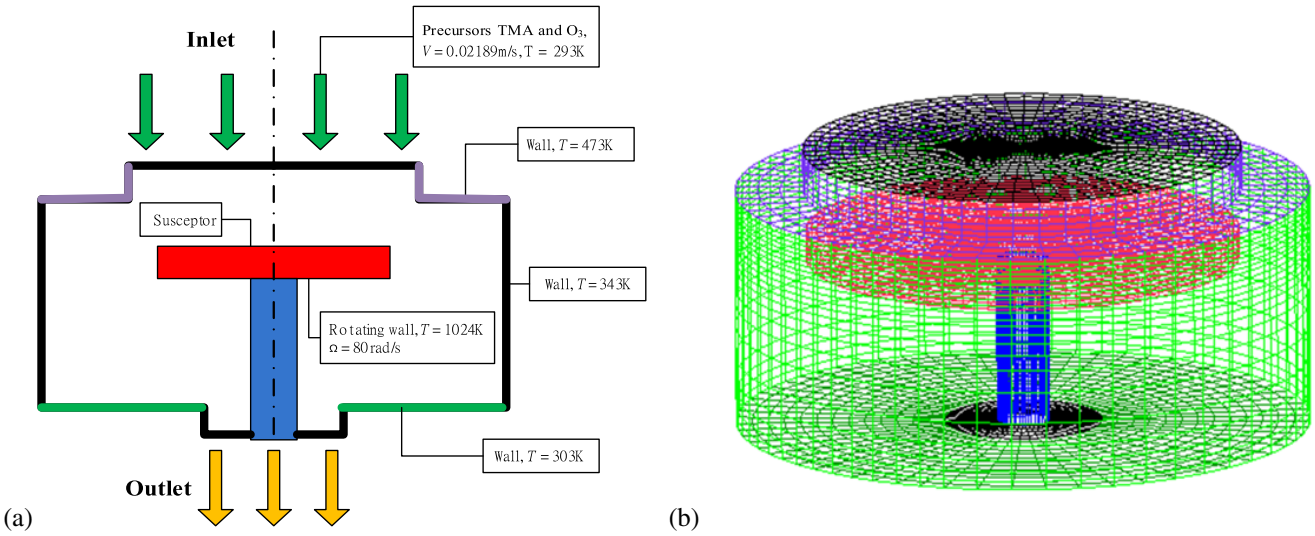

Fig. 1 Schematic of ALD system: (a) boundary and initial conditions and (b) mesh system for CFD calculation.

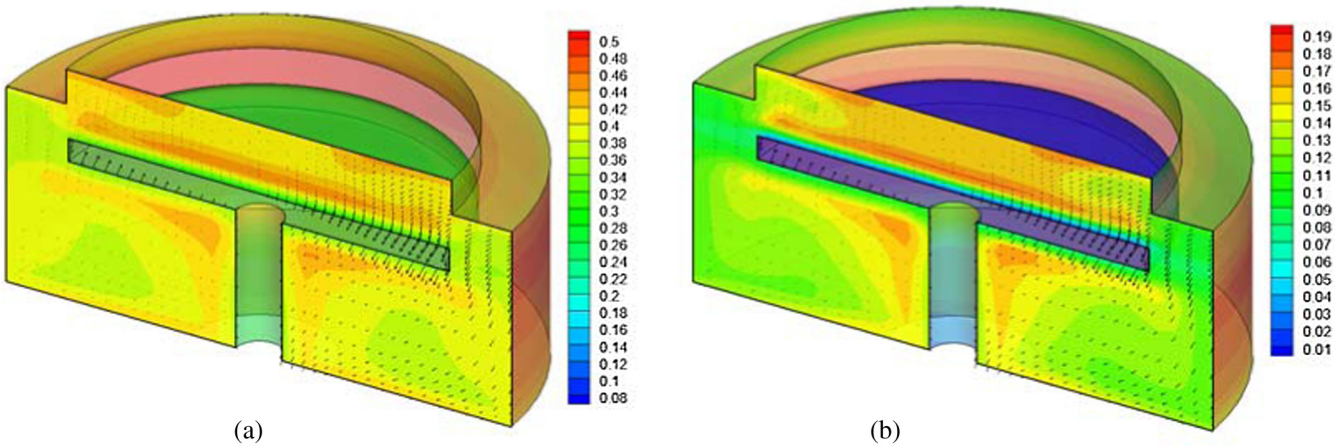

Fig. 2 Concentration plots of the concentration across the outlet of the ALD chamber for the precursor reaction. (a) O_3 concentration distribution at 0.5 s and (b) $Al(CH_3)_3$ concentration distribution at 0.5 s.

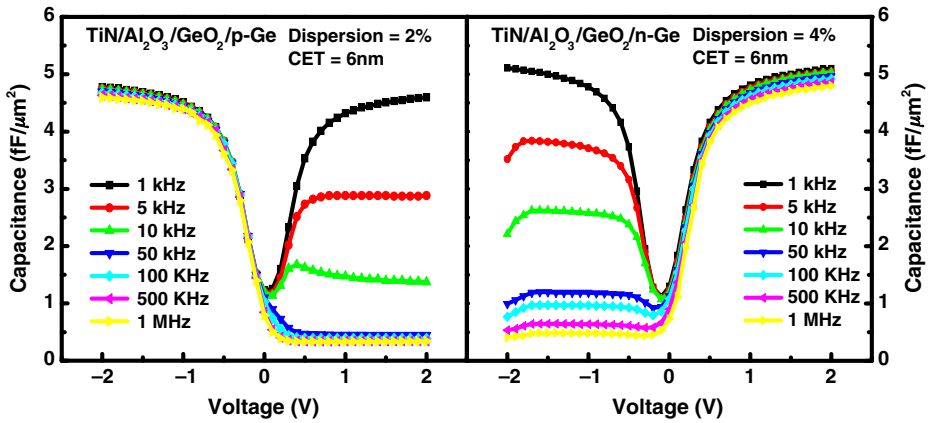

Fig. 3 $C - V$ characteristics of the $TiN/Al_2O_3/GeO_x/Ge$ MOS capacitors with p- and n-type substrates.

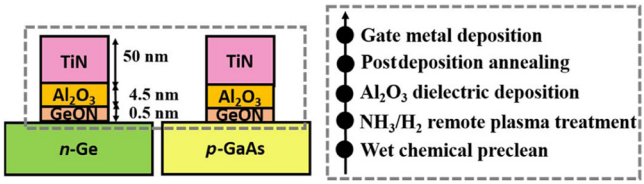

Fig. 4 Schematic common gate process for *n*-Ge and *p*-GaAs process flow of MISCAPs.

significant interface trap extraction, possibly because of metal diffusion in the *n*-Ge/*p*-GaAs and surface defects. The loss, which creates trap levels near the Al_2O_3/Ge and *p*-GaAs interface, shifts the thermal activation energy of minority carrier generation from the *n*-Ge/*p*-GaAs bandgap energy to midgap energies.

The Ge surface with rapid thermal oxidation (RTO) GeO_2 exhibits larger D_{it} than that with the nitridation pretreatment. The EOT is 3.5 nm by fitting and the D_{it} value is 1×10^{12} $cm^{-2} \cdot eV^{-1}$ measured near the midgap (see inset of Fig. 6).

The surface bonding configurations of the RTO-grown GeO_2/Ge and those after 40 cycles of RPT are examined by Ge 3-D XPS spectra (Fig. 7). The XPS curve is well resolved into two peaks, one generated from the Ge substrates at 29 eV (Ge^0) and the other from the oxide layer centered at 32 eV (Ge^{4+}), as shown in Fig. 6. For the samples with RTO on GeO_2/Ge, the spectra are deconvoluted into bulk Ge, GeO, GeON, and GeO_2 features (Fig. 7), with the binding energies reported in Ref. 16 excepting that of the GeON species. The nitrogen incorporation levels are calculated[17,18] by the intensity ratios of *N* 1 s to GeON. Notably, the intensity of oxide-related peaks decreases remarkably with respect to the Ge^0 peaks, indicating that GeO_2 consumption occurs during the RTO process and an ultrathin Ge oxynitride layer remains on the Ge surface. A possible scenario for IL reduction is suggested to be the decomposition of GeO_2 during PDA, which also promotes the different crystalline natures of Al_2O_3. As a proof-of-concept, an IL reduction sample was investigated as a dielectric material in a Ge-based FET.

Figure 8 shows a schematic of the device structure; the channel is patterned using traditional photolithography techniques. The cross-sectional TEM image clearly shows the TiN/Al_2O_3/*n*-Ge stack, with an IL composed of Al_2O_3

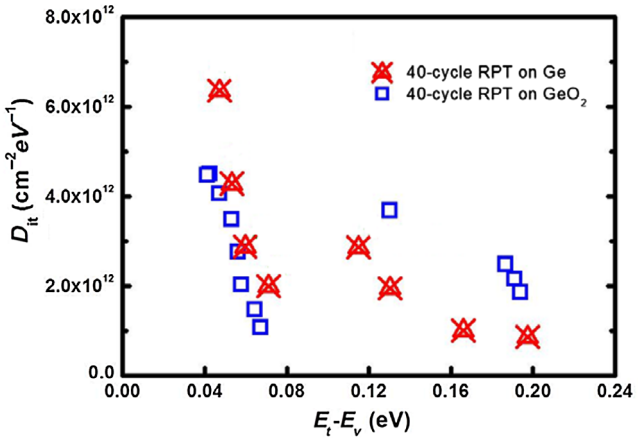

Fig. 6 D_{it} measured by the treatment cycles conductance method.

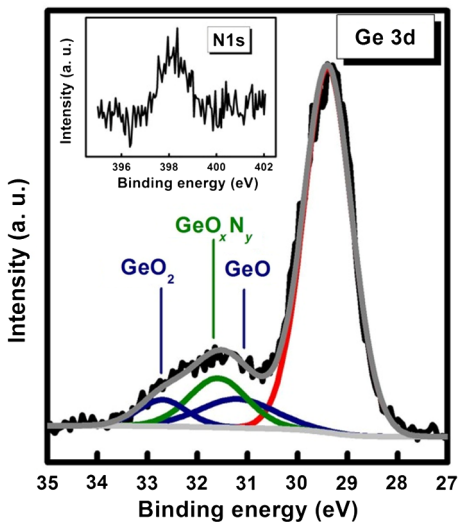

Fig. 7 XPS Ge 3-D spectra from GeO_2 grown at 550°C. Inset indicates the individual components through curve fitting of experimental results.

between the top gate (TiN) and the Ge substrate. The epitaxial Ge layers on silicon-on-insulator wafers were patterned into fins with the desired feature sizes using electron-beam lithography. The fin was formed by anisotropic plasma etching with Cl_2/HBr gas. Following Al_2O_3/TiN gate

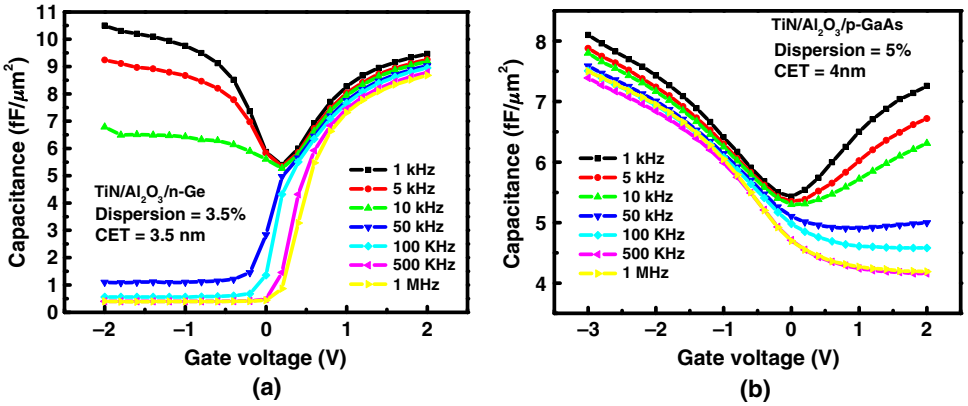

Fig. 5 *C* – *V* characteristics of the MISCAPs using (a) TiN/Al_2O_3/*n*-Ge and (b) TiN/Al_2O_3/*p*-GaAs structures.

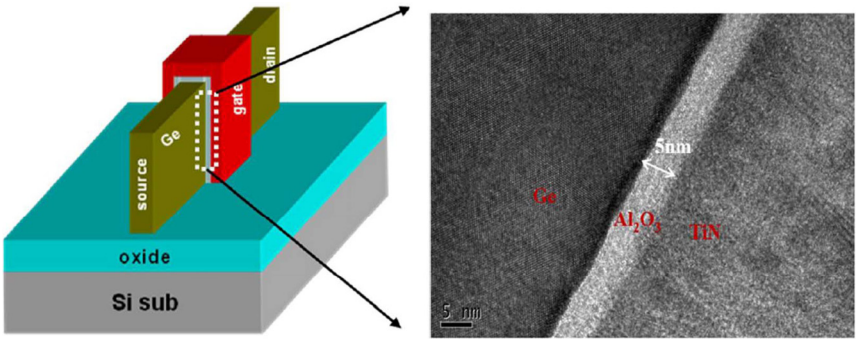

Fig. 8 TiN/Al_2O_3/*p*-Ge (001) gate stack with almost no IL.

formation, sources and drains were implanted with B (1×10^{15} cm^{-2}, 15 keV) and activated by rapid thermal annealing at 550°C for 45 s. Cross-sectional TEM images viewed along the fin width direction are shown in Fig. 9(a). The small fin width (W_{fin}) of 5.5 nm is achieved with a high etching rate of Cl_2/HBr-based plasma for the Ge devices. Due to the narrow nature of fins, the high defect bottom layer of Ge can be removed by anisotropic etching with etched rates enhanced by the defects. Herein, by making use of interfacial misfit along the epitaxial Ge on Si, a simple fabrication process to prepare high-quality and defect-free Ge GAA FETs on insulator is demonstrated.

Figure 9(b) shows the characteristics of short channel devices. The saturation current has a linear dependence with gate-source voltage. This is because the current saturates prematurely mainly due to velocity saturation. This happens because the velocity of the carriers tends to saturate due to scattering effects. Remarkably, Fig. 9(a) shows that an I_{on}/I_{off} ratio reaching $\sim 10^5$ and a subthreshold swing of 103 mV/dec are obtained for the *p*-type Ge GAA FinFET. As a result, the GAA structure is more suitable for the scaled devices. Furthermore, the drain current at $V_{GS} - V_T = V_{DS} = -1.4$ V can reach 313 μA/μm for the device [see Fig. 9(b)].

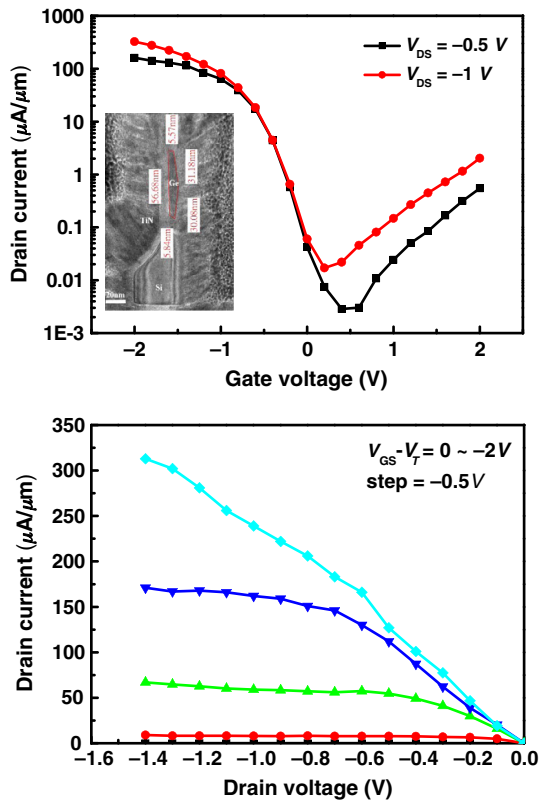

Fig. 9 (a) $I_d - V_g$ and (b) $I_d - V_d$ characteristics of the *p*-type Ge GAA FET. A saturation regime is clearly seen.

4 Conclusions

The MOS interfacial properties of Al_2O_3/Ge structures with *n*-Ge and *p*-GaAs fabricated by thermal oxidation through Al_2O_3 films were studied systematically. A GeO_x IL causes significant degradation of the MOS interface, while a small EOT remains possible with maintaining good GeO_x/Ge interface quality. These results clarified the trade-off relationship between the scaling of EOT and the MOS interfacial quality for high-*k*/Ge and III–V gate stacks employing thin GeO_x ILs. We further demonstrate an extension of eliminating the IL gate stacking process in the fabrication of Ge GAA FETs, providing a basis for future CMOS technologies.

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