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Gate-Stack Engineering for Self-Organized Ge-dot/SiO_2/SiGe-Shell MOS Capacitors

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We report the first-of-its-kind, self-organized gate-stack heterostructure of Ge-dot/SiO_2/SiGe-shell on Si fabricated in a single step through the selective oxidation of a SiGe-nanopatterned pillar over a Si_3N_4 buffer layer on a Si substrate. Process-controlled tunability of the Ge-dot size (7.5–90 nm), the SiO_2 thickness (3–4 nm), and the SiGe-shell thickness (2–15 nm) have been demonstrated, enabling a practically achievable core building block for Ge-based metal-oxide-semiconductor (MOS) devices. Detailed morphologies, structural, and electrical interfacial properties of the SiO_2/Ge-dot and SiO_2/SiGe interfaces were assessed using transmission electron microscopy, energy dispersive X-ray spectroscopy, and temperature-dependent high/low-frequency capacitance-voltage measurements. Notably, NiGe/SiO_2/SiGe and Al/SiO_2/Ge-dot/SiO_2/SiGe MOS capacitors exhibit low interface trap densities of as low as 3–5 × 10^{11} cm^{-2} eV^{-1} and fixed charge densities of 1–5 × 10^{11} cm^{-2}, suggesting good-quality SiO_2/SiGe-shell and SiO_2/Ge-dot interfaces. In addition, the advantage of having single-crystalline $Si_{1-x}Ge_x$ shell ($x > 0.5$) in a compressive stress state in our self-aligned gate-stack heterostructure has great promise for possible SiGe (or Ge) MOS nanoelectronic and nanophotonic applications.

Keywords: gate-stack, SiGe, self-organized, Ge dot, interface, size-tunable, MOS

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INTRODUCTION

Heterostructures of SiO_2/Si have been the microstructural heart of metal-oxide-semiconductor (MOS) devices that have dominated integrated circuit (IC) technology since its inception nearly 60 years ago. There are mind-boggling numbers of MOS devices in production for applications ranging from logic, memory, computing, and power devices. One of the most important applications for MOS transistors is that they are key enablers for low-power circuits that are implemented in complementary MOS (CMOS) technology. In line with the relentless miniaturization of feature sizes for MOS transistors and in order to achieve desired device performance, many types of high-mobility semiconductor channels (Heyns and Tsai, 2009; Doornbos and Passlack, 2010; Oktyabrsky et al., 2010; del Alamo, 2011; Gu et al., 2011; Gupta et al., 2011; del Alamo et al., 2013) and high-k dielectric materials (Brunco et al., 2008a; Kamata, 2008; Yu et al., 2009; Xie et al., 2012) have been proposed for the replacement of the SiO_2/Si gate stack. The inclusion of thin, strained layers of $Si_{1-x}Ge_x$ into Si CMOS technology is one of the preeminent approaches to boost the performance of MOS transistors for both cost-effectiveness and compatibility with state-of-the-art Si technology (Wu and Li, 2007;

Brunco et al., 2008a; Swaminathan et al., 2009; Toriumi et al., 2009; Yu et al., 2009; Lee et al., 2011; Nishimura et al., 2011; Zhang et al., 2012; Takenaka et al., 2013).

The production of high-quality, strained SiGe- or Ge-on-Si MOSFETs has been challenging, in particular, in situations where conventional, high-temperature thermal oxidation processes are involved. For example, during the thermal oxidation process for fabricating the conventional Ge MOSFET gate structure, the interfaces, either between Ge and Si or between Ge and the gate dielectric layers, are susceptible to defect formation (Brunco et al., 2008a; Kamata, 2008). This is because of the large lattice mismatch of 4.2% that exists between Ge and Si as well as the fact that GeO_x is both water-soluble and thermally unstable, all of which are key detriments to good device performance. To date, Ge-based pMOSFETs have been extensively studied and have demonstrated superior hole mobility over Si devices. Excellent charge transfer characteristics coupled with low D_{it} of ~1–5 × 10^{11} cm^{-2} eV^{-1} have been reported for the Ge/GeO_2 or Ge/GeO_2/high-*k* MOSFETs (Swaminathan et al., 2009; Lee et al., 2011; Nishimura et al., 2011; Zhang et al., 2012; Takenaka et al., 2013). However, these characteristics were derived after the additional expense of special interfacial treatments prior to and following gate oxidation, such as postoxidation annealing (Zhang et al., 2012; Takenaka et al., 2013), two-step oxidation (Lee et al., 2011), high-pressure oxidation (Nishimura et al., 2011), and H_2O oxidant prepulsing (Swaminathan et al., 2009). Additionally, all processing temperatures are constrained to be below 500°C in order to prevent GeO desorption that severely deteriorates the Ge/dielectric interface and the thermal stability of the Ge MOSFETs (Lee et al., 2011; Nishimura et al., 2011; Takenaka et al., 2013).

Realistically, gains made from improving individual transistors have not yet contributed to satisfactory improvement in the overall performance of ICs. This is because tight-packing and miniaturized metal wires lead to severe information latency and higher power consumption (Haurylau et al., 2007). Proposed solutions to overcome this looming interconnect crisis include replacing the long electrical interconnects with optical interconnects (Heck et al., 2011; Vlasov, 2015). Among possible semiconductor material choices for Si-based photonics, Ge is also the most promising candidate for active photonic devices on Si, thanks to its pseudo-direct gap electronic structure and compatibility with CMOS fabrication processes. Micrometer-scale-thick Ge-on-Si photonics, such as waveguide-coupled photodetectors (Liu et al., 2006; Assefa et al., 2010; Wang et al., 2011; Going et al., 2015; Sorianello et al., 2015), electro-absorption modulators (Chaisakul et al., 2012; Feng et al., 2012; Ren et al., 2012), and light sources (Liu et al., 2010, 2012; Camacho-Aguilera et al., 2012) have demonstrated their effectiveness and functionality. However, given their micrometer scales, these Ge/Si heterostructures are too thick to be directly integrated with the prevailing submicron or even nanometer-scale-thick Si electronic devices.

Recently, we have demonstrated a unique MOS gate-stack structure for Ge MOS devices consisting of a self-organized SiO_2/Ge-dot/SiO_2/SiGe-shell over the Si substrate that is achieved in a single fabrication step (Chien et al., 2011; Kuo et al., 2012, 2015; Wang et al., 2013; Chen et al., 2014; Lai et al., 2015). Our approach is primarily based on the exquisite control available through lithographic patterning combined with the selective oxidation of $Si_{1-x}Ge_x$ nano-pillars over buffer layers of Si_3N_4 deposited over the Si substrates. Remarkably, our MOS gate-stack structure is generated in a single-step process, effectively eliminating complicated microfabrication processes, such as surface treatments and cleaning prior to the deposition of dielectrics onto the Ge. Importantly, our MOS gate stack possesses good tunability for the Ge-dot size, the interfacial SiO_2 thickness, and the SiGe-shell thickness, thus providing a core building block for practical Ge-based MOS nanoelectronic and nanophotonic devices. We have also successfully exploited the use of this unique heterostructure for the production of Al/SiO_2/Ge-dot/SiO_2/SiGe floating-dot transistors with good charge retention/endurance (Lai et al., 2015) and for the fabrication of ITO/SiO_2/Ge-dot/SiO_2/SiGe MOS phototransistors with superior photoresponsivity and very low dark currents (Kuo et al., 2015). In order to further design and realize high-performance Ge MOS nanoelectronic and nanophotonic devices, it is essential to investigate the interfacial properties of the SiO_2/Ge dot and the SiO_2/SiGe shell within this gate-stack heterostructure of SiO_2/Ge-dot/SiO_2/SiGe-shell. In this paper, we have fabricated two kinds of Ge MOS capacitors: NiGe-gate/SiO_2/SiGe and Al/SiO_2/Ge-dot/SiO_2/SiGe for the characterization of interfacial properties of the SiO_2/SiGe shell and SiO_2/Ge dot, respectively.

MATERIALS AND METHODS

The fabrication of our MOS structure starts with a tri-layer, sequential low-pressure chemical vapor deposition of 25-nm-thick Si_3N_4, 70-nm-thick poly-$Si_{0.85}Ge_{0.15}$, and finally a capping layer of 5-nm-thick SiO_2 over a Si substrate. The topmost SiO_2/poly-$Si_{0.85}Ge_{0.15}$ layers are then lithographically patterned to create nano-cylindrical poly-$Si_{0.85}Ge_{0.15}$ pillars with a pillar density of 10^9 cm^{-2} over the buffer Si_3N_4 layers. Next, thermal oxidation at 900°C in an H_2O ambient for 30–80 min converts each poly-SiGe nano-pillar (30–240 nm in diameter) into single spherical Ge dots with diameters ranging from 20 to 90 nm and positioned directly below each oxidized nano-pillar (**Figures 1A–C**). It takes ~15 min to completely oxidize the SiGe nano-pillars.

For MOS capacitors (**Figure 1D**), two different device configurations of Al/SiO_2/Ge dot/SiO_2/SiGe and NiGe/SiO_2/SiGe were fabricated by mean of our self-organized fabrication process described above. Two metallization schemes for fabricating gate electrodes were employed for forming (a) Al gates and (b) NiGe gates, respectively. The former is achieved by a direct etch back of the newly formed SiO_2 layer over the Ge dots to a resulting gate oxide thickness of 15 nm, followed by the deposition of Al. The latter heterostructure is formed by the complete removal of the newly formed SiO_2 layer over the Ge dots, followed by the deposition of 60 nm Ni and subsequent rapid thermal annealing at 400°C for 1 min within a N_2 ambient (Jaeger et al., 2007; Brunco et al., 2008b). The strong intensity of Ni X-ray fluorescence within the entire dot as evidenced from cross-sectional transmission electron microscopy-energy dispersive X-ray (CTEM-EDX) line-scan examinations confirms the complete Ni germanidation of the Ge dot, as shown in **Figure 1E**. Meanwhile, a Si trench

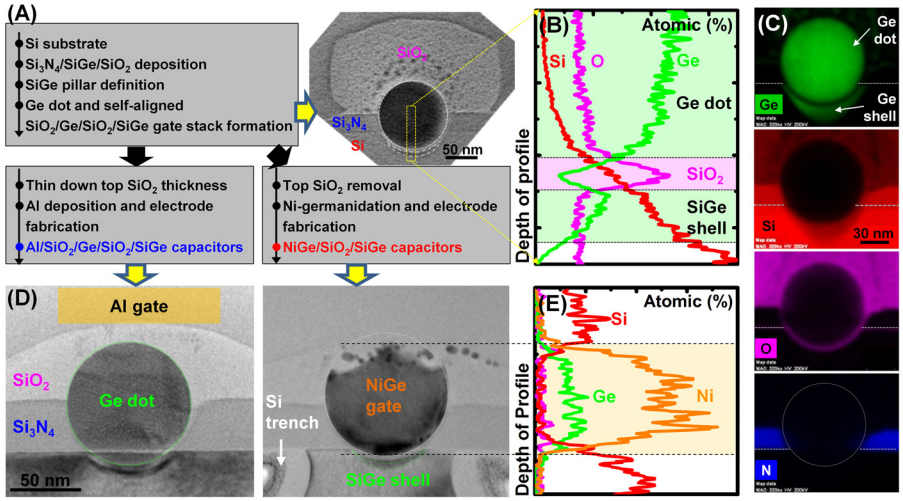

FIGURE 1 | **(A)** Schematic of the nanofabrication process, TEM images, EDX elemental X-ray **(B)** line-scan spectra and **(C)** mapping micrographs for a SiO_2/Ge-dot/SiO_2/SiGe-shell MOS heterostructure on the Si substrate. **(D)** TEM cross-sections of an Al/SiO_2/Ge-dot/SiO_2/SiGe and a NiGe/SiO_2/SiGe MOS capacitors with **(E)** corresponding EDX line-scan spectra confirming the complete Ni germanidation of the dot.

structure adjacent to the SiGe shell was designed for minimizing parasitic capacitance, as indicated in **Figure 1D**. The final process step for both MOS configurations is the fabrication of the substrate electrode on the backside of the Si substrate, followed by forming gas (95% N_2 and 5% H_2) annealing for 30 min at 400°C. Detailed characterization of interfacial morphologies and structural properties for the Ge dot/SiO_2 and the SiO_2/SiGe shell was conducted using high-resolution CTEM, EDX spectroscopy, and Raman spectroscopy. The interfacial electrical properties for the NiGe/SiO_2/SiGe and the Al/SiO_2/Ge-dot/SiO_2/SiGe MOS capacitors were determined using frequency-dependent capacitance–voltage (*C-V*) and current–voltage (*I-V*) measurements over a range of temperatures (300–77 K).

RESULTS

Our previous results (Chien et al., 2011; Kuo et al., 2012; Wang et al., 2013; Chen et al., 2014; Lai et al., 2015) have shown that thermal oxidation performed on poly-$Si_{0.85}Ge_{0.15}$ nano-pillar structures preferentially converts the Si from the poly-$Si_{0.85}Ge_{0.15}$ to SiO_2, leading to the formation of a single Ge dot within each oxidized nano-pillar through an unusual Ostwald Ripening process consolidating the segregated Ge nanocrystallites (Chien et al., 2011). Interestingly, excess thermal oxidation (or thermal annealing) of 15–65 min enables the as-formed Ge dot to penetrate the underlying, buffer Si_3N_4 layer, and ultimately form a 2–15-nm-thick $Si_{1-x}Ge_x$-shell layer ($x > 0.5$) with a "cup"-shape morphology near the top surface of the Si substrate when the Ge dot comes in close proximity to the Si substrate. Essentially, Ge atoms migrate from the dot to convert the top surface of the Si substrate to a thin $Si_{1-x}Ge_x$ shell (**Figure 1A**). Additionally, the Ge dot also catalyzes the formation of an amorphous oxide layer between the dot and the SiGe shell by oxidizing Si interstitials released by the faster oxidizing SiGe shell on the substrate. In this way, a MOS heterostructure of Ge-dot/oxide/SiGe shell is created in a single step by having a conformal interfacial gate dielectric layer around the Ge dot but also itself conformal with the SiGe shell/Si substrate (**Figure 1C**). The chemical composition of this interfacial, gate dielectric layer is confirmed by an EDX line scan to be SiO_2 instead of GeO_x as evidenced by a sharp dip in the Ge X-ray fluorescence combined with a significant increase in the Si signal (**Figure 1B**). Thus, we have a thermally stable dielectric layer of SiO_2 between the Ge dot and the SiGe shell. Simultaneously, we prevent interfacial defect issues observed in conventional Ge MOSFET structures. These defects include the loss of Ge due to miscibility in Si, the formation of electrically active dislocations, and associated point defects that are generated during the strain relaxation of the lattice mismatch between Ge and Si.

Extensive TEM observations reveal that following the thermal oxidation, 7.5–90-nm-diameter Ge dots can be controllably produced from 20 to 240-nm-diameter $Si_{0.85}Ge_{0.15}$ nano-pillars with a pillar height of 5–70 nm, as shown in **Figures 2A,B**. The Ge-dot size appears to have a strong dependence on the total Ge content within the original SiGe nano-pillar. That is, the generation of a smaller Ge dot is made possible by thermally oxidizing a smaller volume SiGe nano-pillar (**Figure 2C**). **Figure 3A** shows that the thickness of the interfacial SiO_2 layer (T_{ox}) between the Ge dot and the SiGe shell is almost constant at 3.9 ± 0.4 nm regardless of the nano-pillar (or dot) size. However, this interfacial SiO_2 layer reduces to 3.6 ± 0.4 nm in thickness by decreasing the annealing temperature to 850°C and further shrinks to 3.1 ± 0.25 nm when a poly-Si underlying layer is employed, as shown in **Figures 3B–D**. It is observed in **Figures 4A,B** that the SiGe-shell thickness (T_{shell}) and the penetration depth (D_{dot}) for Ge dots into the Si substrate also have a strong dependence on the Ge-dot sizes. Thus, we show our ability to exercise good control of the Ge-dot size, the interfacial SiO_2 thickness, and the SiGe-shell thickness in our

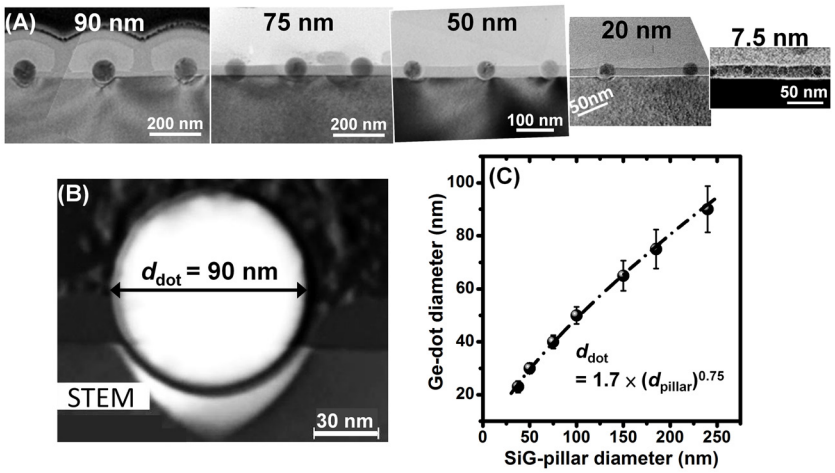

FIGURE 2 | **(A)** TEM images for SiO_2/Ge-dot/SiO_2/SiGe-shell heterostructures containing 7.5–90-nm-diameter Ge dots, produced from 20 to 240-nm-diameter $Si_{0.85}Ge_{0.15}$ nano-pillars with pillar heights of 5–70 nm. **(B)** Representative scanning TEM micrograph of a 90-nm Ge dot and the corresponding gate-stack heterostructure. **(C)** The relationship of Ge-dot diameter (d_{dot}) to the original SiGe nano-pillar diameter (d_{pillar}) with a pillar height of 70 nm prior to the oxidation.

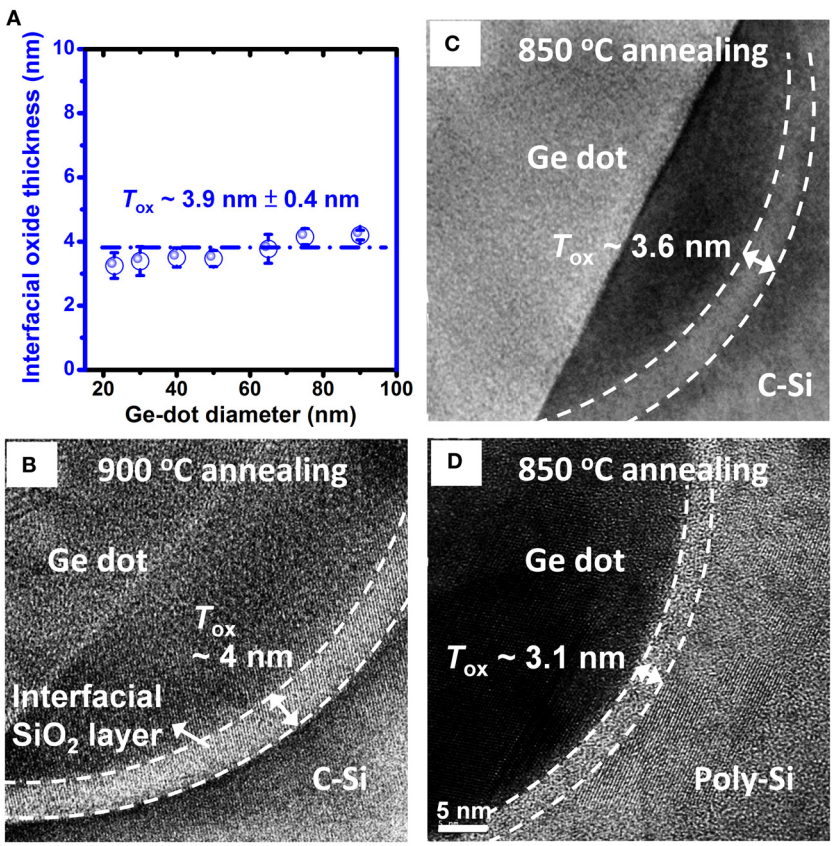

FIGURE 3 | **(A)** The interfacial SiO_2 layer has an almost constant 3.9-nm thickness regardless of the Ge-dot size. CTEM micrographs of the Ge-dot/SiO_2 and SiO_2/SiGe-shell interfaces for the proposed MOS structure fabricated on a Si substrate following thermal annealing at **(B)** 900°C and **(C)** 850°C. **(D)** The interfacial oxide thickness is smaller, i.e., ~3 nm for the case of our MOS structure nanofabricated over poly-Si and annealed at 850°C.

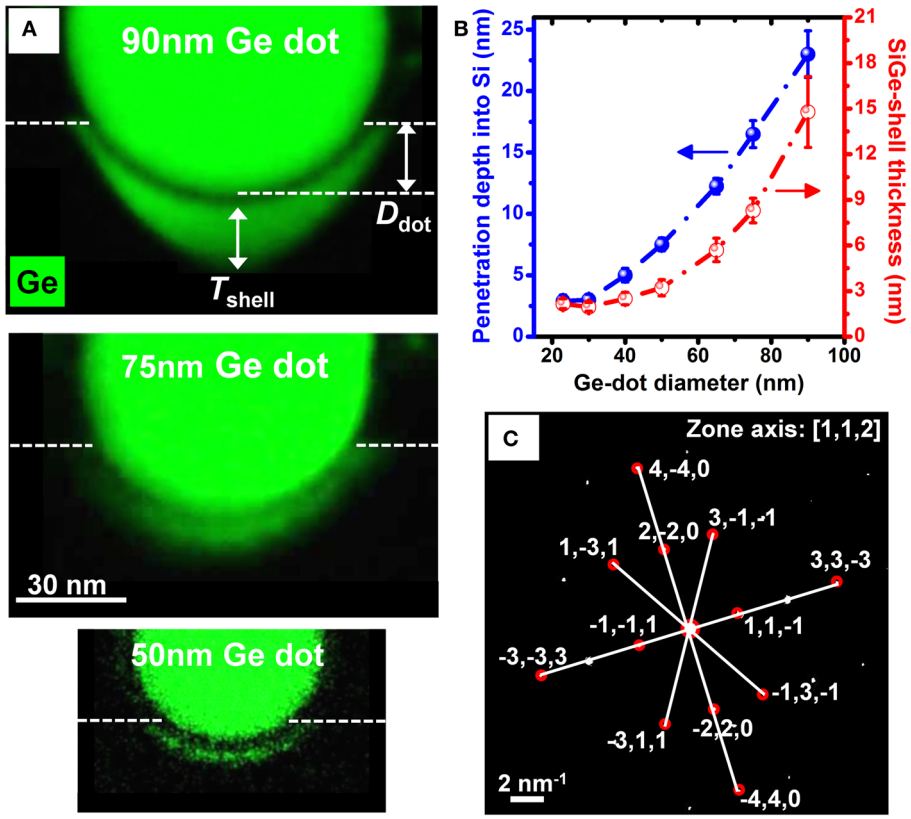

FIGURE 4 | **(A)** EDX elemental X-ray mapping micrographs for the SiGe shells generated by 90, 75, and 50-nm-diameter Ge dots, respectively. **(B)** Penetration depth of the Ge dot into Si (D_{dot}) and SiGe-shell thickness (T_{shell}) as a function of the Ge-dot diameter. **(C)** Selected area diffraction pattern of a SiGe shell in **(A)** confirms its good crystallinity and its state of compressive strain.

MOS heterostructure, thereby providing a core building block for Ge-based MOS devices. Moreover, the clear lattice fringes observed in the high-resolution TEM micrographs and the sharp, lattice-plane spots in the SiGe selected area diffraction patterns (SADs) in **Figure 4C** confirms the excellent crystallinity of the SiGe shell. Detailed analysis of the SADs give the average lattice spacings of the {110}, {111}, and {311} SiGe planes as 3.928, 3.216, and 1.657 Å, corresponding to residual compressive strains of −1.60, −1, and −2.64%, respectively. Our previous work (Pezzoli et al., 2008; Liao et al., 2014) on the Raman characterization of the SiGe-shell region has also shown that Ge mole fractions as high as $x = 0.55$–0.72 are achieved for the SiGe shells formed from 50 to 90 nm Ge dots. The advantage of having single-crystalline $Si_{1-x}Ge_x$ shells ($x > 0.5$) in a compressive stress state has extensive applications in nanoelectronics and nanophotonics, especially in SiGe (or Ge) p-MOS devices.

Figure 5A shows the high-/low-frequency C–V characteristics of NiGe/SiO_2/SiGe and Al-gate/SiO_2/Ge-dot/SiO_2 MOS capacitors measured at 77–300 K. Both devices exhibit good gate bias control of the surface charge and minority carriers at 100 Hz–1 MHz. The measured gate dielectric capacitances (C_{ox}) in the accumulation region are 8–8.8 and 5–5.5 pF, respectively, for NiGe/SiO_2/SiGe and Al-gate/SiO_2/Ge-dot/SiO_2 capacitors. These measurements are in reasonable agreement with the theoretically calculated values of ~8.7 and 5.9 pF based on the dielectric layer thicknesses, dielectric constants, and gate areas. From the extensive, variable temperature high-/low-frequency C–V characteristics, the extracted D_{it} values show a typical U-shaped distribution profile across the energy band gap with minimum D_{it} of ~4.5×10^{11} and ~3×10^{11} $cm^{-2}{\cdot}eV^{-1}$, respectively, for NiGe/SiO_2/SiGe and Al-gate/SiO_2/Ge-dot/SiO_2 MOS capacitors, as shown in **Figure 5B**. A significantly large negative flat-band voltage (V_{fb}) is observed for both NiGe/SiO_2/SiGe and Al-gate/SiO_2/Ge-dot/SiO_2 MOS capacitors, suggesting the presence of positive fixed charges. The measured interface trap densities and fixed charge densities are comparable to the reported values (10^{11}–10^{12} cm^{-2}) of state-of-the-art Ge MOS capacitors (Lee et al., 2011; Xie et al., 2012), suggesting that good-quality interface properties are achievable for our fabricated MOS gate-stack structures. **Figure 5C** contains the I–V characteristics of NiGe/SiO_2/SiGe capacitors, showing the typical features of direct tunneling, Fowler–Nordheim tunneling, and hard breakdown, as indicated by regions I, II, and III, respectively. A low leakage current density of about 10^{-9} A/cm^2 and a high breakdown electric field (E field) of 8.3 MV/cm further confirm the electrical robustness of the 3.9-nm-thick interfacial SiO_2 layer.

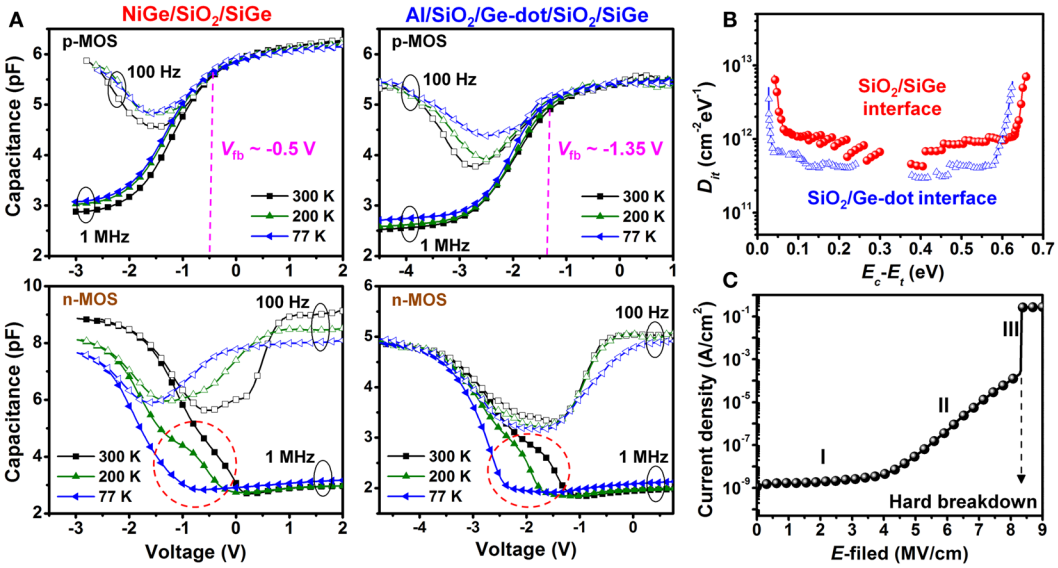

FIGURE 5 | **(A)** Frequency-dependent *C–V* characteristics and **(B)** extracted D_{it} for NiGe/SiO_2/SiGe and Al/SiO_2/Ge-dot/SiO_2/SiGe capacitors in the temperature range of 300–77 K. Red dashed circles indicate weak-inversion humps because of the faster capture and emission of carriers within the small bandgap of Ge. **(C)** *I–V* behavior of NiGe/SiO_2/SiGe capacitors confirms the robustness and integrity of interfacial oxide layer.

DISCUSSION

We have clearly demonstrated that our proposed MOS gate-stack structure is not only formed in a self-organized manner but also possesses excellent, process-controllable, size tunability. For Ge MOS transistor applications, the gate geometry or channel length (L_g) of the MOS structure is directly dependent on the diameter of the Ge dot (d_{dot}). As mentioned above, d_{dot} is essentially determined by the total Ge content within the original $Si_{1-x}Ge_x$ nano-pillar and therefore, lithographically controllable *via* the geometrical dimensions (diameter: d_{pillar} and height) and the composition of the original $Si_{1-x}Ge_x$ nano-pillar prior to oxidation. For $Si_{0.85}Ge_{0.15}$ nano-pillars with a pillar height of 70 nm, the relationship between the experimentally produced Ge-dot size and the original $Si_{0.85}Ge_{0.15}$ nano-pillar diameter is well described by $d_{dot} = 1.7 \times (d_{pillar})^{0.75}$ (**Figure 2C**), indicating good mass conservation of the Ge content prior to and following the thermal oxidation. This experimental fact demonstrates that as compared to the direct fabrication of nano-channels in bottom-up methods for conventional MOSFETs, our approach lends itself to simplified process control. Only the geometry of the original SiGe need be controlled in order to generate the desired MOS geometry *via* nano-patterning steps.

As regards the interfacial oxide layer separating the Ge dot and the SiGe shell/Si substrate, its thermal stability, gate oxide integrity, and thickness scalability determine the performance of our Ge MOS devices. Our previously reports (Kuo et al., 2012; Chen et al., 2014; Lai et al., 2015) have described that the interfacial SiO_2 thickness is determined by an exquisitely controlled dynamic balance that exists between the fluxes of oxygen and Si interstitials. Thus, judicial control of either the source of Si interstitials or the flux of oxygen interstitials by changing thermal annealing conditions during the penetration of Ge dot effectively controls the interfacial SiO_2 thickness. The shrinkage of the interfacial SiO_2 layer in thickness is enabled by either decreasing the annealing temperature to 850°C or by employing a poly-Si underlying layer (**Figures 3B–D**), demonstrating, once again, that the interfacial layers within our MOS heterostructure are individually tunable. We believe that with further optimization of substrate and thermal annealing parameters, the interfacial SiO_2 thickness could be made even smaller, i.e., below 1 nm, if needed for advanced Ge MOS applications. Additionally, the presence of a robust, thermally stable SiO_2 interfacial layer completely obviates GeO desorption issues experienced by previous workers. As described previously, GeO desorption has a severe and detrimental impact on the Ge/dielectric interface and consequently the thermal stability of Ge MOS devices during sequential high-temperature processes (Toriumi et al., 2009; Lee et al., 2011). In contrast, our Ge-MOS oxide stability is evidenced by the abrupt interfacial boundaries and an absence of structural defects. Also, and importantly, such an amorphous SiO_2 interfacial layer effectively decouples the lattice-mismatch constraints between the Ge dot and the Si substrate. The absence of lattice mismatch generated defects, such as dislocations and point defects, is particularly beneficial for the production of Ge-on-Si photonic devices. Hence, our MOS heterostructure and associated processing eliminate not only the stringent limitations on the thermal budget for processing conventional Ge MOS structures but also the complicated surface cleaning and interfacial treatments that are needed prior to and following the deposition of each layer within the conventional Ge MOS gate stack.

Good process control of the composition, thickness, and crystallinity of the SiGe channel is essential for the application of our $Si_{1-x}Ge_x$ shell as a high-mobility channel material in

nanoelectronics. Our SiGe shell is generated by the substitutional diffusion of Ge within the Si substrate. Thus, since the Ge dot is a sufficiently large source of Ge atoms, the thickness and chemical composition of the SiGe shell are mainly determined by the diffusion coefficient of Ge in Si, the oxidation temperature and time, and the Ge-dot size. **Figures 4A,B** do indeed show a strong dependence the SiGe-shell thickness on the Ge-dot size. The estimated diffusion lengths for Ge in Si at a temperature of 900°C and for diffusion times of 15–65 min are 1.5–2.4 nm, respectively, based on the diffusion coefficient equation of $D_{Ge\ in\ Si} = 1.03 \times 10^5 \cdot \exp(-5.33/k_BT)$ (Fahey et al., 1989; Silvestri et al., 2006), where k_BT represents the thermal energy, in our case, at 900°C. The theoretically calculated values are in reasonable agreement with the observed thicknesses of 2–3 nm for the SiGe shells formed from the 20–50 nm Ge dots, but they are too small to explain SiGe-shell thicknesses of 6–15 nm when the Ge dot increases to 50–90 nm in diameter. We have experimentally determined that the formation of substantially thicker SiGe shells is associated with these larger Ge dots catalytically enhancing the release of Si interstitials from the Si substrate. Therefore, for the case of larger Ge dots, interstitial generation significantly increases Si vacancy concentrations and consequently enhances Ge diffusion lengths. Increased catalytic generation of Si interstitials is also clearly evidenced by the enhanced penetration depth for Ge dots into the Si substrate with increasing the dot size, as shown in **Figures 4A,B**. In summary, the thicker $Si_{1-x}Ge_x$ shells resulting from the larger Ge dots have shown us that Ge diffusion lengths in Si calculated using conventional formulas may have to be revised in light of the observed Ge-catalyzed Si vacancy enhancement. In addition to excellent crystallinity confirmed by the clear lattice fringes observed in the high-resolution TEM micrographs and SADs, our previous work (Liao et al., 2014) on the Raman characterization of the SiGe-shell region has shown a large blue shift of the longitudinal optical Ge–Ge phonon line (309 cm^{-1} from the SiGe shell as opposed to the 301 cm^{-1} for bulk Ge). This blue shift suggests the SiGe shell is being subjected to a compressive strain of ~1.6% and is therefore in reasonable agreement with the SAD analysis from **Figure 4C**. Also, the appearance of a weak Raman signal at 406–414 cm^{-1} suggests that the chemical composition of the $Si_{1-x}Ge_x$ shell has a strong dependence on the dot size. The Ge mole fraction is as high as $x = 0.55$–0.72 for the SiGe shells formed from 50 to 90 nm Ge dots (Pezzoli et al., 2008; Liao et al., 2014).

As described above, the thickness of the SiGe shell is tunable simply by controlling the flux of Ge atoms leaving the dots to form the SiGe shells on the surface of the Si substrate. It is indeed interesting to note that a corresponding SiGe shell is not discernible on the surface of the Ge dot in spite of the fact that dissolution of Ge in Si actually requires a larger enthalpy (38.4 kJ/mole) than for Si to dissolve in Ge (30.7 kJ/mole) (Harrison and Kraut, 1988). The absence of the SiGe shell in the Ge dot could be attributable to the rapid migration of Si interstitials over the surface of the Ge dot enroute to their oxidation at the distal surface of the dot. Thus, even if Si is fully soluble in Ge, the chemical gradient created by the high temperature oxidation process acts as a "sink" for Si interstitials. Experimentally, we have shown that the Si X-ray fluorescence signal is undetectable within the Ge dots in **Figures 1B,C**.

A MOS capacitor is the basic, effective core device for qualifying the integrity of a novel gate-stack structure. In particular, the electrical properties of the interface between the inversion layer and gate dielectric layers can be exquisitely characterized using an MOS device. In our particular case, there are two interfaces of interest, namely the SiO_2/Ge-dot and the SiO_2/SiGe-shell interfaces. These interfaces are in series for our self-organized SiO_2/Ge-dot/SiO_2/SiGe heterostructure. In order to fully exploit the electrical interfacial properties of our MOS gate-stack heterostructures, we fabricated both NiGe-dot/SiO_2/SiGe and Al/SiO_2/Ge-dot/SiO_2/SiGe MOS capacitors and then characterized the interfaces of the SiO_2/SiGe shell and the SiO_2/Ge dot, respectively, for both device types. Both MOS capacitors of the NiGe/SiO_2/SiGe and the Al/SiO_2/Ge-dot/SiO_2/SiGe types feature interface trap densities of as low as 3–5×10^{11} $cm^{-2} \cdot eV^{-1}$ (**Figures 5A,B**) and which are insensitive to the dot (nano-pillar) density and to the gate areas. The measured low D_{it} for NiGe/SiO_2/SiGe MOS capacitors suggests excellent quality for the SiO_2/SiGe-shell interface. Also, the comparably low D_{it} for Al/SiO_2/Ge-dot/SiO_2/SiGe MOS capacitors suggests that the SiO_2/Ge-dot interface system is at least as good as the SiO_2/SiGe-shell interface. The apparent weak-inversion humps induced in Al/SiO_2/Ge-dot/SiO_2/SiGe n-MOS devices at 300 K, and which are suppressed at 77 K, probably originate from the fast capture and emission of carriers within the small bandgap of Ge (Marten et al., 2008; Kobayashi et al., 2009; Swaminathan et al., 2010).

The Al/SiO_2/Ge-dot/SiO_2/SiGe heterostructures exhibit a larger negative V_{fb} than the corresponding NiGe-dot/SiO_2/SiGe MOS capacitors, as shown in **Figure 5A**. Also, the measured V_{fb} is nearly independent of the dot size (20–90 nm) or the original nano-pillar diameter (30–240 nm). In theory, V_{fb} is primarily determined by the work function difference (φ_{ms}) between the gate material and the semiconductor. V_{fb} values are modified by stored charges (fixed charge: Q_f and interfacial charges: Q_{it}) located at the gate oxide/semiconductor interface, i.e., $V_{fb} = \varphi_{ms} - (Q_f + Q_{it})/C_{ox}$. Considering the work functions for Al (4.16 eV), NiGe (5.2 eV), Ge (4.33 eV), and SiGe (4.55 eV) and the gate oxide thickness of 3–4 nm, our experimental observations of negative V_{fb} suggest estimated positive fixed charge densities of $\sim 5 \times 10^{11}$ cm^{-2} at interfaces of SiO_2/SiGe and SiO_2/Ge dot. It is interesting to note that the positive fixed charges measured for our NiGe/SiO_2/SiGe and Al/SiO_2/Ge-dot/SiO_2/SiGe MOS capacitors are in contrast to the conventional expectation of negative fixed charges produced by the thermal oxidation of SiGe alloys (LeGoues et al., 1989; Nayak et al., 1990, 1992) or at high-k dielectric/Ge interfaces generated either by chemical vapor deposition or atomic layer deposition (Bai et al., 2005; Zhang et al., 2006; Deng et al., 2011) As described in our previous reports (Kuo et al., 2012; Lai et al., 2015), the interfacial SiO_2 layer between the Ge dot and the SiGe shell is formed by the thermal oxidation of Si interstitials that are released from the Si substrate. The oxide layer between the Ge dot and the deposited Al gate is formed by the thermal oxidation of Si interstitials that migrate along the surface of Ge dot to its distal end. We believe that the observed positive fixed charges and interface traps very likely originate from dangling bonds within the SiGe shell and from residual, unoxidized Si interstitials. To our knowledge, the experimentally

measured interface trap densities and fixed charge densities in our self-organized Ge-dot/SiO_2/SiGe gate-stack heterostructures are better, or at the very least, comparable to the reported values (10^{11}–10^{12} cm^{-2}) for Ge/GeO_2 or Ge/GeO_2/high-*k* MOS devices (Swaminathan et al., 2009; Lee et al., 2011; Nishimura et al., 2011; Xie et al., 2012; Zhang et al., 2012; Takenaka et al., 2013). In these cases, the Ge/GeO_2 structures are subjected to the additional expense of special interfacial treatments prior to and following gate oxidation. The exploration of post-annealing processes for suppressing fixed charges and interface traps are the subject of ongoing research.

In conclusion, we report the first-of-its-kind, unique, CMOS-compatible approach for generating a self-aligned, gate-stacking MOS heterostructure of SiO_2/Ge-dot/SiO_2/Ge-shell over the Si substrate. Our MOS structures are nanofabricated in a single oxidation step of SiGe nano-pillars that are lithographically patterned over a buffer Si_3N_4 layer on the Si substrate. Process-controlled tunability of the Ge-dot size (20–90 nm), the SiO_2 thickness (3–4 nm), and the SiGe-shell thickness (2–15 nm) have been demonstrated. Good interfacial and electrical properties with low D_{it} of $3–5 \times 10^{11}$ $cm^{-2}\cdot eV^{-1}$ and fixed charge densities of $1–5 \times 10^{11}$ cm^{-2} are observed for SiO_2/SiGe and SiO_2/Ge interfaces, respectively, and are comparable to literature-reported values for state-of-the-art Ge MOS capacitors. In comparison to previously proposed Ge-based devices, our MOS heterostructure not only exhibits superior performance but also has simplicity and elegance in terms of its one-step fabrication process. Therefore, we envisage further scientific exploration of our MOS heterostructures toward the ultimate goal of demonstrating advanced Ge-based MOS nanoelectronic and nanophotonic devices.

AUTHOR CONTRIBUTIONS

W-TL conceived the experimental work and contributed to data analysis and the manuscript preparation. K-CY performed structure/device fabrication and characterization. P-HL carried out the diffraction pattern and Raman examination and analysis. TG conceived the mechanism of heterostructure formation and revised the manuscript. P-WL conceived the study, revised the manuscript, and supervised the work. All authors read and approved the final manuscript.

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