Design of Integrated Gate Driver With Threshold Voltage Drop Cancellation in Amorphous Silicon Technology for TFT-LCD Application

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***Abstract*—A new integrated gate driver has been successfully designed and fabricated by amorphous silicon (a-Si) technology for a 3.8-in WVGA ($800 \times \mathrm{RGB} \times 480$) TFT-LCD panel. With the proposed threshold voltage drop-cancellation technique, the output rise time of the proposed integrated gate driver can be substantially decreased by 24.6% for high-resolution display application. Moreover, the proposed noise reduction path between the adjacent gate drivers can reduce the layout area for slim bezel display. The transmittance brightness and contrast ratio of the demonstrated 3.8-inch panel show almost no degradation after the 500 h operation under 70 °C and −20 °C conditions.**

***Index Terms*—Amorphous silicon (a-Si), gate driver, thin-film transistor liquid-crystal display (TFT-LCD).**

I. Introduction

IN RECENT YEARS, the consumer electronic devices with high resolution, light weight, narrow bezel, low cost, and low power consumption are gaining popularity. Therefore, the integrated gate driver using amorphous silicon (a-Si) technology for the TFT-LCD has become the main stream due to the mature manufacturing, low-cost processing, and elimination of the gate driver ICs [1]–[12]. Nevertheless, design of the integrated gate driver encounters two main challenges, which are the low field-effect mobility and the reliability issue under high-voltage stress. In order to alleviate the low-mobility restriction, the thousands of micrometer width of the main driving thin-film transistor (TFT) is required to drive the gate line of the panel. However, it inevitably comes with a large parasitic capacitance. In addition, the reliability issue of the integrated gate driver is also a notable challenge. While a-Si TFT suffers long-term high-voltage stress, the defect-state creation in a-Si:H as well as the charge trapping at the interface of the insulating and active layers will cause threshold voltage shifts to decrease the lifetime of the integrated gate driver [13]–[17].

Manuscript received March 14, 2011; revised May 11, 2011 and May 26, 2011; accepted July 14, 2011. Date of current version October 21, 2011. This work was supported in part by Giantplus Technology Corporation, Taiwan; and by the National Science Council, Taiwan, under Contract NSC 100-2628-E-009-016-MY3 and .99-2221-E-009-116; and by the "Aim for the Top University Plan" of National Chiao-Tung University and the Ministry of Education, Taiwan.

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Digital Object Identifier 10.1109/JDT.2011.2162937

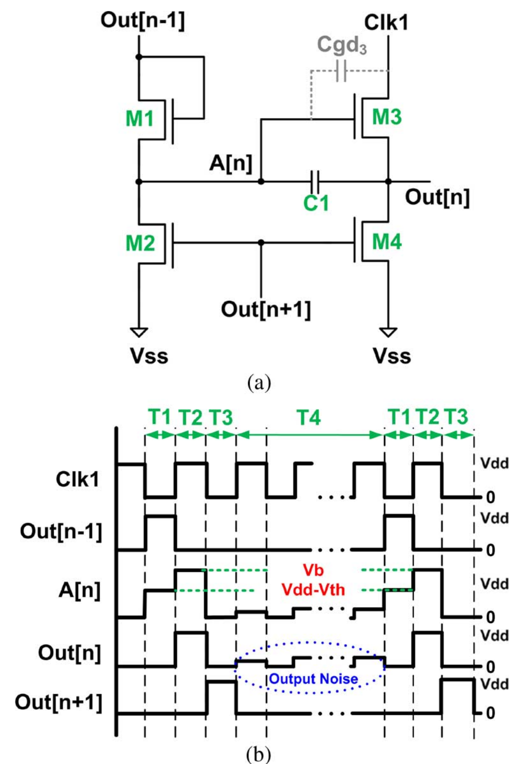


Fig. 1. (a) Schematic of the Thomson's shifter register circuit [2], [3]. (b) Corresponding control signals and outputs.

So far, a-Si integrated gate driver was originated from Thomson's shifter register which was composed of four transistors and one capacitor [2], [3]. Fig. 1(a) and (b) presents the schematic and its corresponding control signals. In the T1 period, $\mathrm{A[n]}$ is pre-charged to Vdd-Vth through M1, where the Vth is the threshold voltage of M1 and $[\mathrm{n}]$ is the nth gate line of the panel. Subsequently, Clk1 becomes high and $\mathrm{Out[n]}$ is charged by M3. At this moment, $\mathrm{A[n]}$ is simultaneously boosted from Vdd-Vth to a higher voltage (Vb) through C1. $\mathrm{Out[n]}$ represented the Vdd level in the T2 period. In the T3 period, M2 and M4 are turned on by the next output node $(\mathrm{Out[n+1]})$ to discharge $\mathrm{A[n]}$ and $\mathrm{Out[n]}$. The shifter register works repeatedly when voltage level of the previous output node $(\mathrm{Out[n-1]})$ becomes high again. Therefore, $\mathrm{Out[n]}$ is floating during most of the frame time in the T4 period and output voltage is continuously coupled by Clk1 through the parasitic capacitance (Cgd3) to produce the output noise. For this reason, adding two transistors into Thomson's shifter register were proposed to form a noise reduction path to release output noise from clock coupling [5]. Nevertheless, it also led

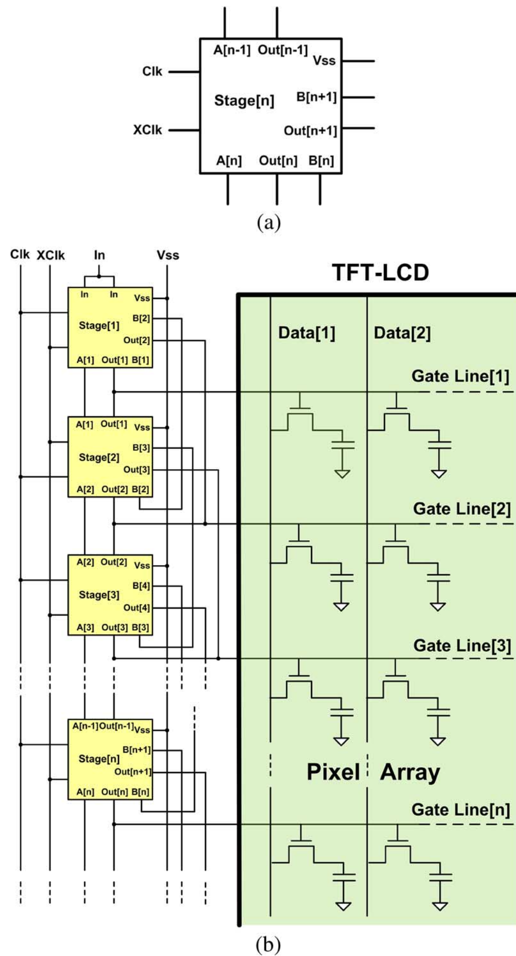


Fig. 2. (a) Block diagram and (b) connections between stages of the proposed integrated gate drivers for TFT-LCD application.

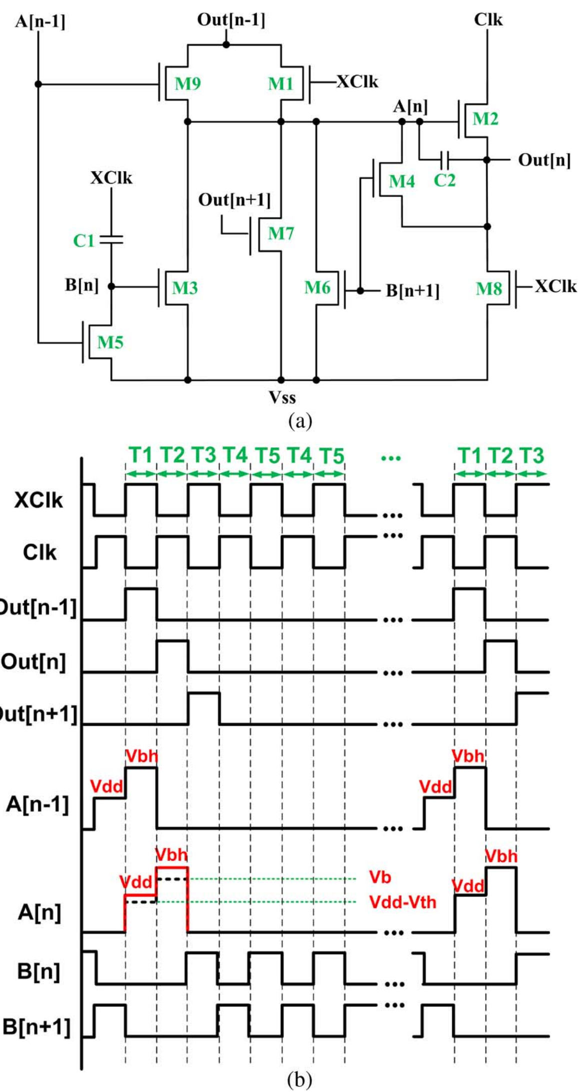


Fig. 3. (a) Schematic diagram and (b) corresponding operation waveforms of the proposed integrated gate driver.

to a serious Vth shift for pull down TFTs since their operations were analogous to dc stress. To alleviate this effect, the manners of pull down TFTs operated alternately with the 50% duty cycle were proposed to reduce the stress effect [6], [7]. Besides, Choi *et al.* [8] reported the center-offset a-Si:H TFTs which were utilized as pull-down TFTs in the integrated gate driver for higher reliability.

From the prior arts, the input transistor is mostly implemented by the circuit style of diode connection, similar as M1 in Fig. 1(a). Hence, $\mathrm{A[n]}$ is restricted to Vdd-Vth in the T1 period. The output rise time in the T2 period is thereby degraded due to the threshold voltage drop at $\mathrm{A[n]}$. In this work, the proposed integrated gate driver uses the threshold voltage drop-cancellation method to resolve the lower output rise-time issue. In addition, the proposed noise-reduction path between the adjacent gate drivers can reduce the layout area for slim bezel display.

II. Operation of the Proposed Integrated Gate Driver

The block diagram of the proposed integrated gate driver is shown in Fig. 2(a), which is composed of the input signals ($\mathrm{A[n-1]}$ and $\mathrm{Out[n-1]}$), control signals (Clk and XClk), feedback signals ($\mathrm{B[n+1]}$ and $\mathrm{Out[n+1]}$), and output signals ($\mathrm{A[n]}$, $\mathrm{B[n]}$, and $\mathrm{Out[n]}$). Fig. 2(b) depicts the connections among the proposed integrated gate driver stages for TFT-LCD application. The block manipulation is activated while a start signal (In) inputs a high voltage level to Stage[1]. A pulse signal is subsequently generated at Out[1] and being acted as the start signal for Stage[2]. Accordingly, sequential pulse signal can be periodically transferred stage by stage for feeding the whole gate lines of the pixel array in TFT-LCD.

Fig. 3(a) presents the schematic diagram of the proposed integrated gate driver with its corresponding waveforms in Fig. 3(b). The high and low voltage levels in Fig. 3(b) are defined as Vdd and Vss, respectively. The operation can be divided into five periods: T1, T2, T3, T4, and T5. In the T1 period, M1, M8, M5, and M9 are turned on by XClk and $\mathrm{A[n-1]}$. The other transistors are turned off. At this moment, Out[n] is Vss through M8 and A[n] is charged by M1 and M9. Because M1 is operated in saturation region (diode connection), the threshold voltage drop (Vdd-Vth) will be applied at A[n]. Nevertheless, M9 is operated with its gate voltage of Vbh, which is larger than Vdd in the T1 period, so A[n] is charged to Vdd through M9 to avoid the threshold voltage drop. Therefore, the node voltages of A[n] and Out[n] are Vdd and Vss at the end of this period. The design

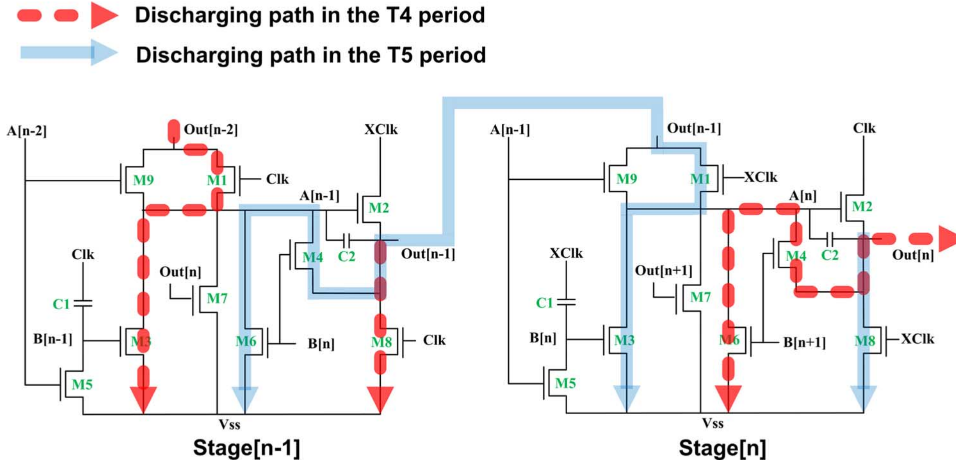


Fig. 4. Discharging paths between two adjacent stages in the T4 and T5 periods.

of M9 is utilized to cancel the threshold voltage drop as compared with the previous works using only the diode connection (M1).

In the T2 period, M1, M8, M5, and M9 are turned off by XClk and $\mathrm{A[n-1]}$. Clk becomes a high voltage level and then Out[n] is charged by M2. At this moment, A[n] is boosted through C2 from Vdd to a higher voltage level, which is labeled as Vbh in Fig. 2(b). The current can be derived from the linear region of M2 and depicted as [18]

$$I_{\mathrm{M2}} = K\frac{W}{L}\left(\mathrm{A[n]} - \mathrm{Out[n]} - \mathrm{Vth}\right)^{\alpha-1}\left(\mathrm{Vdd} - \mathrm{Out[n]}\right) \quad (1)$$

where K and α are the process-dependent parameters, and W/L is the aspect ratio of M2. Since IM2 is proportional to the A[n], higher A[n] leads to larger output charging current. Consequently, the output rise time of the proposed integrated gate driver can be substantially decreased due to larger IM2. In the T3 period, M1 and M8 are turned on by XClk. M3 and M7 are turned on by B[n] and $\mathrm{Out[n+1]}$. The other transistors are all keep at off state. At this period, A[n] and Out[n] are discharged to Vss by M3, M7, and M8. M1 is as a feedback path from Stage[n] to $\mathrm{Stage[n-1]}$ to speed up the discharging process.

After the T3 period, it leads to the T4 and T5 alterative transition periods until $\mathrm{Out[n-1]}$ becomes a high voltage level again. In these two periods, the output fluctuation noise induced by the clock transition (Clk and XClk) must be diminished to ensure the output with a constant voltage level (Vss). Therefore, an approach of sharing the noise-reduction path between the adjacent gate drivers is proposed and shown in Fig. 4. During the T4 period, M4 and M6 in Stage[n] are series connected with M1 and M3 in $\mathrm{Stage[n+1]}$ to form a discharging path (dash line) for settling $\mathrm{A[n-1]}$ and $\mathrm{Out[n-1]}$ to Vss. Similarly, M1 and M3 in Stage[n] are series connected with M4 and M6 in $\mathrm{Stage[n-1]}$ to form the other path (solid line) in the T5 period. Consequently, the noise is intensely minimized since both A[n] and Out[n] are discharged to Vss in the T4 and T5 periods. In addition, the layout area can be constructed with miniature size due to the sharing of the proposed noise reduction paths between the adjacent gate drivers.

TABLE I
DEVICE PARAMETERS OF THE PROPOSED INTEGRATED GATE DRIVER

TFT aspect ratio W/L (μm/μm)			
M1	300/3	M6	150/3
M2	4000/3	M7	500/3
M3	100/3	M8	2000/3
M4	150/3	M9	100/3
M5	100/3		
Capacitance (pF)			
C1	4	C2	3

III. EXPERIMENTAL RESULTS AND DISCUSSION

A. *Simulation of the Proposed Integrated Gate Driver*

The proposed integrated gate driver was designed and verified by HSPICE simulation with the RPI a-Si TFT model $(\mathrm{Level} = 61)$ provided by the foundry. The field-effect mobility and threshold voltage of a-Si TFT are 0.369 $\mathrm{cm^2/V \cdot s}$ and 4.019 V, respectively. The widths of M2 and M8 of the proposed integrated gate driver are designed with thousands of micrometers for faster speed in a few microseconds to pull the output loading of oscilloscope up and down. Although the lager widths of M2 and M8 can reinforce output charging and discharging speed, these accompany with larger parasitic capacitances which decrease the boosted voltage of A[n] [Vbh-Vdd in Fig. 3(b)] to further reduce the output charging speed [19]. Furthermore, the clock-induced output noise of the integrated gate driver also becomes severely from larger parasitic capacitance [5]. The tradeoff between speed and parasitic effects should be an explicit concern during the design of the integrated gate driver. Therefore, the device parameters (channel width W to channel length L aspect ratio and capacitance) of the proposed integrated gate driver are indicated in Table I with the output loading (oscilloscope) of one capacitor (17 pF) in parallel with one resistor (10 MΩ). The input signals are composed of start (In), clock (Clk and XClk), and ground (Vss) signals with voltage levels from 25 to 0 V. In addition,

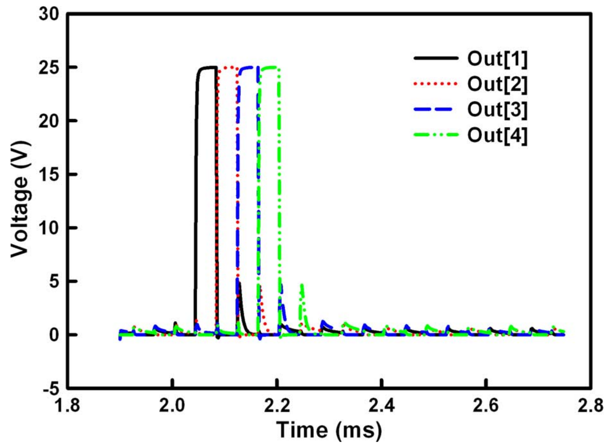


Fig. 5. Simulated output waveforms of the proposed integrated gate driver from the first to the fourth stages.

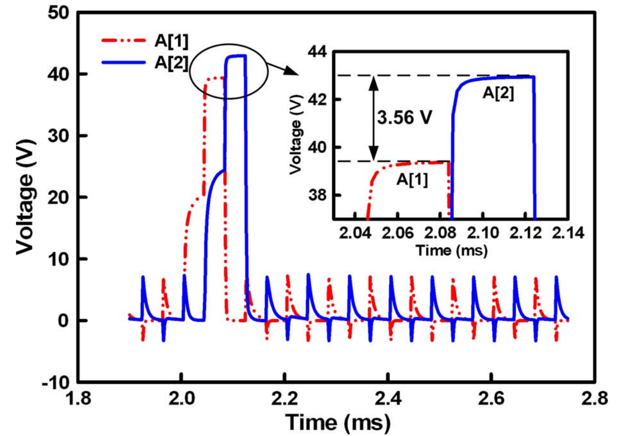


Fig. 6. Transient waveforms of A[1] and A[2] show the proposed integrated gate driver without (A[1]) and with (A[2]) threshold voltage drop cancellation method.

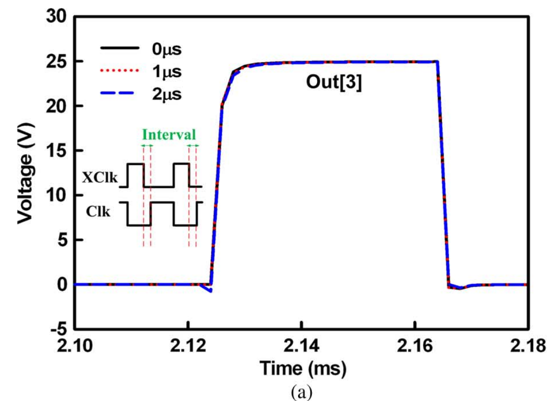
TABLE II
SIMULATED RESULTS OF THE PROPOSED INTEGRATED GATE DRIVER

	Rise time (μs)	Fall time (μs)	Noise RMS (V)
Out[1]	1.775	0.481	0.104
Out[2]	1.472	0.409	0.113
Out[3]	1.518	0.432	0.106
Out[4]	1.526	0.448	0.124

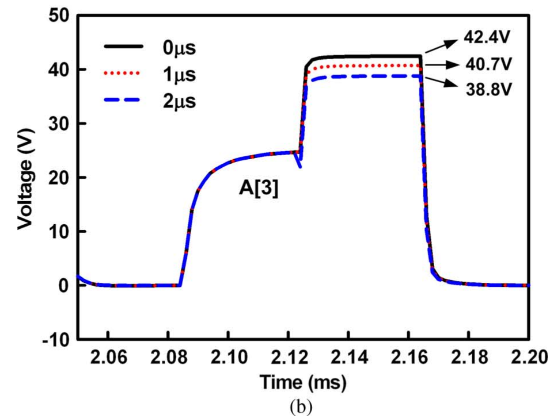
the duty cycle of the start and clock signals are 16.6 ms and 80 μs, respectively. The timing settings are according to the conventional frame time 16.6 ms (60 Hz) and 400 row numbers of a TFT-LCD panel.

Fig. 5 illustrates the simulated output waveforms of the proposed integrated gate driver from the first to the fourth stage. Sequential pulse signals have been successfully observed in Fig. 5 to verify the output function of the proposed integrated gate driver. The rise time, fall time, and noise rms voltage are represented in Table II, where the rise and fall times are defined by the time difference between 10% to 90% pulse voltage levels, the noise rms is the root mean square voltage of Out[n] in the T4 and T5 periods.

Table II presents that the rise times of Out[2], Out[3], and Out[4] are rapider than that of Out[1] (1.775 μs) which can be simpler figured out through the transient waveforms of A[1] and A[2] in Fig. 6. Since the Stage[1] does not have the feedback signal [Vbh in Fig. 3(b)] from the previous stage, the voltage difference between A[1] and A[2] is about 3.56 V, as derived from (1), A[n] is proportional to the charging current of M2, so Out[1] has longest rise time than that of other stages. With the proposed threshold voltage drop cancellation method, the rise time of the proposed integrated gate driver can be substantially decreased about 16%. Therefore, the first stage of the proposed integrated gate driver has to be set as a dummy stage to avoid the larger output rise time issue for panel integration. Furthermore, the issue of higher noise rms decreases the holding capability of pixel array which will reduce the image quality of the panel. Table II depicts that the noise rms values of the proposed integrated gate driver from Out[1] to Out[4] are comprehensively less than 0.13 V, which is much lower than the requested specification (0.5 V) from the foundry. Consequently, these simulation



(a)



(b)

Fig. 7. Simulated (a) Out[3] and (b) A[3] waveforms of the proposed integrated gate driver under three timing intervals (0, 1, and 2 μs).

results successfully confirm the proposed noise reduction path between the adjacent gate drivers which has lower noise rms to be capable of panel integration.

The discussions for a shortcoming of the proposed integrated gate driver are presented when it is applied to nonoverlapping gate pulses, which has been proposed to prevent crosstalk between adjacent rows. For this reason, timing intervals between the falling edge of XClk and rising edge of Clk (both Clk and XClk are 0 V) are varied to simulate the cases of overlapping and non-overlapping gate pulses. Fig. 7 depicts the simulated waveforms of the proposed integrated gate driver under three

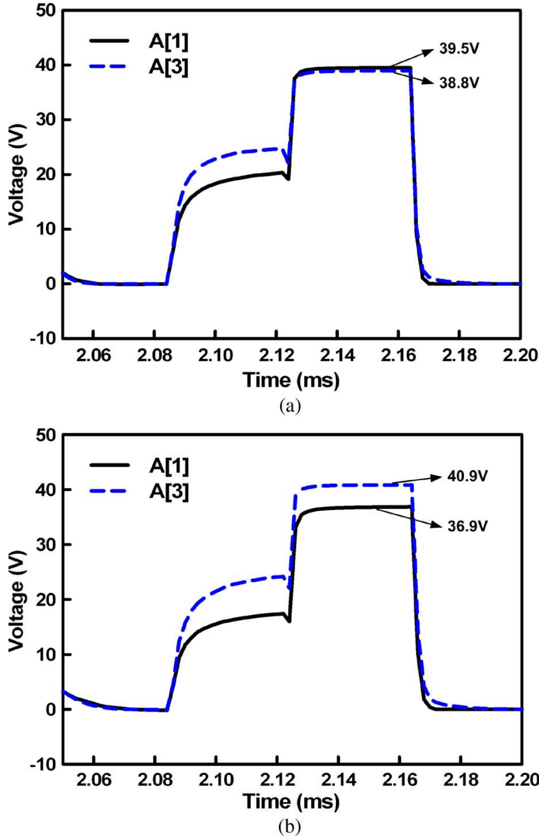


Fig. 8. Simulation results of A[1] and A[3] (a) before and (b) after all of the a-Si TFTs in the proposed integrated gate driver are suffering from 3-V threshold voltage shifts.

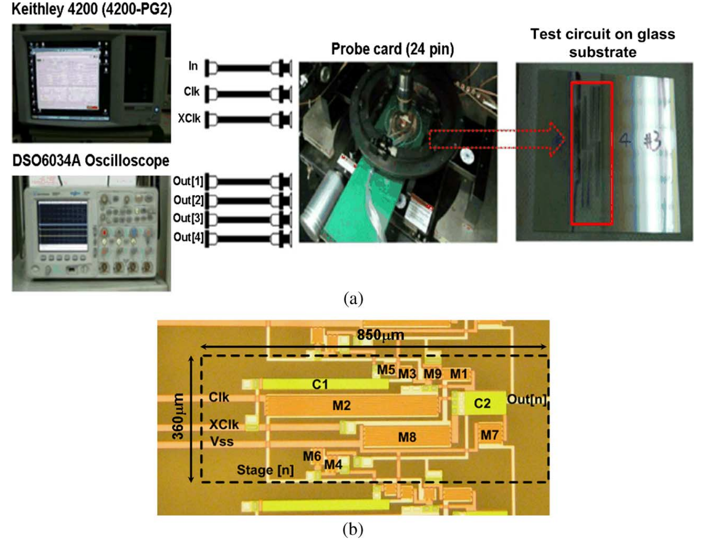


Fig. 9. (a) Measurement setups and (b) die photograph of the proposed integrated gate driver for array testing.

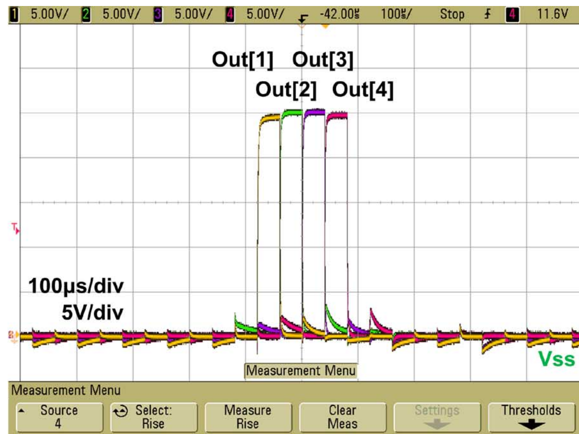
timing intervals (0, 1, and 2 μs). As derived from Fig. 7(a), the output rising time is degraded from 1.518 μs (0 μs) to 1.88 μs (2 μs), and A[3] is also decreased from 42.4 V (0 μs) to 38.8 V (2 μs) in Fig. 7(b). These can be explained in that, when Xclk goes low (after precharging A[3]) in the T2 period, A[3] will discharge through M9 because A[2] is still high, and this will reduce the overdrive of M2 when Clk eventually goes high. Therefore, M9 can provide additional drive and also be responsible for degrading the drive under the case of nonoverlapping gate pulses. Furthermore, noise rms is also increased from 0.106 V (0 μs) to 0.31 V (2 μs), which larger timing interval will diminish the noise reduction durations in the T4 and T5 periods, and thereby the lager noise rms is revealed.

Since stabilities of a-Si TFTs are crucial factors for the integrated gate drivers, the following simulation results still show the proposed integrated gate driver that has highly reliability even under the case of the 2-μs interval for nonoverlapping gate pulses. Fig. 8 shows the simulation results of A[1] and A[3] (a) before and (b) after all of the a-Si TFTs in the proposed integrated gate driver are suffering from 3-V threshold voltage shifts [20]. As shown in Fig. 8(a), A[1] (39.5 V) has lager value than A[3] (38.8 V), and the output rise times are 1.77 μs (Out[1]) and 1.88 μs (Out[3]), respectively, which seem to indicate that M9 is unnecessary for the integrated gate driver under the case of a 2-μs interval. Nonetheless, after all of the a-Si TFTs in the proposed integrated gate driver are suffering from 3-V threshold voltage shifts, Fig. 8(b) depicts that A[1] (36.9 V) has a lower value than A[3] (40.9 V), and the output rise times are 3.24 μs (Out[1]) and 1.96 μs (Out[3]). The degradation rates of rise time of Out[3] and Out[1] are 4.3% and 45.4%, and these can be referred from the previous statements about M9. Although it can be responsible for degrading the drive under the case of nonoverlapping gate pulses, when M9 suffers bias stress-induced threshold voltage shifts, the discharging current through M9 is decreased, and this means that A[3] has a higher voltage from 38.8 to 40.9 V in Fig. 8. Consequently, the proposed threshold voltage drop-cancellation method is quite suitable for long-term operation as compared with prior works even under the case of a 2-μs interval.

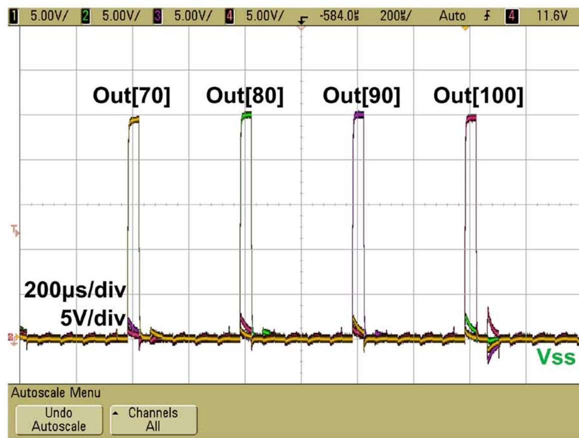
B. Measurement of the Proposed Integrated Gate Driver

For array verification, 100 integrated gate driver stages realized with the proposed threshold voltage-drop cancellation method are manufactured on glass substrate in amorphous silicon technology. As shown in Fig. 9(a), the measurement setups depict that the synchronous control signals (Clk, XClk, and In) are generated by the pulse card option for Keithley 4200 (4200-PG2), and the input range are set as 0 to 25 V. Furthermore, digital oscilloscope is utilized to observe the output waveforms. The equivalent loading of its probes is one capacitor (17 pF) in parallel with one resistor (10 MΩ) which is equal to the simulation environment. Moreover, the probe card with 24 pins is applied for the connections between fabricated circuit and measurement equipments. Fig. 9(b) presents the die photograph of the proposed integrated gate driver. Because the widths of M2 and M8 are designed with thousands of micrometers for pulling up and down the output node (Out[n]), the larger layout area is occupied by M2 and M8 in Fig. 9(b).

Fig. 10(a) shows the measured output waveforms of the proposed integrated gate driver from the first to fourth stages (Out[1], Out[2], Out[3], and Out[4]). In addition, Out[70], Out[80], Out[90], and Out[100] are shown in Fig. 10(b). The rise time, fall time, and noise rms of Fig. 10(a) are represented in Table III. As shown in Table III, the rise time results of Out[2], Out[3] and Out[4] are more rapid than Out[1] (2.32 μs) about



(a)



(b)

Fig. 10. Measured output waveforms of the proposed integrated gate driver at the outputs of (a) Out[1], Out[2], Out[3], Out[4] and (b) Out[70], Out[80], Out[90], Out[100].

TABLE III
MEASUREMENT RESULTS OF THE PROPOSED INTEGRATED GATE DRIVER

	Rise time (μs)	Fall time (μs)	Noise RMS (V)
Out[1]	2.32	1.41	0.318
Out[2]	1.68	1.21	0.28
Out[3]	1.75	1.12	0.25
Out[4]	1.67	1.17	0.278

24.6%. With the threshold voltage-drop cancellation method, the decreasing of 24.6% on rise time has been successfully verified and it is compatible with the simulation results in Table II. In addition, the noise rms values are less than 0.32 V to further determine the proposed noise reduction path between the adjacent gate drivers with lower noise rms to be capable for panel integration. These results demonstrate that the proposed integrated gate driver has faster output charging speed and lower output fluctuation with fine layout area by using the threshold voltage-drop cancellation method and sharing the noise-reduction path between the adjacent gate driver stages.

C. Panel Integration of the Proposed Integrated Gate Driver

A 3.8-in WVGA panel has been fabricated with the proposed integrated gate driver, and its specification is summarized in Table IV. The resolute ion of the panel is 800 $\times$ RGB $\times$ 480 with the contrast ratio of 350:1. In addition, the frame rate and back light brightness are 60 Hz and 4500 cd/m^2, respectively. Fig. 11 presents the photograph of the proposed integrated gate drivers that are allocated at the both sides of pixel array in a 3.8-in WVGA panel. The layout area of each stage is 207 μm $\times$ 900 μm under the layout optimization.

Fig. 12 shows the display image of a 3.8-in WVGA panel without the color filter cell. The average transmission brightness is 527 cd/m^2 under the back light brightness of 4500 cd/m^2, and the average contrast ratio is 353 in the demonstrated panel. For reliability (RA) testing, Figs. 13 and 14 show the contrast ratio

TABLE IV
SPECIFICATION OF A 3.8-in WVGA PANEL

	Specification
Panel size	3.8" diagonal
Resolution	800*RGB*480
Frame rate (Hz)	60
Pixel pitch (μm*μm)	103.5*103.5
Pixel density (ppi)	0.051
Back light brightness (cd/m^2)	4500
Contrast ratio	350:1
Integrated gate driver cell area (μm*μm)	207*900

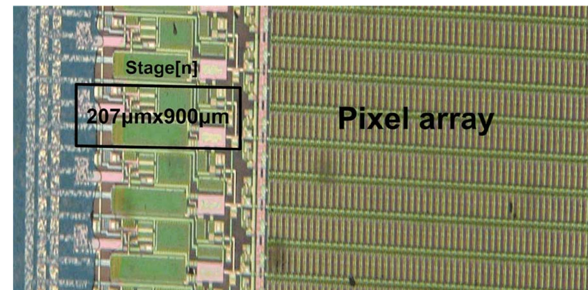
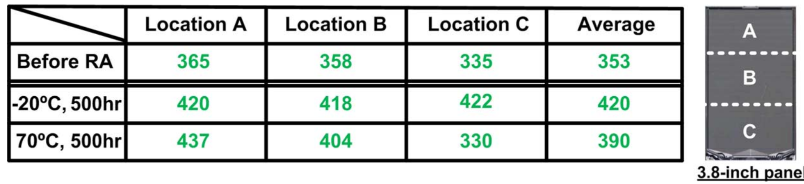


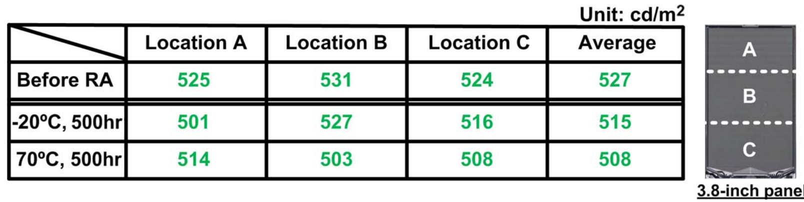
Fig. 11. Photograph of the proposed integrated gate drivers that are allocated at the both sides of pixel array in a 3.8-in WVGA panel.

Fig. 12. Display image of a 3.8-in WVGA panel without the color filter cell.



	Location A	Location B	Location C	Average
Before RA	365	358	335	353
-20ºC, 500hr	420	418	422	420
70ºC, 500hr	437	404	330	390

Fig. 13. Contrast ratio of the fabricated panel before and after 500 h operating at different panel locations (A, B, and C).



Unit: cd/m²

	Location A	Location B	Location C	Average
Before RA	525	531	524	527
-20ºC, 500hr	501	527	516	515
70ºC, 500hr	514	503	508	508

Fig. 14. Transmission brightness of the fabricated panel before and after 500 hours operating at different panel locations (A, B, and C).

and transmittance brightness of the demonstrated panel before and after 500 h operating under 70 °C and −20 °C conditions at different panel locations (A, B, and C).

Fig. 13 shows the average contrast ratio of the demonstrated 3.8-in panel which is from 353 to 390 (70°C) and 420 (−20 °C) after RA testing. Since these show the average contrast ratio that is not degraded after RA testing, the superior reliability of the proposed integrated gated driver is manifested. However, the larger variations before and after RA testing could be as results of the definition of the contrast ratio, the ratio of the luminance of the brightest color (white) to the darkest color (black), which depicts that the luminance of the darkest color varies slightly to further prompt the contrast ratio with larger variation.

Fig. 14 represents the average transmittance brightness which is from 527 to 508 cd/m^2 (70 °C) after RA testing. The decay rate is only less than 3.61% for passing the production standard of the foundry, where the decay rate is defined by the difference value of average transmittance brightness $(527 - 508 = 19)$ divided the value before RA testing (527). In summary, these results have completely verified the proposed integrated gate driver with good reliability for high resolution panel integration.

IV. Conclusion

An integrated gate driver with highly output charging speed has been successfully fabricated in amorphous silicon technology for a 3.8-in WVGA panel. The output rise time of the proposed integrated gate driver is dramatically reduced about 24.6% by using the threshold voltage drop cancellation method. For panel reliability testing, the decay rate of transmittance brightness for the demonstrated 3.8-in panel implemented with the new proposed integrated gate drivers represents less than 3.61%, and the contrast ratio shows almost no degradation after the operating of 500 h under 70 °C and −20 °C conditions. The proposed gate driver is quite appropriate for integration into to the high resolution TFT-LCD panels.

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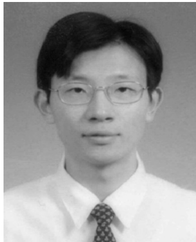

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