A thin FinFET Si-fin body structure fabricated with 193nm scanner photolithography and composite hard mask etching technique upon bulk-Si substrate

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ABSTRACT

A thin FinFET bulk Si-fin body structure has been successfully fabricated upon bulk-Si wafers through using 193nm scanner lithography and a composite hard mask etching technique. First, a 100Å-thick buffer SiO_2 layer was thermally grown upon the bulk silicon layer and subsequently a 1200Å-thick SiN_x layer and a 1000Å-thick TEOS SiO_2 hard mask layer was chemically vapor deposited to form a composite hard mask structure of buffer-SiO_2/SiN_x/TEOS. Second, both 1050Å-thick BARC and 2650Å-thick photoresist (P/R) were coated and a 193nm scanner lithography tool was used for the Si-fin body layout patterning under relatively high exposure energy. This achieves the ADI (after develop inspection) of 80nm from the original as-drawn Si-fin layout of 110nm. Then, a deep sub-micron plasma etcher was used for an aggressive P/R and BARC trimming down processing and both the capping TEOS and CVD-SiN_x with its underlying buffer oxide layers were subsequently etched in other etching plasma chambers, respectively. Resultantly, the AMI (after mask inspection) can reach 60nm. Subsequently, both the P/R and BARC were removed with a nominal plasma ashing as well as a RCA cleaning for the final sub-micron Si-fin plasma etching. Eventually, a 60nm-width and 400nm-height bulk Si-fin body structure can be successfully etched out after a fixed time-mode silicon plasma etching.

Keywords: Bulk-Si FinFET, Si-fin body, 193nm lithography, composite hard mask etching

Optical Microlithography XX, edited by Donis G. Flagello, Proc. of SPIE Vol. 6520, 65204N, (2007)
0277-786X/07/$18 · doi: 10.1117/12.714391

1. INTRODUCTION

1.1 Research Background

To achieve ultra-high density CMOS devices with high drive currents, 3D vertical double gate MOSFET device (FinFET) has emerged as a promising candidate compared with other double gate device structures due to its process compatibility with the traditional VLSI or ULSI logic devices [1-4]. Moreover, FinFET devices present some additional advantages such as: (1) shallow trench isolation is not necessary, (2) device drain induced barrier lowering (DIBL) or short channel effect (SCE) can be effectively improved due to good controlling of the gate electrode upon the erected ultra thin silicon body of Si-fin.

The conventional FinFET devices were fabricated upon SOI wafers to overcome problems associated with short channel effect (SCE). However, the unavoidable SOI heat transfer problem and high SOI wafer cost has necessitated the new FinFET device development upon the bulk-Si substrates. [5-9] In this work, we propose a feasible method to fabricate FinFET Si-fin upon bulk-Si wafers through using both the advanced 193nm scanner lithography and composite hard mask etching structure of buffer-SiO_2/SiN_x/TEOS.

2. EXPERIMENTS AND RESULTS

2.1 193nm scanner lithography

The bulk-Si wafers were used to fabricate high aspect ratio FinFET Si-fins with a traditional ULSI logic 90nm generation technology. Figure 1 shows a cross-sectional sketch of a bulk-Si FinFET Si-fin (W_{fin}=60nm) body structure with 4000Å (400nm) height after a time-mode bulk-Si etching through using a composite hard mask of buffer-SiO_2/SiN_x/TEOS. First, above the bulk-Si substrate the composite hard mask structure of LPCVD buffer-SiO_2 (100Å), PECVD SiN_x (1200Å) and TEOS (1000Å) were formed subsequently. Second, both 105nm-thick BARC and 265nm-thick deep ultra-violet (DUV) photoresist were coated through a NIKON track tool and a 193nm ASML scanner lithography tool was used for the ultra-narrow Si-fin layout patterning under relatively high exposure energy. This achieves ADI (after develop inspection) of ~80nm from the original as-drawn Si-fin layout of 110nm.

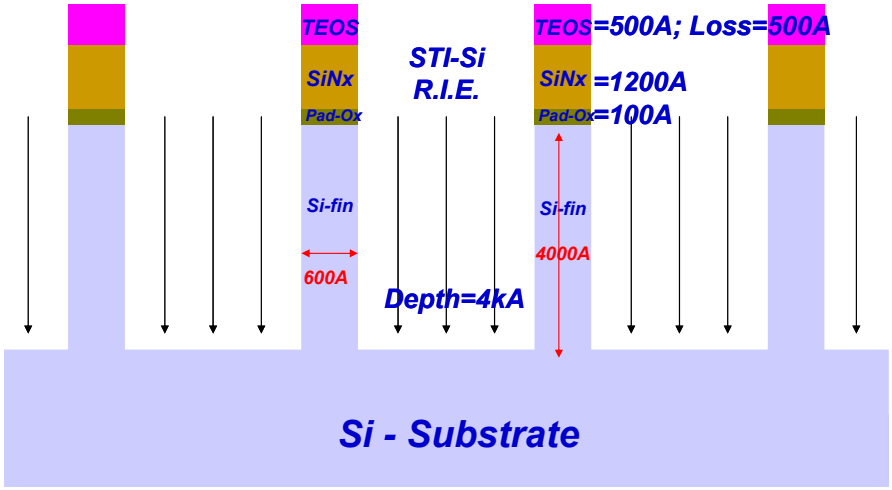

Figure 1 Cross-sectional sketch of a FinFET Si-fin (W_{fin}=60nm) body structure with 4000Å height after time-mode bulk silicon etching through using a composite hard mask structure of buffer-SiO_2/SiN_x/TEOS.

2.2 Composite hard mask plasma etchings

After the aggressive photolithography patterning with high ASML exposure energy, a deep sub-micron plasma etcher was used for both DUV photoresist and BARC trimming-down processing. Next, the 1000Å-thick TEOS layer with its upper DUV P/R developed Si-fin patterns was plasma etched and patterned in a second SiO_2 etching chamber without breaking the cluster etchers' loadlock vacuum. Continuously, the 1200Å-thick PECVD-SiN_x and its underneath buffer oxide was etched out by using the third SiN_x plasma etcher with over-time etching mode in the same cluster etcher tool. Subsequently, both the DUV P/R and its underneath BARC was removed with an additional photoresist ashing procedure. Consequently, the after-mask-inspection (AMI) width of the patterned composite hard mask of buffer-SiO_2/SiN_x/TEOS can reach ~60nm. Figure 1 displays that after these serial plasma etchings of composite hard mask structure, the top TEOS thickness will loss ~500Å and remain a final thickness of ~500Å. Figure 2 shows both tilted SEM AMI pictures of (a) single Si-fin and (b) multiple Si-fin after the composite hard mask plasma etchings and subsequent photoresist removing.

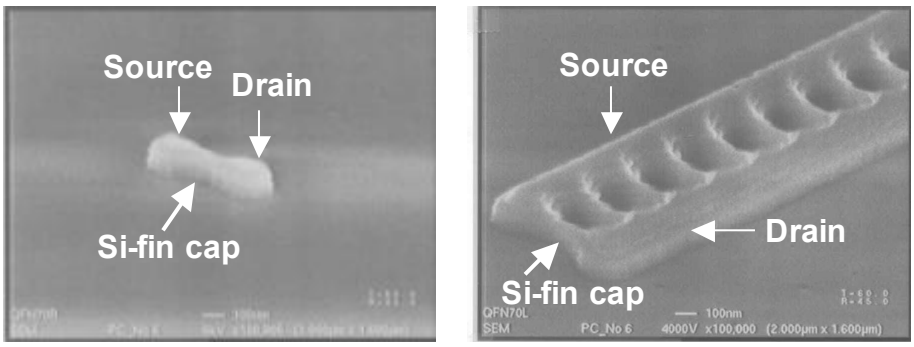

Figure 2 The tilted SEM AMI pictures of (a) single Si-fin and (b) multiple Si-fin just after composite hard mask etchings and subsequent photoresist removing. (Tilted SEM magnification rate=100KX)

2.3 Bulk Si-fin plasma etching

Through using the plasma defined composite hard mask the final bulk Si-fin body etching can be rendered by using a poly-Si etcher. With a fixed time-mode silicon etching, the bulk-Si etching can reach ~4000Å (400nm) depth and the Si-fin body width still keeps ~60nm. Figure 3 shows the tilted SEM images of (a) single Si-fin and (b) multiple Si-fin (11fins) just after the final silicon plasma etching. Hence, a high aspect ratio bulk-Si FinFET structure with its Si-fin body height/width=400/60nm can be eventually formed. This also means that it is possible to achieve relatively higher electrical device drive currents due to high aspect ratio of bulk Si-fin as its device conduction region.

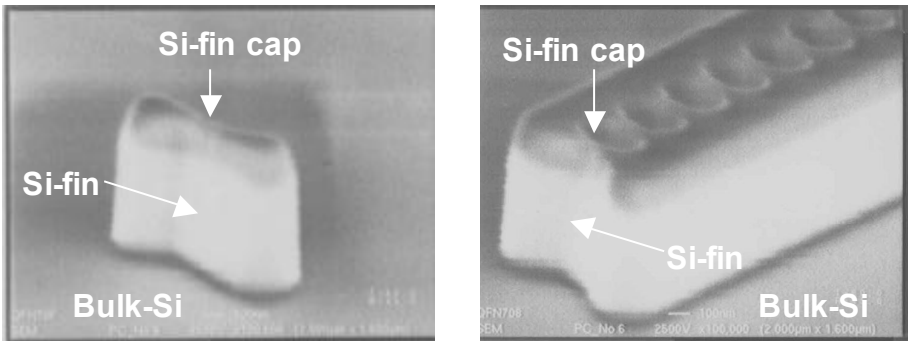

Figure 3 The tilted SEM pictures of (a) single Si-fin and (b) multiple Si-fin after a fixed time-mode bulk silicon plasma etching. (Tilted SEM magnification rate=100KX)

3. SUMMARY

A high aspect ratio FinFET bulk-Si fin body has been successfully developed on the bulk-Si wafers through using high exposing energy in a 193nm ASML scanner lithography tool and a specially designed composite hard mask etchings of buffer-SiO_2/SiN_x/TEOS. An high aspect ratio of bulk Si-fin body of height/width=400/60nm can hence be formed. This exhibits a possible realization of a 3D bulk-Si FinFET with its relatively high device density as well as high device drive currents due to high aspect ratio bulk Si fin body for both electron and hole carrier conductions.

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