A thick CESL stressed ultra-small (Lg=40nm) SiGe-channel MOSFET fabricated with 193nm scanner lithography and TEOS hard mask etching

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ABSTRACT

A 100Å-thick SiGe (22.5%) channel MOSFET with gate length down to 40nm has been successfully integrated with 14Å nitrided gate oxide as well as a 1200Å high-compressive PECVD ILD-SiN_x stressing layer as the contact etching stop layer (CESL) that enhances the PMOS electron mobility with +33% current gain. To achieve a poly-Si gate length target of 400Å (40nm), a 193nm scanner lithography and an aggressive oxide hard mask etching techniques were used. First, a 500Å-thick TEOS hard mask layer was deposited upon the 1500Å-thick poly-Si gate electrode. Second, both 1050Å-thick bottom anti-reflective coating (BARC) and 2650Å-thick photoresist (P/R) were coated and a 193nm scanner lithography tool was used for the gate layout patterning with nominal logic 90nm exposure energy. Then, a deep sub-micron plasma etcher was used for an aggressive P/R and BARC trimming down processing and the TEOS hard mask was subsequently plasma etched in another etching chamber without breaking the plasma etcher's vacuum. Continuously, the P/R and BARC were removed with a plasma ashing and RCA cleaning. Moreover, the patterned Si-fin capping oxide can be further trimmed down with a diluted $HF_{(aq)}$ solution (DHF) while rendering the RCA cleaning process and the remained TEOS hard mask is still thick enough for the subsequent poly-Si gate main etching. Finally, an ultra narrow poly-Si gate length of 40nm with promising PMOS drive current enhancement can be formed through a second poly-Si etching, which is above the underneath SiGe (22.5%) conduction channel as well as its upper 14Å-thick nitrided gate oxide.

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1. INTRODUCTION

1.1 Research Background

Silicon Germanium ($Si_{1-x}Ge_x$) has been considered as a promising device conduction layer for the sub-micron CMOS channel engineering.[1-2] Many researches have proved compressively strained SiGe channels could provide a significant mobility gain for long channel PMOS devices.[3-4] The mobility gain is attributed to the reduction of the hole effective mass as well as the splitting between heavy and light hole sub-bands. The SiGe-channel devices under tensile or compressive stressors to improve the device mobility and drive current have also been studied elsewhere.[5-6] In this work, we will explore an effective technique to fabricate an ultra-small gate length (L_g) of 40nm (Lg=40nm) SiGe-channel MOSFET fabricated with both the 193nm scanner lithography and TEOS hard mask in one of UMC 8" FAB in Hsinchu, Taiwan.

2. EXPERIMENTS AND RESULTS

2.1 High-stressed SiGe-channel with ultra-small gate length

Figure 1 is a process flow to fabricate the CMOS with SiGe channel and highly stressed contact etching stop layer (CESL). First, 3μm-thick epi-Si wafers were used with a traditional ULSI logic 90nm generation technology to fabricate the SiGe-channel MOSFET devices. An STI processing and N/PMOS well and threshold implants were processed followed by a high-temperature well RTA. After removing the remained sacrificial oxide with DHF, the wafers were sent to epi-grow a SiGe-channel structure composed of buffer-Si/SiGe(22.5%)/cap-Si with an AMAT tool and the cap-Si were fabricated with at least 9Å thickness after the growth of gate N/O. A plasma nitrided gate oxide of 14Å (physical thickness) was then grown upon the very thin surface of cap-Si. Subsequently, a 1500Å-thick un-doped polysilicon gate electrode was deposited followed by a high dosage phosphorus (P) implantation in the NMOS area. To achieve a poly-Si gate length target of 40nm, as shown in Fig. 1, a 193nm scanner lithography and an aggressive oxide hard mask etching techniques were used. Both the 105nm-thick BARC and 265nm-thick deep ultra-violet (DUV) photoresist were coated through a NIKON track tool and a 193nm ASML scanner lithography tool was subsequently used for an ultra-narrow gate layout patterning under relatively high exposure energy.

Continuously, a deep sub-micron plasma etcher was used for an aggressive P/R and bottom anti-reflective coating (BARC) trimming down processing and the TEOS hard mask was subsequently plasma etched in another etching chamber without breaking the plasma etcher's vacuum. Then, the P/R and BARC were removed with a plasma ashing as well as a RCA cleaning. Moreover, the patterned gate capping oxide can be further trimmed down with a diluted $HF_{(aq)}$ solution (DHF) while rendering the RCA cleaning process and the remained TEOS hard mask is still thick enough for the subsequent poly-Si gate main etching. Finally, an ultra narrow poly-Si gate length of 40nm with inherent PMOS drive current enhancement can be formed through a second poly-Si etching, which is just above the underneath SiGe (22.5%) channel and upper 14Å-thick nitrided gate oxide.

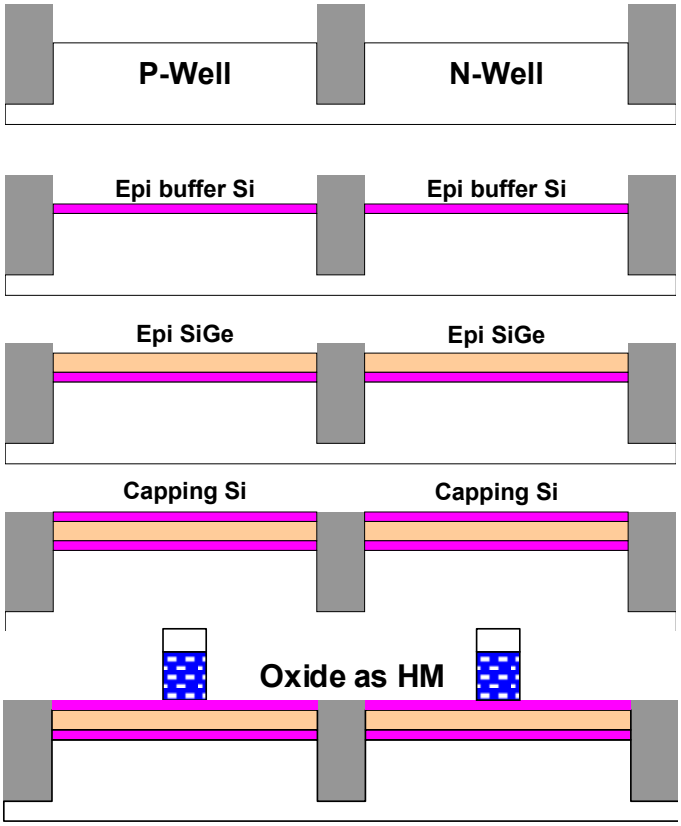

Figure 1 The schematic process flow for fabricating ultra-small gate length (Lg=40nm) SiGe-channel MOSFETs

2.2 Top-view SEM measurements

Figure 2 shows the after etching inspection (AEI) top-view of a poly-Si gate with its upper 50nm-thick TEOS hard mask. The SiGe conduction channel layer with its very thin capping oxide is just below the nitrided gate oxide and poly-Si gate electrode. In order to achieve a uniform and controllable gate length through the 193nm photolithography and plasma patterning, the dummy gate lines were also used in our experiment. Through using the remaining 50nm-thick thermal capping oxide as a hard mask for the final poly-Si etching, an ultra-narrow width below 45nm can be successfully fabricated eventually.

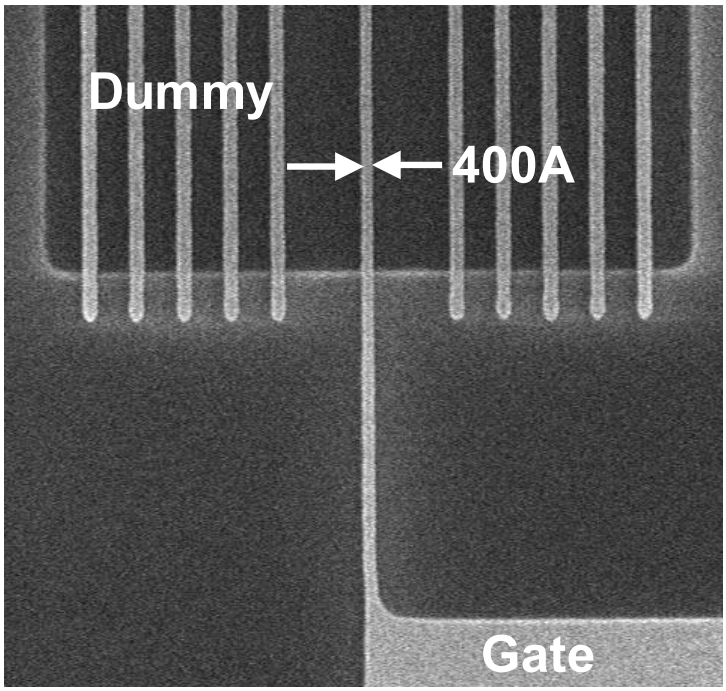

Figure 2 The after etching inspection (AEI) top-view image of Lg=40nm poly-Si gate electrode and its underneath SiGe-channel.

2.3 HRTEM X-TEM image

Figure 3 exhibits the high-resolution cross-sectional X-TEM image of a SiGe-channel MOSFET with its gate length of 40nm. This picture also shows that Lg=40nm poly-Si gate has been successfully fabricated upon the very thin (100Å) conduction layer of SiGe (22.5%) layer. The highly stressed CESL

SiNx layer for further device carrier mobility enhancement, NiSi source/drain for contact resistance reduction, as well as tunstung (W) plug in the contact hole can also be clearly identified.

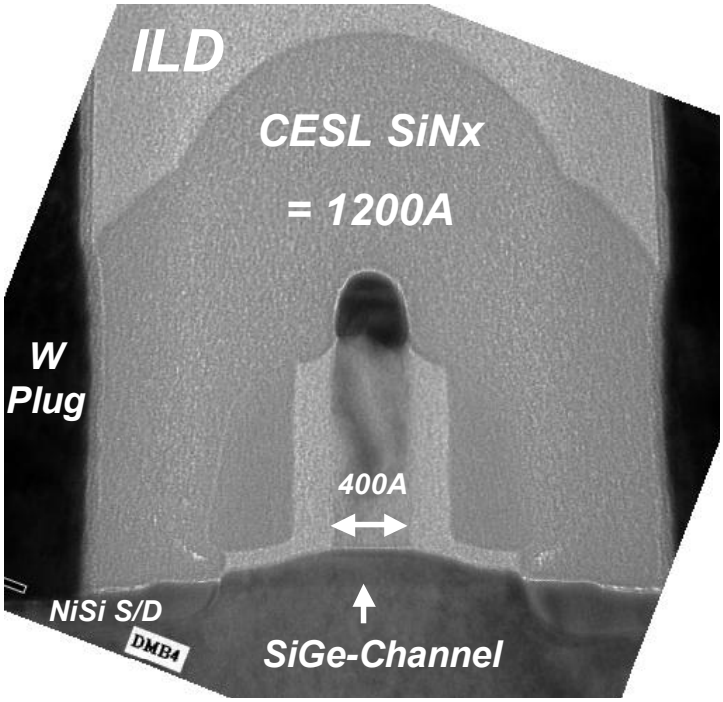

Figure 4 The X-TEM pictures of of a Lg=40nm SiGe-channel MOSFET with a compressive CESL ILD-SiN_x stressing layer. by a 193nm ASML scanner lithography.

3. SUMMARY

The SiGe-channel MOSFET with gate length down to 40nm has been successfully integrated with a nitrided gate oxide of 14Å as well as a 1200Å high-compressive or high-tensile CESL ILD-SiN_x stressing layer. Both 193nm scanner lithography and an aggressive oxide hard mask etching techniques were used to achieve the ultra-narrow gate length of 40nm with a very thin layer (100Å) of SiGe (22.5%) conduction layer. This means relatively higher CMOS device carrier mobilities as well as its drive currents can be drastically enhanced not only through the combination of high-mobility SiGe-channels and high-tensile CESL layers but also through the successful reduction of gate length to 40nm.

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