Low Resistivity Metal Silicide Nanowires with Extraordinarily High Aspect Ratio for Future Nanoelectronic Devices

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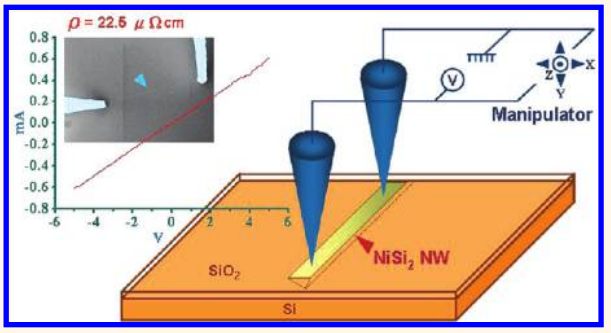
ABSTRACT



One crucial challenge for the integrated circuit devices to go beyond the current technology has been to find the appropriate contact and interconnect materials. NiSi has been commonly used in the 45 nm devices mainly because it possesses the lowest resistivity among all metal silicides. However, for devices of even smaller dimension, its stability at processing temperature is in doubt. In this paper, we show the growth of high-quality nanowires of $NiSi_2$, which is a thermodynamically stable phase and possesses low resistivity suitable for future generation electronics devices. The origin of low resistivity for the nanowires has been clarified to be due to its defect-free single-crystalline structure instead of surface and size effects.

KEYWORDS: nickel silicide · nanowires · low resistivity · high aspect ratio · epitaxy · nanoelectronic devices

As the scale of electronic devices continues to shrink, self-assembled one-dimensional silicon-based structures have received much attention for the use as a nanoscale device building block.[1] Metal silicides are an integral part of nanoelectronics. Recently, many one-dimensional epitaxial metal silicides have been grown.[2−9] Epitaxial silicide nanowires (NWs) with high aspect ratios can be fabricated by the reactive deposition epitaxy (RDE) method. Furthermore, the characteristics such as metal-like resistivity, excellent thermal stability, perfect single crystallinity, atomically flat interfaces with Si substrates, and high compatibility with the silicon process make epitaxial silicide NWs attractive for applications in nanoscale metallization as contacts and interconnects.

For self-assembled epitaxial silicide NWs, controlling the NW growth and investigating the electron transport properties of NWs are the two essential steps toward practical employment. A previous work revealed the nitride-mediated epitaxy (NME) effect on promoting growth of epitaxial silicide NWs.[7] The length and aspect ratio can be increased significantly by the NME effect.[8] The dependence of NW growth on the orientation or step edges of Si substrates was observed.[10,11] The resistivities of epitaxial silicide NWs were measured by different methods.[12−14]

The Ni/Si system is one of the most extensively studied systems for nanosilicide formation.[15−19] Among all Ni silicides, NiSi has been the most widely used silicides in sub-45 nm devices for its low resistivity.[20] However, one main deficiency of NiSi is its tendency to transform into $NiSi_2$, which is the stable phase of the Ni/Si system, at about 700 °C.[21] Metallic $NiSi_2$ was reported to possess considerably higher resistivity (35−50 $\mu\Omega$cm) than that of NiSi (14−20 $\mu\Omega$cm). It has also been widely investigated for the unique epitaxial growth of $NiSi_2$ on silicon.[22]

In this work, record low resistivity of epitaxial $NiSi_2$ NWs was discovered. The NWs were fabricated by combining the methods of RDE and oxide-mediated

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epitaxy (OME) and can reach several tens of micrometers in length with an ultrahigh aspect ratio. The average resisitivity of 30−35 nm diameter $NiSi_2$ NWs was determined to be as low as 22.5 $\mu\Omega$cm by a two-tip probing method in a scanning electron microscope. Such value is considerably lower than the bulk $NiSi_2$ value (35−50 $\mu\Omega$cm) and just slightly higher than the bulk NiSi value (14−20 $\mu\Omega$cm).[23] The result reveals the vast potential of eitaxial $NiSi_2$ NWs for applications in nanoscale device metallization as contacts and interconnects.

RESULTS AND DISCUSSION

Figure 1a,b shows SEM and TEM images of Ni silicide NWs on (001) Si substrates capped with 3 nm thick oxide thin films by RDE at 730 °C followed by post-annealing at the same temperature for 30 min, respectively. The phase of the NW was identified to be $NiSi_2$. The length, width, and aspect ratio of the individual wire in Figure 1a are 62.5 μm, 35 nm, and 1785, respectively. The density of the $NiSi_2$ NWs on Si substrates is about 2/10−5/10 μm^2 and can be controlled by post-annealing. Prolonging post-annealing time could lead to higher wire density. The NWs grow in ⟨110⟩ Si directions with flat edges, as shown in the TEM image in Figure 1b. It is worth mentioning that such an aspect ratio is about 9 times higher than that of other epitaxial silicide NWs reported to date.[8] The result can be attributed to the presence of a thin amorphous SiO_2 capping layer which serves as a diffusion barrier and effectively diminishes the flux of Ni atoms toward the Si surface.[7,24] The process of rearrangement of Ni adatoms is essential for NW growth since the Ni atoms impinge on the silicide from all sides during NW growth. Diminishing the Ni flux is beneficial to the rearrangement process and could lead to the high aspect ratio NWs with the shape transition predicted theroetically.[25,26] In addition to the flux adjustment, one main mechanism of OME or NME is to allow the metal-rich phase to be skipped and lead the formation of epitaxial NiSi2 phase directly.[24,27] For the 20 NWs measured, the average length and width are 25.5 μm and 38.6 nm, respectively. The most frequent widths were between 30 and 35 nm, but widths ranging from 16 to 52 nm have been observed. Compared to the epitaxial growth of $NiSi_2$ NWs with a thin nitride barrier layer in the previous work, NWs grown with a thin oxide layer in the present work possess much higher aspect ratio and smaller diameters.[7] The result is correlated to the lower rate of Ni atoms diffusing through amorphous SiO_2 layers than through amorphous Si_3N_4 layers.[28] Indeed, there was no silicide formation on the as-grown SiO_2-capped substrates. By the post-annealing process, the Ni atoms would arrive at the Si surface in succession with very low rate.

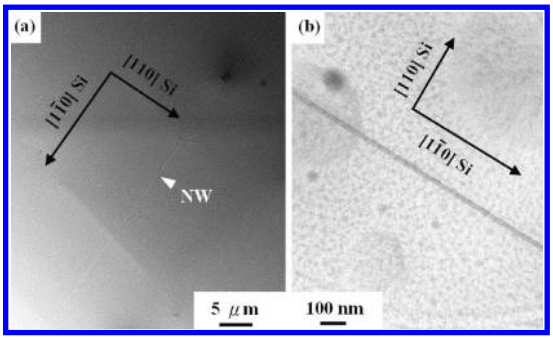

Figure 1. (a) SEM and (b) TEM images of epitaxial $NiSi_2$ NWs on (001) Si substrates capped with 3 nm thick oxide thin films by RDE at 730 °C followed by post-annealing at the same temperature for 30 min.

Before the electrical measurement, a marker was applied on the sample for tracing the specific NW, as shown in Figure 2a. Figure 2b shows the SEM image of two W probes conducting *I*−*V* measurements on a 32 nm wide NW. Electrical contacts of the probes to the NWs were controlled by an *in situ* multiple-probe manipulator. There are two essential steps for the measurements. First, the tips of W probes were locally melted by applying high current passing through two connected probes to remove the oxide on the tips before measurement. Second, we performed a destructive measurement by the tip penetrating into NWs to make an intimate contact between the tip and NWs. The trace of penetration can be seen in the inset of Figure 2b. The influence of the presence of surface oxide on *I*−*V* characteristics can be therefore eliminated. Resistance higher than the true values would be obtained if each of the above two steps was not implemented. The result of the measurement is shown in Figure 2c. The *I*−*V* curve with applied voltages ranging from −5 to 5 V is linear, and a resistance of 8.19×10^3 Ω can be obtained. Figure 2 (d) shows a resistance-length curve by altering the contact distance on a specific NW. The contact resistance can therefore be estimated to be less than 100 Ω, which is much smaller than the NW resistance and can be neglected in the present measurement. It is worth mentioning that, for the same nanowire, we have measured at least five times for each condition in Figure 2d. The values obtained at each point are within an extremely narrow range. The error bar is less than 1%.

TEM specimens cut from marked regions of the samples by FIB apparatus were used to determine the phase and cross section area of the individual NWs with measured resistances. Figure 3a shows a cross section TEM image viewed in the long direction of a specific NW. Figure 3b is an atomic resolution image at the region near the silicide/Si interface. The NW was identified to be $NiSi_2$ grown epitaxially into Si substrates (endotaxial growth).[6] The NW was almost completely submerged below the Si surface. A previous investigation shows that epitaxial silicide

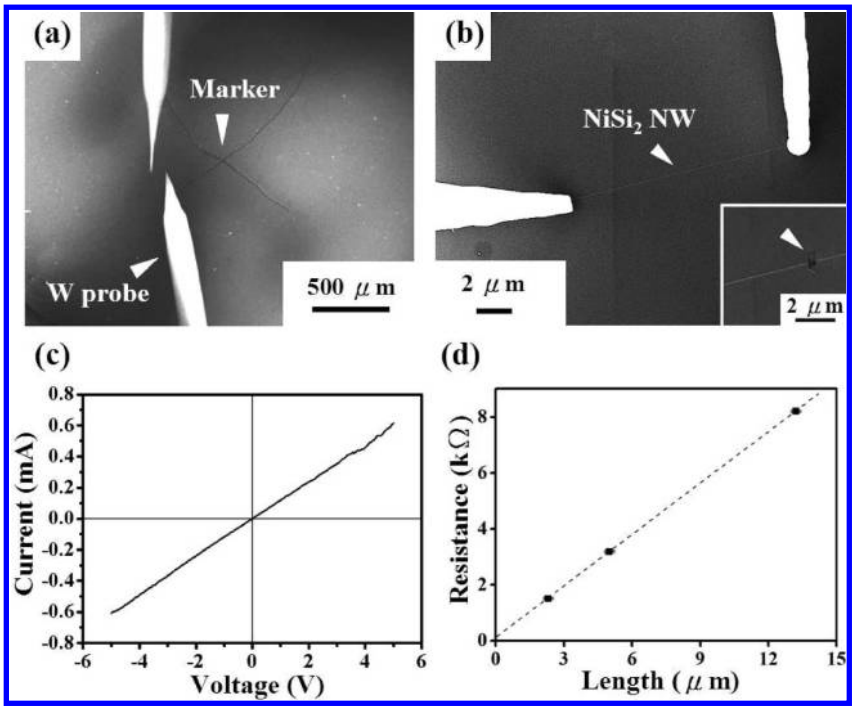

Figure 2. Process and results of electrical transport measurements. (a) Marked sample for tracing the specific NW. (b) SEM image of *I*−*V* measurements on a 32 nm wide NWs. (c) Resulting *I*−*V* curve with applied voltages ranging from −5 to 5 V. (d) Resistance−length curve obtained by altering the contact distance on a specific NW.

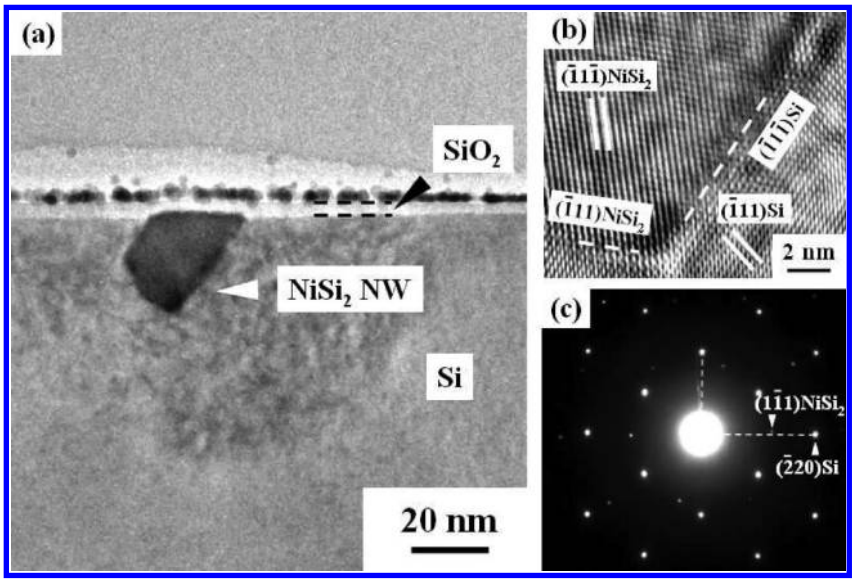

Figure 3. (a) Cross section TEM image of the $NiSi_2$ NW corresponding to that of Figure 2b. (b) Atomic resolution image at the region near the silicide/Si interface. (c) Selected area diffraction pattern. The streaking is due to artifact in the imaging system.

NWs were protruded above the surface in various proportions.[6] Analysis of the selected area electron diffraction pattern, shown in Figure 3c, indicates that the NW is of $NiSi_2$ phase with cubic CaF_2 structure. The formation of other Ni silicides, such as NiSi and Ni_2Si, can be excluded. In addition, the $NiSi_2$ NW is epitaxially related to the substrate with $[110]NiSi_2//[110]Si$ and $(1\bar{1}1)NiSi_2//(\bar{2}20)Si$ (off by about 2°). The slight misorientation (by about 2°) is perhaps caused by the local stress at the SiO_2/Si interface during the growth. Furthermore, there were no defects observed in the NW. The resistivity of the specific $NiSi_2$ NW can therefore be precisely calculated based on the known cross section area. For different nanowires investigated, ranging from 30 to 37 nm in diameter, the resistivity values range from 20.3 to 23.3 $\mu\Omega$cm, with an average value of 22.5 $\mu\Omega$cm, which is considerably lower than the bulk $NiSi_2$ value (35−50 $\mu\Omega$cm).[23]

A possible inaccuracy in the measurement is the electrical conductance through the Si substrate since

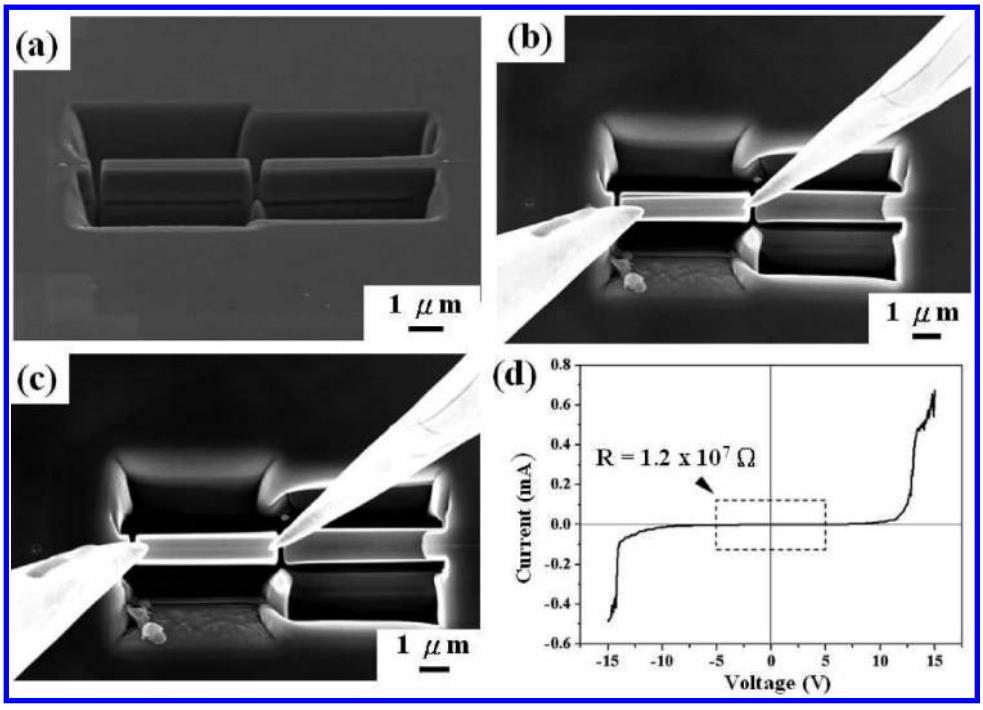

Figure 4. (a) Tiny Si block with an individual $NiSi_2$ NW on top obtained by cutting with FIB apparatus. (b) Loosely attached Si block structure can be displaced slightly by probes, indicating poor adhesion between the Si block and the substrate. (c) *I*−*V* measurements on an individual NW on the separated Si block. (d) *I*−*V* characteristic of W probes on Si.

the size of the probe tip is larger than those of NWs. Although the resistivity of Si wafers used in our work is about 10^6 times higher than $NiSi_2$, the far larger area in the cross section of the Si substrate could result in a lower resistance. A tiny block structure with an individual $NiSi_2$ NW on top cut from the Si substrate by focus ion beam (FIB) apparatus, as seen in the SEM image in Figure 4a, was used to limit the cross sectional area of the conducting path of the Si substrate. The measured resistances were compared with the measured values for the same NW prior to the cutting. The tiny Si block structure was separated from the surrounding regions and loosely attached to the underlying Si. The loose attachment was confirmed by the slight displacement of one end of the tiny block by probes, as verified in the SEM image shown in Figure 4b. As the Si block is about 1 μm in both width and thickness, its cross section area is about 1/10 000 × 1/500, that is, about 2×10^{-7} of the 1 cm (width) × 500 μm (thickness) specimen. On the other hand, the ratios of resistance and length (*R*/*L*) obtained by the *I*−*V* measurement on the individual NW before and after FIB cutting were found to be nearly identical with values of 4.57×10^3 Ω/7.5 μm and 1.97×10^3 Ω/3.3 μm, respectively. The ratio is therefore largely independent of the cross section area of Si. A further *I*−*V* measurement of W probes on Si, as shown in Figure 4d, indicates that a high resistance of 1.2×10^7 Ω in the range of −5 to 5 V was obtained. The value is significantly higher than the measured resistance on NWs. The conductance through Si substrates can therefore be neglected. Same conclusions can be drawn for the *I*−*V* measurements of two different nanowires. As a result, the measured resistance of the NW is very close to the true value.

A recent investigation on 15−45 nm diameter NiSi NWs synthesized by solid-state reaction of Ni-deposited Si NWs shows a resistivity as low as 9.5 $\mu\Omega$cm at 4 K.[29] In that investigation, the single-crystal NiSi NWs with resistivity equal to the bulk value can be scaled to 15 nm without degradation on electrical properties. The scattering of transport carriers in 15−45 nm diameter NiSi NWs was found to be negligible. Similar result can be found for single-crystal Ni_2Si NWs with a lower resistivity (20 $\mu\Omega$cm) than the bulk value.[30] In addition, Lim *et al.* found a lower resisitivity (13.7 $\mu\Omega$cm) for epitaxial Pt_2Si NWs with height and width less than 1 and 10 nm, respectively, than the bulk value and attributed it to the formation of a space charge layer under a metal−semiconductor interface consisting of silicide NWs and Si substrates.[31] The much lower interface/volume ratio of $NiSi_2$ NWs than Pt_2Si NWs in this work is expected to cause the carrier to transport mainly through the bulk NW. To clarify further the role of surface conduction, the resistivities of $NiSi_2$ NWs on both p-type and n-type Si substrates were measured and found to be identical. Since the distinct Schottky barrier heights at $NiSi_2$/p-Si and $NiSi_2$/n-Si interfaces did not lead to the variation on the measured resistivity, the surface conduction would not be the dominant factor in determining the resitivity.[32] As a result, the low resistivity value for a 30 nm diameter $NiSi_2$ NW is attributed mainly to the perfect-crystal feature of the NWs.

To determine whether there is a size effect on 1-D electrical transport, it is important to find out the electrical mean free path (l_{pm}) of carriers. By the equation proposed by Sagnes *et al.* for calculating the l_{pm} of metal and the electrical parameters of Ni silicide, the l_{pm} of $NiSi_2$ was estimated to be less than 5 nm and similar to that of NiSi at room temperature.[33,34] Therefore, the size effect should not be significant for electrical transport in 30 nm diameter $NiSi_2$ NWs in the present work.

Some recent studies on electrical transport of epitaxial silicide NWs showed higher measured resistivity compared to the bulk values. Okino *et al.* found a resistivity of 31 $\mu\Omega$cm for the 60 nm diameter epitaxial $CoSi_2$ NW.[13] Lin *et al.* and Li *et al.* found the resistivities of 800 and 700 $\mu\Omega$cm for a 15 nm diameter epitaxial $NiSi_2$ NW and a 20 nm diameter epitaxial $ErSi_2$ NW, respectively,[12,14] which are both much higher than bulk values. In the present instance, we utilized a unique measurement scheme to eliminate the inaccuracy on resistance caused by the contact problem and the existence of oxide layers and accurately determine the geometry of the specific NW for resistivity calculation. The measured resistivity of 22.5 $\mu\Omega$cm for 30−37 nm diameter $NiSi_2$ NWs is even lower than the bulk values. The low resistivity value for a 30 nm diameter epitaxial $NiSi_2$ NW can be considered to be intrinsic and related to the perfect crystallinity of the NW. Furthermore, the feature of atomically flat interface of epitaxial silicide NWs could minimize the generation of interface scattering.

$NiSi_2$ was known to have higher resistivity (35−50 $\mu\Omega$cm) than $CoSi_2$ (14−20 $\mu\Omega$cm) despite their identical crystal structures and epitaxial forms on Si.[23] According to Matthiessen's rule, the temperature-dependent resisitivity can be represented as $\rho(T) = \rho_0 + \rho_L(T)$, where ρ_0 is the residual resisitivity to reflect the structural contribution and $\rho_L(T)$ reflects the phonon contribution. A previous investigation on the electrical transport properties of $CoSi_2$ and $NiSi_2$ thin films showed the identical $\rho_L(T)$ and the divergent ρ_0 of $CoSi_2$ and $NiSi_2$ and attributed the divergence to the intrinsic defects in $NiSi_2$.[35] In other words, it is possible to lower the resistivity of $NiSi_2$ by inhibiting the defect generation, which is consistent with our finding and discussion. It is worth mentioning that there were reports on the formation of $NiSi_2$ by Ni-ion implantation with resistivity lower than the bulk values.[36,37] However, the works lacked the appropriate structural characterization of the dimensions, distribution, as well as morphological features of the silicides, so that the accuracy of the resistivity values needs to be verified.

NiSi/Si/NiSi nanowire heterostructures have been grown by several groups.[29,38−40] Silicon nanowire transistors have been fabricated for such heterostructures.[29,38] A very recent work for PtSi/Si/PtSi transistors based on intrinsic Si nanowires has achieved high performance normally off transistors.[41,42] In addition, sub-100 nm channel length Ge/Si nanowire transistors contacted with nanoscale $NiSi_xGe_y$ layer showing potential for 2 THz switching speed were reported.[43] With the discovery of low-resistivity $NiSi_2$, it shall be of much interest to investigate device characteristics of the $NiSi_2$/Si/$NiSi_2$ heterostructures.

In summary, record low resistivity epitaxial $NiSi_2$ NWs with extraordinarily high aspect ratio have been grown by the methods of RDE and OME. By the OME effect, the lengths of $NiSi_2$ NWs can reach 50−60 μm with typical widths ranging from 30 to 35 nm. The low resitivity is correlated to the defect-free single-crystal structure of $NiSi_2$ NWs. The high aspect ratio is attributed to the slow growth rate controlled by the presence of a thin amorphous SiO_2 layer acting as a diffusion barrier. As the resistivity of $NiSi_2$ is close to the commonly used low-resistivity NiSi, it has potential to resolve the stability issue of the transition form NiSi to $NiSi_2$ in the metallization of sub-45 nm integrated circuit devices.

METHODS

The RDE process was performed in an ultrahigh vacuum electron-beam evaporation chamber with a base pressure better than 3×10^{-10} Torr. Then, 2 nm thick Ni films were deposited onto p-type, boron-doped (001)-oriented Si wafers capped with a 3 nm thick SiO_2 layer, prepared by dry oxidation, and heated to 730 °C. The purity of the Ni source was 99.97%. The deposition rate was maintained to be less than 2×10^{-3} nm/s. After the RDE process, the as-grown samples were post-annealed in the same chamber at 730 °C for 30 min with a pressure better than 5×10^{-9} Torr.

The resistances were measured with a Keathly 4200-SCS semiconductor characterization system at room temperature. The measurement was performed in a Zeiss ultra-55 field-emission scanning electron microscope (FESEM) combined with a Zyvex S100 manipulator. The electrochemically etched W probes were used to contact with silicide NWs. One main feature of epitaxial silicide nanowires is the compatibility with the conventional Si processing. The direct *I*−*V* measurement of epitaxial silicide nanowires on Si substrates is advantageous since the influence of the silicide/Si interface on electrical conductance can be taken into account. A JEOL JSM-6500 FESEM and a JEOL 2010 transmission electron microscope (TEM) were used for the examination of morphology and structures. High-resolution lattice images were taken in a JEOL 3000F high-resolution TEM. The cross section TEM specimens for fixed-position observation were obtained with a SMI3050SE FIB−SEM hybrid system.

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