A high-speed 850-nm optical receiver by integrating Si photodiode and CMOS IC

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ABSTRACT

In this work, three approaches are proposed to implement high-speed 850-nm optical receivers fully in standard bulk 0.18 μm silicon (Si) CMOS technology. In the first approach, the lateral p-i-n photodiode (PD) with designed block well to limit the photocarriers being generated from the laterally depleted regions is integrated in optical receiver. The receiver consists of TIA, LA, offset-cancellation-network and buffer to provide a conversion gain of 110 dBΩ and data rate of 2.5 Gbps operation. In the second receiver, the spatially modulated PD (SMPD) with -3 dB bandwidth of 590 MHz is integrated in optical receiver with the extra adaptive equalizer and demonstrates a data rate of 3.125 Gbps. Finally, the proposed novel structure of PD eliminates the slow diffusion photocarriers by using body contact design to create a new current path under the PD. A bandwidth of 2.8 GHz with 100 % improvement in PD is obtained. The eye diagrams of PD with cable connected amplifiers at 2.5 Gbps, 4 Gbps and 5 Gbps are demonstrated. Furthermore, the optical receiver's optical-electrical (O-E) conversion bandwidth is also increased from 3.6 GHz to 4.3 GHz. To our knowledge, these are the highest O-E conversion bandwidth of the PD and optical receiver ever reported by using the standard bulk 0.18 μm Si CMOS technology.

Keywords: Si, 850-nm, optical receiver, CMOS, photodiode

1. INTRODUCTION

Optical receiver with monolithically integrated photodetector in standard silicon (Si) complementary metal oxide semiconductor (CMOS) technology has drawn tremendous research efforts recently [1]-[4]. In contrast to conventional multi-die solutions, which composed of photodetector implemented in expensive III-V technologies such as GaAs, and InP based devices technology, the fully integrated optical receiver in standard CMOS is much more cost effective. Moreover, these optical receivers which are adopted for short distance and high volume communication systems such as local area network (LAN), back plane interconnect and optical storage system applications that the cost issue can be mitigated compared to utilize the expensive III-V solutions. Besides, the Si photodetector is a good, low-cost approach for the general 850-nm vertical cavity surface emitting laser (VCSEL) transmitter.

In standard Si CMOS technology, the light detection is mainly performed by the reverse biased p-n junction diode. In the depletion region of the diode, the generated electron-hole pairs will be separated by electric field and result in a high-speed drift current. However, the penetration depth of the 850-nm wavelength light into silicon (~20 μm) is much deeper than that of the depth of depletion region (~2 μm). As a result, a large portion of carriers are generated in the Si substrate and diffuse in all directions. The slow diffusion carriers will reach the depletion region and lead to the slow response of the CMOS photodetector. On the other hand, from the perspective of a high speed light detection, the solution for decreasing the impact from those slow diffusion carriers is the crucial issue and should be circumvented in high speed monolithically integrated CMOS optical receiver design.

In this paper, there are three different kinds of solutions for mitigating the influence from diffusion carriers. In first design, the high speed operation is achieved by utilizing a proposed lateral p-i-n photodiode (PD). The PD with designed block well which consists of n-well and deep n-well lets that the photocarriers are mainly generated from the laterally depleted regions is integrated in optical receiver and shows a data rate of 2.5 Gbps. Moreover, it achieves higher sensitivity as well as operating speed compared to the prior art [2] without equalizer.

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In second design, the different layout topologies of the spatially modulated PD (SMPD) [1]-[3], in which the cancellation of the partial diffusion photocurrent in the substrate is realized by subtraction of the signal from the illuminated and shaded diodes, are compared and investigated to achieve the highest gain bandwidth product. Finally the SMPD with a -3 dB bandwidth of 590 MHz and a responsivity of 0.07 A/W is integrated in optical receiver with adaptive analog equalizer and demonstrates a data rate of 3.125 Gbps.

In third design, a novel method to eliminate the slow diffusion photocarriers is presented. The designed current flow under PD results in eliminating the long tail in pulse response directly. The PD (50×50 μm^2) with cable connected transimpedance amplifier (TIA) shows improved bandwidth from 1.4 GHz to 2.8 GHz and data rates of 2.5, 4, and 5 Gb/s operation. Consequently the optical receiver with smaller active area (20×20 μm^2) PD shows the improved bandwidth of the optical-electrical (O-E) conversion from 3.6 GHz to 4.3 GHz by tuning the body voltage. To our knowledge, these are the highest O-E conversion bandwidth of PD and receiver circuit in standard bulk CMOS technology.

2. LATERAL P-I-N PD DESIGN IN OPTICAL RECEIVER [5]

The lateral p-i-n PD is fabricated by a p^+/p-substarte/n^+ interleaved architecture. Figure 1 illustrates the top view and cross-sectional view of the PD. The PD's active region is surrounded by n-well and deep n-well. The top of the sensing region is striped of salicide and passivation layer to disconnect $p^+/p^-/n^+$ regions. Compared to conventional p substrate/ n^+ junction, the electron-hole pairs are mainly generated in the laterally depleted regions and the block well (surrounded n-well and deep n-well) protects the PD from substrate noise coupling.

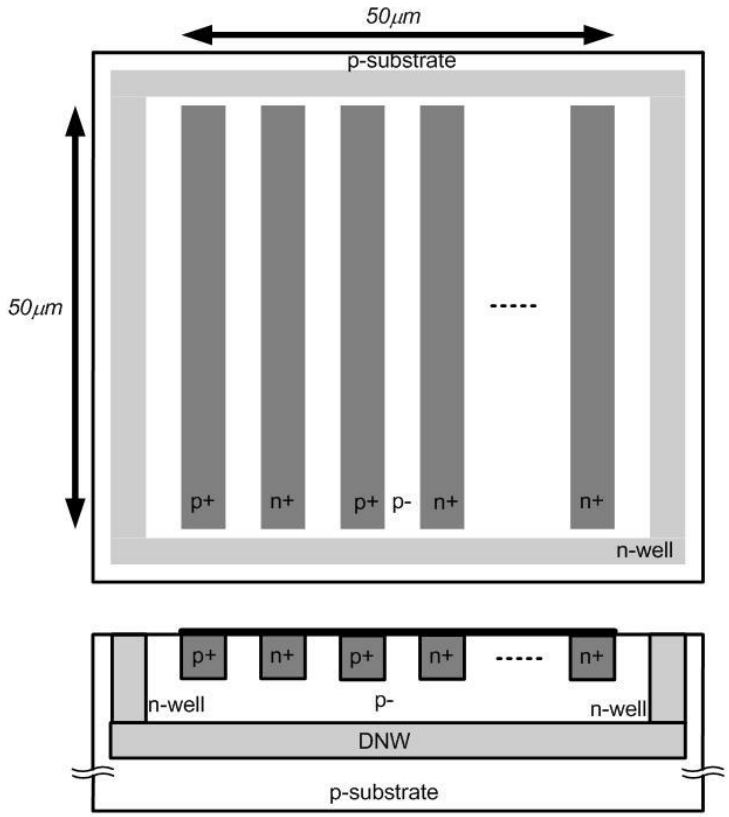


Fig. 1 The illustrations of the top view and cross-sectional view of the lateral p-i-n PD.

The dimension of the PD is 50×50 μm^2 which consists of 13 p-i-n fingers. The p^+ and n^+ strips are 1.45 μm wide, separated by 0.5 μm wide p-substrate region. Thus a reasonable low (~ 2 to 6V) reverse biased voltage is sufficient to deplete the p- region within the cathode and anode of the PD for a high speed operation. The proposed architecture is expected to provide a higher responsivity by enlarging the p-substrate region and operated in the avalanche mode.

2.1 Receiver circuit

The architecture of the fully integrated optical receiver is shown in Fig. 2. The incoming optical signal is converted to a modulated photocurrent by the on chip integrated PD, and regenerated to a voltage signal of 420 mV-V_{PP} by a transimpedance amplifier (TIA) and a post limiting amplifier (LA). To alleviate bandwidth degradation caused by the parasitic capacitance of the PD, a regulated cascode (RGC) topology is adopted as the input stage [6].

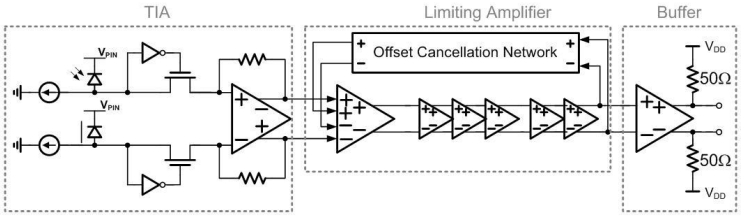


Fig. 2 The architecture of the monolithically integrated optical receiver with the on-chip lateral p-i-n PDs.

In this design, the conversion gain of the TIA is about 60 dBΩ and the -3 dB bandwidth is chosen to be about 2.58 GHz. Figure 3 illustrates the circuit schematic of the TIA incorporating with the PD. The TIA is in pseudo differential architecture, composing of an RGC input stage followed by a common source gain amplifier with shunt-feedback. When light illuminates on the PD D_1, the photocurrent I_{in} is injected into the main amplifier (M_1, M_3, M_5, R_1, R_3, R_5, and R_{f1}). The amplifier on the right hand side (M_2, M_4, M_6, R_2, R_4, R_6, and R_{f2}) along with dummy diode D_2 is a replica to provide a DC biased voltage for the TIA to perform single to differential voltage conversion (V_{OUT}).

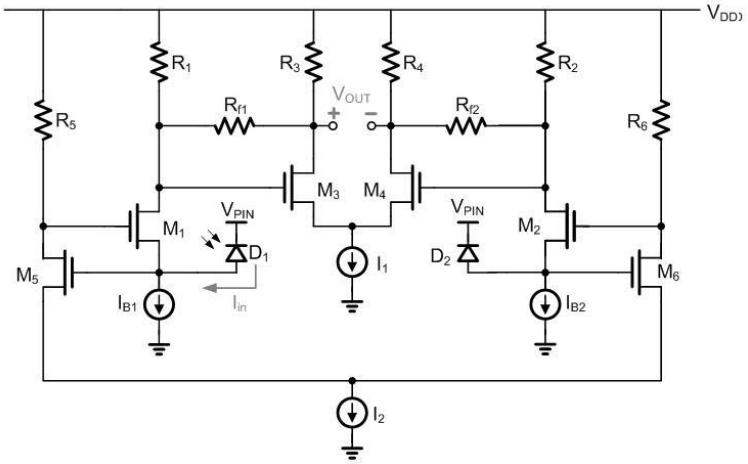
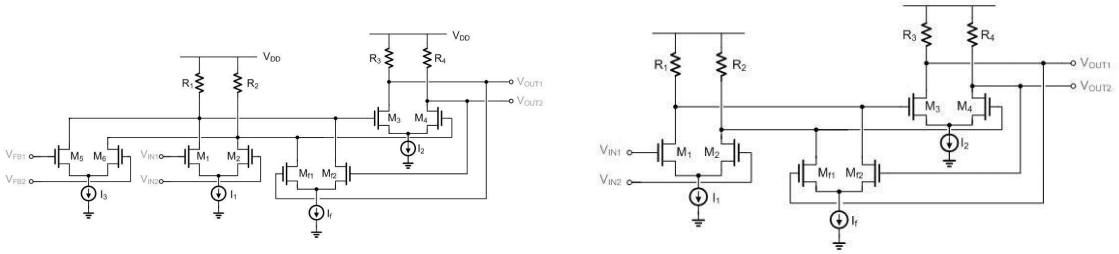


Fig. 3 The circuit topology of the TIA.

The architecture of post LA is shown in the middle of Fig. 2, which is composed of a chain of five gain cells, an offset cancellation circuit, a feedback low pass filter, and a current mode output buffer to drive 50 Ω output loads. To provide a total conversion gain of 50 dB and the gain bandwidth product (GBW) is about 18 dB-GHz per stage in this design.

The input stage and gain cell of the LA is shown in Fig. 4 (a) and Fig. 4 (b) respectively. Both circuits are based on Cherry-Hooper amplifier with active feedback. It has been shown in [7] that the active feedback can increase the GBW of the gain cell beyond the technology f_T. Thus no peaking inductor is needed. The input stage functions as both an input buffer and an offset subtractor. The offset voltage derived from the low pass loop filter is converted to a compensation current and subtracted from the input signal by the source coupled pairs (M_1-M_2) and (M_5, M_6). Finally, a f_T doubler output buffer is adopted as shown in Fig. 5, which is capable of delivering 420 mV V_{PP} to 50 Ω output loads.



(a) (b)

Fig. 4 The (a) input stage and (b) gain cell of the limiting amplifier.

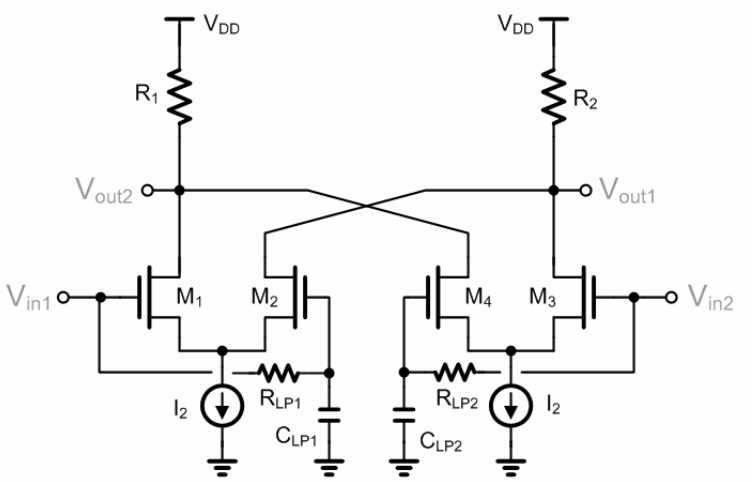


Fig. 5 The topology of the f_T doubler output buffer.

2.2 Optical receiver performance

The chip micrograph is shown in Fig. 6. Fully fabricated in standard 0.18 μm CMOS technology, the total chip area is about 620×860 μm^2. The receiver IC is mounted on a printed circuit board for the measurement. The eye diagrams and the bit error rate performance are characterized by using Agilent N4901B. The pattern generator sends a 2^{31}-1 PRBS test pattern to modulate a 4.25 Gbps 850 nm VECSEL as a light source. The TIA and the post LA are operated under 3.3 V and 1.8 V supply voltages, respectively. The total power dissipation is 138 mW. By cascading TIA and LA on a single chip, the optical receiver provides a conversion gain of 110 dBΩ. However, the overall O-E conversion bandwidth is limited by the PD.

When the PD is reversed bias at the low voltage of 2 V and the high voltage of 6 V, the bit error rate performance is summarized in Fig. 7 (a) and (b) respectively. Under the high voltage operating mode, the input sensitivity level for BER less than 10^{-12} at 622 Mbps, 1.25 Gbps, and 2.5 Gbps are -9.2 dBm, -8.2 dBm, and -4.5 dBm, respectively. Figure 8 shows the measured eye diagram at (a) 622 Mbps and (b) 2.5 Gbps at low-voltage and high voltage modes. The data rms-jitter is about 35.6 ps (peak-to-peak jitter is 248.9 ps) and 34.4 ps (peak-to-peak jitter is 166.7 ps), respectively.

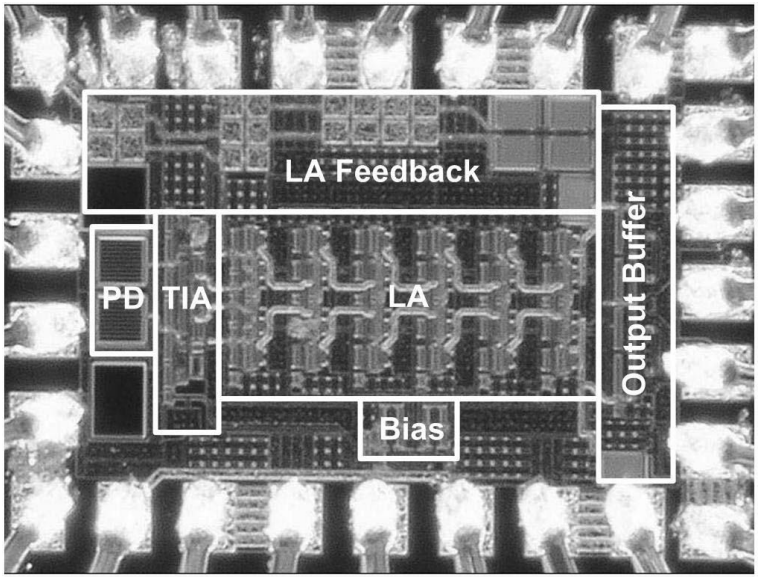
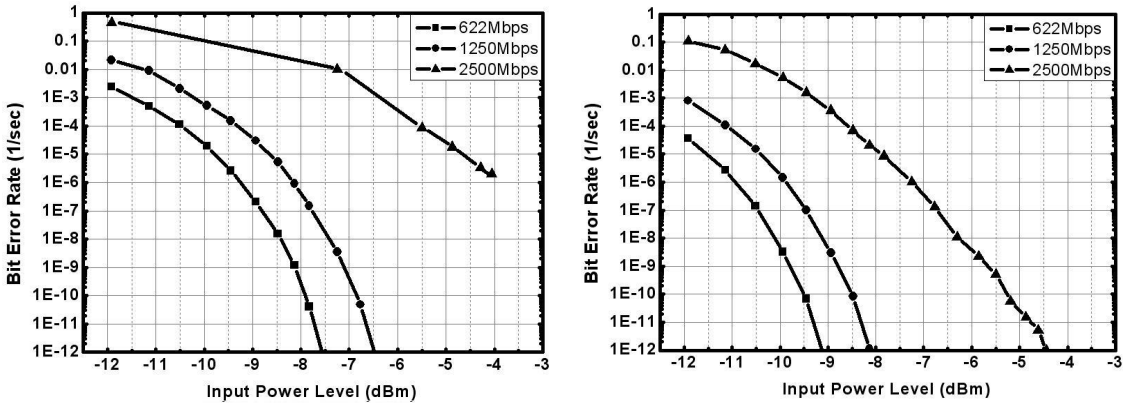
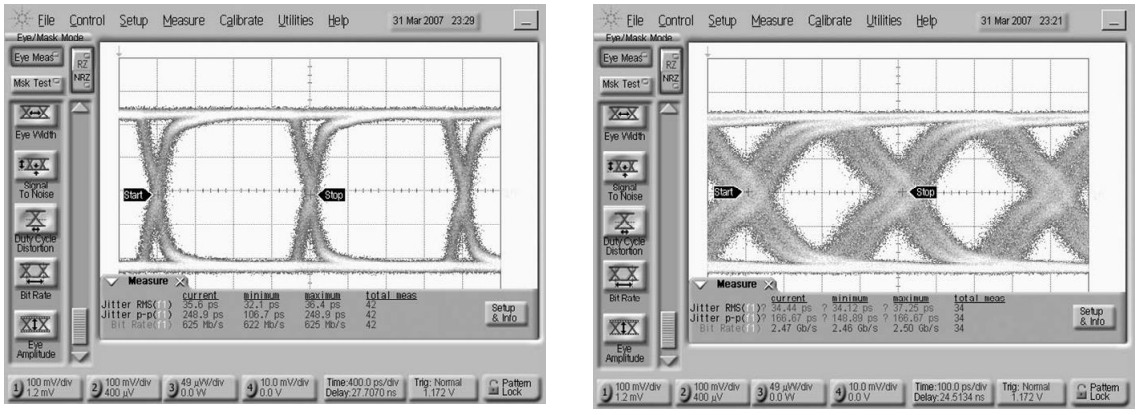


Fig. 6 The micrograph of the optical receiver circuit for the first approach.



(a) (b)

Fig. 7 The measured bit error rate performance with supplied voltage of (a) 2 V and (b) 6 V.



(a) (b)

Fig. 8 The measured eye diagram at data rates of (a) 622 Mbps @ 2V and (b) 2.5 Gbps @ 6V.

3. SML PD DESIGN IN OPTICAL RECEIVER [8]

The SMPD consists of the covered and uncovered PDs by using the light blocking metal [1]-[3]. The covered PD is named dark PD, while the uncovered detector is named illuminated PD. As the photocarriers generated in the neutral regions of the PDs diffuse in all directions, they can be partially eliminated by subtracting the photocurrent collected by the dark detectors (mainly composed of slow carriers) from that of the illuminated PD (composed of both fast drift carriers and slow diffusion carriers). The SMPD is capable of high-speed operation, but at the expense of a relatively smaller responsivity. In this section, three layout topologies of SMPDs are investigated, as are shown in Fig. 9 (a), (c) and (e). Here the illuminated and dark PDs are laid out in cross, strip-line and rectangular shapes. Fig. 9 (b), (d), and (f) respectively illustrate their cross sectional views.

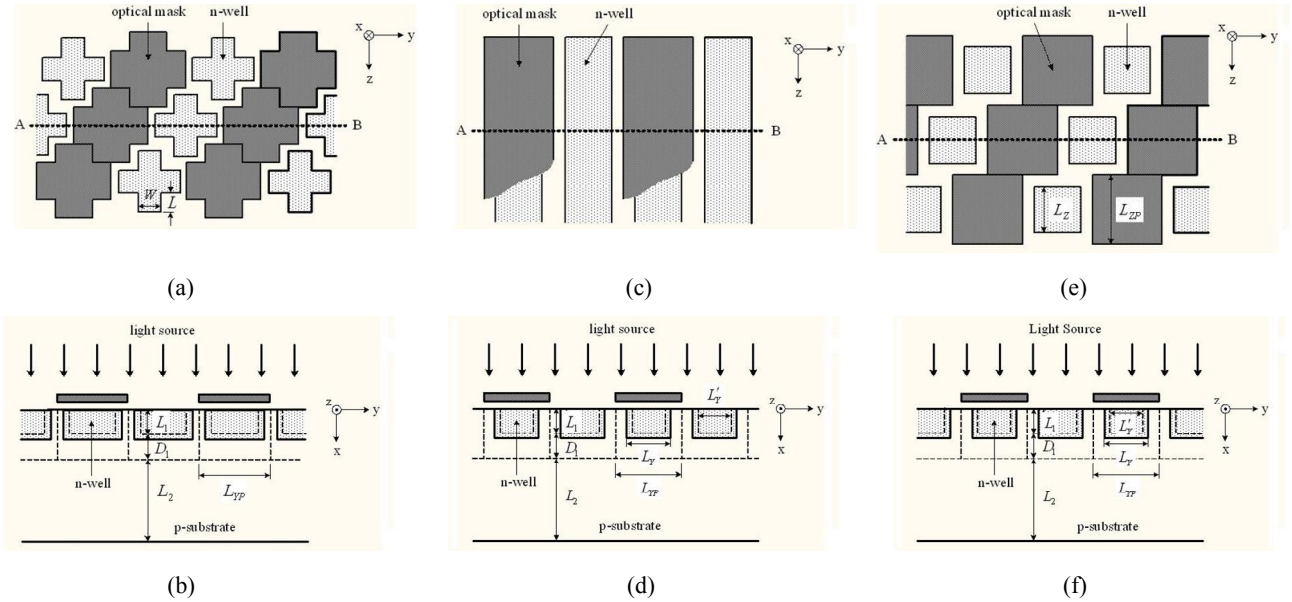


Fig. 9 The layout topologies of SMPDs.

To characterize the performance of the SMPDs, these three detectors are integrated with on chip TIAs for measurement. The experimental results are shown in Fig. 10, which reveals a compromise between the responsivity and bandwidth performance. The measured responsivities of the cross, strip-line, and rectangular PDs are about 0.074 A/W, 0.07 A/W, and 0.029 A/W respectively, while their -3 dB bandwidth are about 240 MHz, 590 MHz, and 1100 MHz.

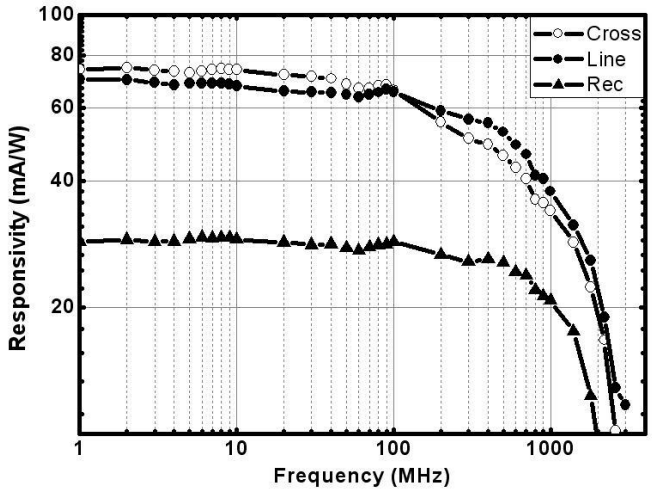


Fig. 10 The measured frequency response of the proposed SMPDs.

Although both the responsivity and bandwidth performance of the strip-line SMPD are in the middle among the three prototypes, it manifests the highest responsivity-bandwidth product. Compared to cross-type, its bandwidth is improved by 2.46 times while its responsivity degrades by less than 5 %. Hence it was selected for the receiver integration in this design.

3.1 Integrated Optical Receiver

The architecture of the optical receiver is shown in Fig. 11, which integrates an on chip SMPD, a TIA, a post LA and output buffer in a single chip. In order to achieve an operating data rate above 3 Gbps, adaptive equalizer is also adopted to compensate the modest frequency response of the SMPD. Besides, due to a relatively low responsivity of the SMPD, no automatic gain control circuit is needed in this design.

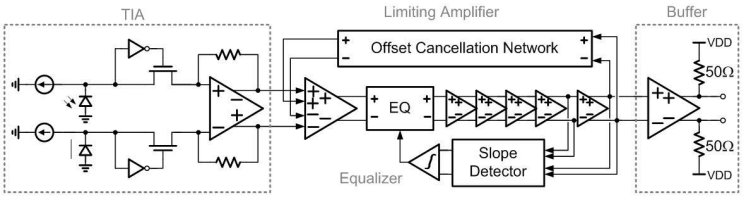


Fig. 11 The architecture of the monolithically optical receiver with on-chip SMPDs.

Fig. 12 illustrates the circuit schematic of the transimpedance amplifier incorporating with the SMPD. It consists of two identical TIAs in a differential configuration as mentioned in section 2.1. The current subtraction is performed in the second stage, which is a common source gain amplifier with shunt-feedback. The slow photocurrent (I_{Dark}) collected by the dark diode is then subtracted from that collected by the illuminated diode (I_{Light}) in the voltage domain.

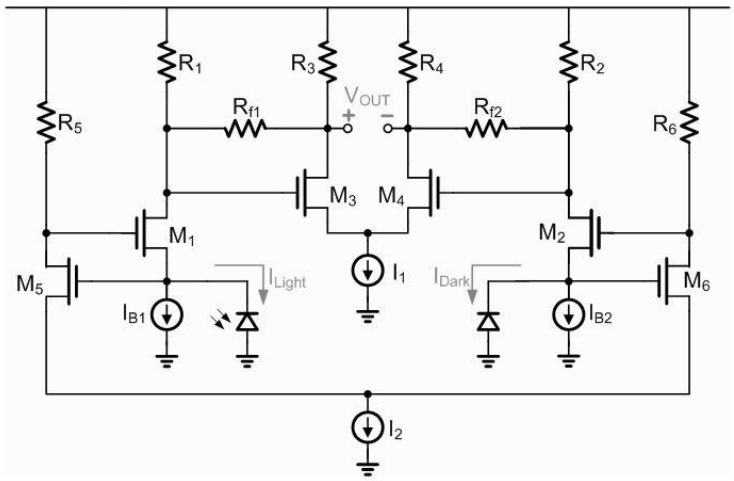


Fig. 12 The circuit topology of the SMPD and TIA.

The architecture of post LA is shown in the middle of Fig. 11. Excluding the input stage for DC offset cancellation, the LA is composed of an adaptive equalizer in the front followed by 5 gain stages. The equalizer provides additional zero to compensate the bandwidth degradation caused by the PD. The zero location is adjusted by a feedback control loop which detects the edge slope of the output waveforms in the last two stages [9]. The -3 dB bandwidth of the post LA is about 3.6 GHz and the total conversion gain is 50 dB.

The core circuit of the gain cell in the LA is mentioned in section 2.1 too. The adaptive equalizer is shown in Fig. 13. In contrast to the other gain cells, it introduces a tunable zero in the transconductance stage of the Cherry-Hooper amplifier. The zero can be adjusted from 400 MHz to 960 MHz, which provides a sufficiently wide range to cover bandwidth variations and fulfill the requirement of high speed operation.

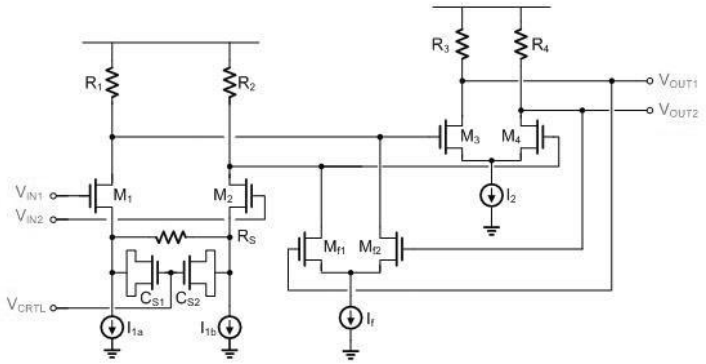


Fig. 13 The circuit topology of the adaptive equalizer.

3.2 Optical receiver performance

The receiver IC is mounted on a printed circuit board for measurement. The measurement setup has been described in section 2.2. The TIA is biased with a 3.3 V supply to provide a sufficient reverse voltage for the PD, while the LA is operated under a single 1.8 V supply. The total power dissipation is 175 mW. By cascading TIA and LA on a single chip, the optical receiver provides a conversion gain of 110 dBΩ. The overall f_{-3dB} is about 2.46 GHz, which is limited by the PD. It is capable of delivering 420 mVpp differential voltage swings to 50 Ω output loads directly.

The bit error rate performance is summarized in Fig. 14. As the responsivity of the PD is only about 70 mA/W, the input sensitivity level for BER less than 10^{-12} at 625 Mbps, 1.25 Gbps, 2.5 Gbps, and 3.125 Gbps are about -7.5 dBm, -7.0 dBm, -5.8 dBm, and -4.2 dBm respectively.

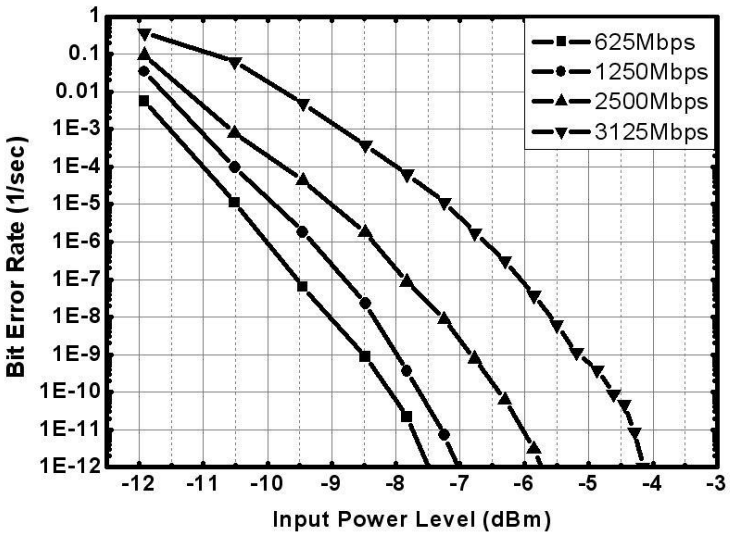


Fig. 14 Measured bit error rate performance of the optical receiver.

Fig. 15 shows the measured eye diagram at 3.125 Gbps at the input sensitivity level. The data rms-jitter is about 16.86 ps and peak-to-peak jitter is 120.89 ps. The chip micrograph is shown in Fig. 16 and implemented in standard 0.18 μm CMOS technology; the total chip area is about 710×990 μm^2. The area of PD is 65×65 μm^2 to comply with the diameter of the multi-mode fiber.

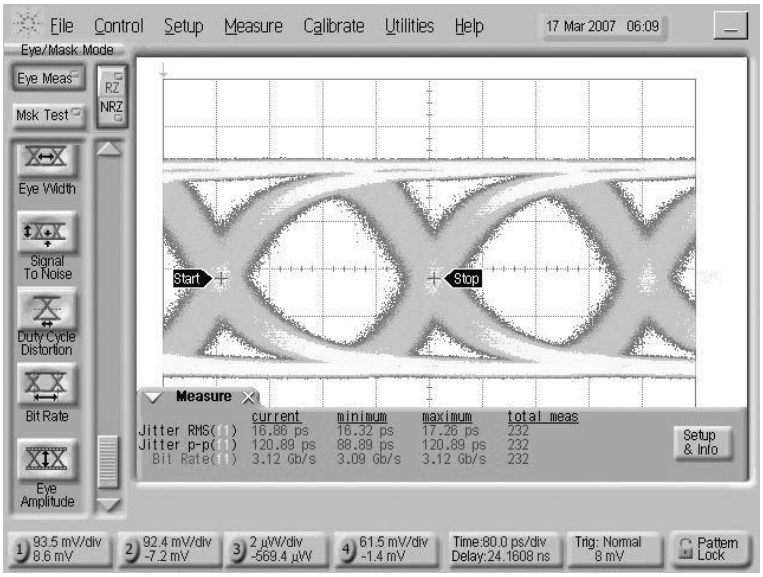


Fig. 15 The measured eye diagram at 3.125 Gbps.

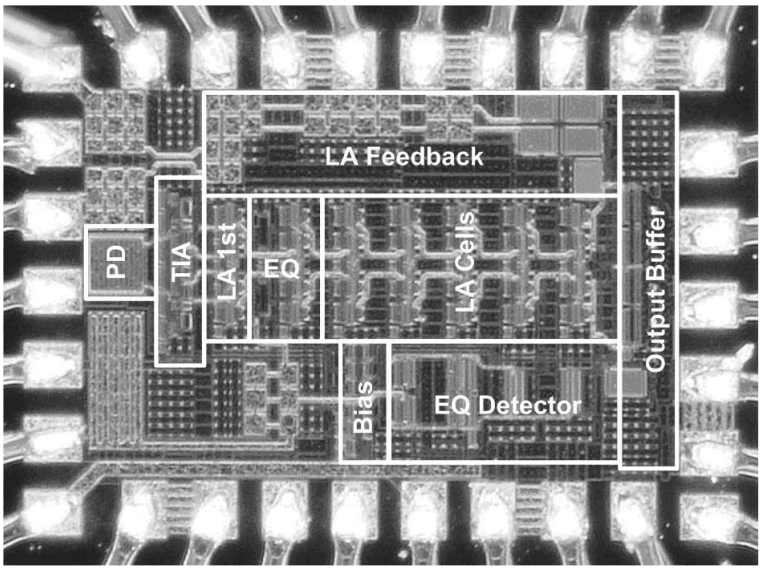


Fig. 16 The micrograph of the optical receiver circuit for the 2nd approach.

4. PD WITH BODY CONTACT DESIGN [10]

In this section, a novel structure of PD which eliminates the diffusion photocarriers effectively in CMOS is proposed. The inset in Fig. 17 shows a 3-D schematic structure of the proposed PD. The basic diode structure of the proposed Si PD is fabricated by standard 0.18-μm CMOS technology without any process modification. The n-well, p-well, shallow trench isolation (STI) oxide, and source/drain implant (S/D implant) from standard CMOS process are used to implement the basic multiple p^+-p-n PD structure [11]. The designed p-implant and p-well form deeper and higher p-type doping in p-region. In addition, by using STI oxide, it not only improves the breakdown voltage but also extends the depletion region. Accordingly, it would improve the responsivity. The designed body contact is around the device and connected to substrate through p-implant and p-well. And the body contact metal is also the shaded metal to prevent from the unnecessary illumination into the substrate to generate more slow diffusion carriers.

The total dimension of this PD is 50×50 μm^2, which consists of 22 p-regions and 23 n-regions. The width for p-well (W_P), n-well (W_N), STI oxide (W_{STI}), body region (W_B) and contact metal strip is 1.4, 0.86, 0.36, 5.6 and 0.45 μm respectively.

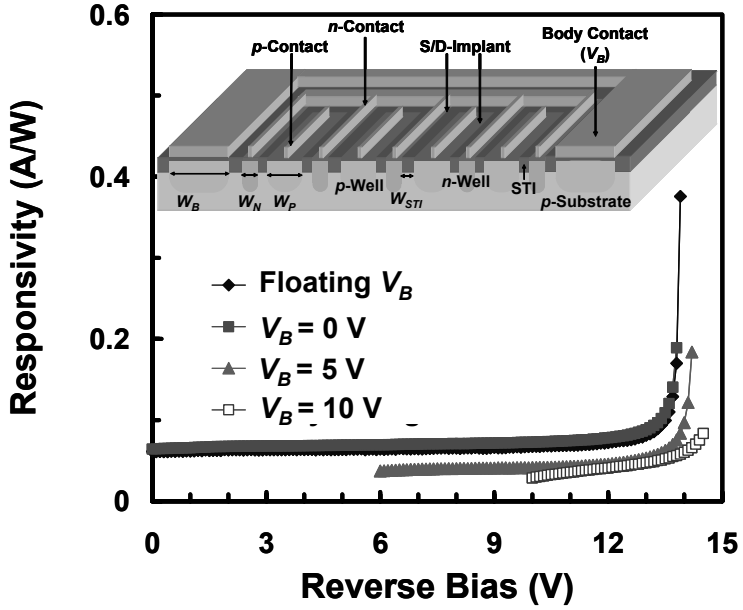


Fig. 17 The measured responsivity of the proposed PD with different V_B conditions. The inset shows a 3-D schematic structure of the proposed PD.

The DC characteristic of fabricated PD is similar to a standard Si p-n junction diode with turn-on voltage of 0.8 V (> 2 mA) and breakdown voltage of 14.2 V (at 100 μA). Figure 17 shows the measured responsivity versus reverse bias (V_R) of the proposed PD with different body voltages (V_B) includes floating, 0 V, 5 V and 10 V. The measurement range of V_R is limited by the supplied V_B due to the turning on between body region and n-regions. The photocurrent is measured by illuminating a continuous laser with wavelength of 823 nm and optical power of 380 μW. The PD with floating V_B shows a responsivity of 0.061 A/W at zero bias. At V_R of 13.9 V (dark current, I_{DARK} < 1 μA), a higher responsivity of 0.38 A/W is observed from impact ionization.

As the body contact V_B is 0 V, the electric potential of substrate is equivalent to 0 V and slightly better responsivity (0.064 A/W) is observed. By further increasing V_B the responsivity is decreased. The supplied V_B creates a current path from body contact, through the substrate, to the p-contact (ground). At the same condition, the current at the n-region shows reversed diode characteristics with breakdown voltage increased to 15.1 V. Since the electric potential of substrate from the supplied V_B screens the V_R at the interface of n-well and substrate, this results in decreasing the depth of the depletion region and collecting less diffusion carriers from substrate.

In the pulse measurement, a pulse laser with wavelength of 823 nm and pulse width around 50 ps is used to measure the optical pulse response to investigate the slow carriers of the PD. The PD is biased through a bias-T, which in turn is connected to Agilent DSO80604B oscilloscope to record the waveform and the parameters of pulse responses includes rise time, fall time and full width at half maximum (FWHM). The inset in Fig. 18 shows the pulse responses of different V_B conditions while PD is operated in avalanche region (I_{DARK} < 1 μA). In Table I, it summarizes the pulse responses. The rise time is improved from 78 ps (floating V_B) to 67 ps (V_B = 10 V), the FWHM is improved from 140 ps (floating V_B) to 118 ps (V_B = 10 V) and the fall time is improved from 108 ps (floating V_B) to 73 ps (V_B = 10 V). Especially in the improvement of the fall time, the original long tail from the PD with floating V_B is significantly eliminated when the PD with body contact V_B of 10 V. And the difference between the rise time and fall time is very close. It indicates the most of the slow carriers are generated from substrate and can be swept into designed current path.

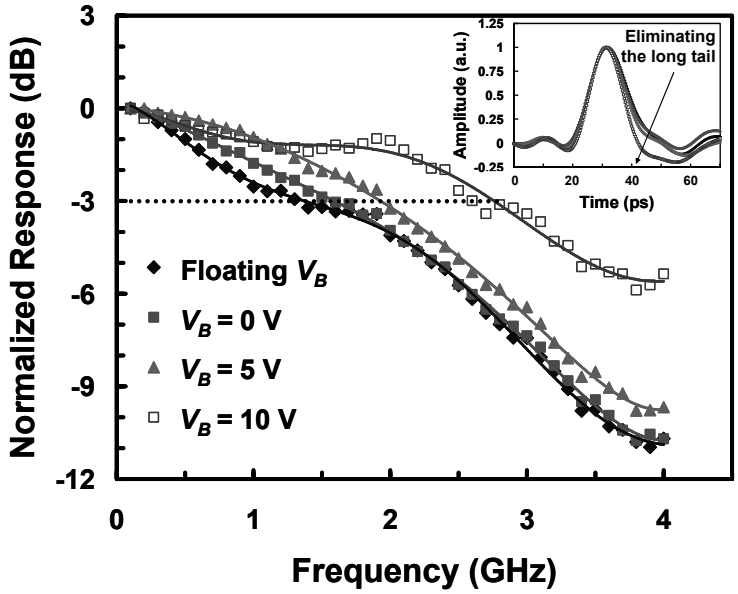


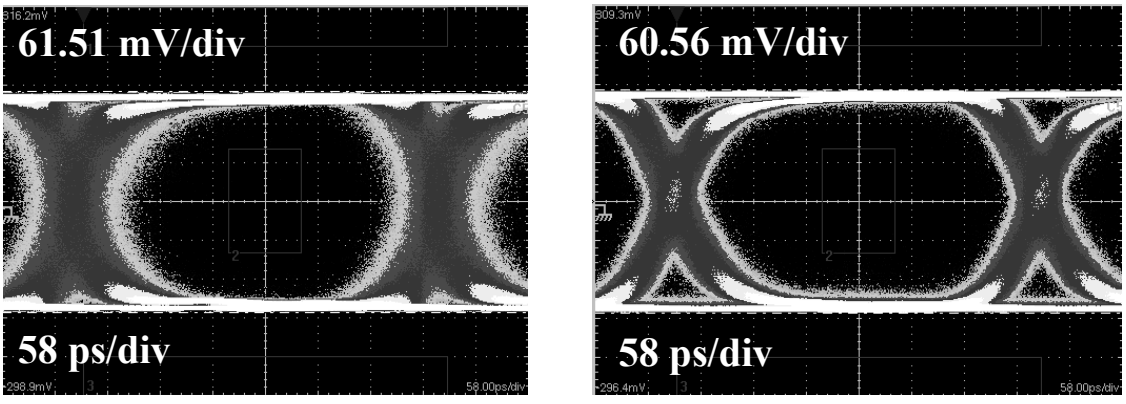
Fig. 18 The normalized frequency responses of PD with different V_B conditions. The inset shows the pulse responses with different V_B conditions when the PD is operated in avalanche region (I_{DARK} < 1 μA).

Table 1. Summary of the pulse responses with different V_B conditions

	Floating V_B	V_B = 0 V	V_B = 5 V	V_B = 10 V
FWHM (ps)	140	134	130	118
Rise Time (ps)	78	75	72	67
Fall Time (ps)	108	112	100	73

Figure 18 shows the normalized frequency responses of PD with different V_B conditions. It shows the -3 dB bandwidth is improved from 1.4 GHz (floating V_B) to 2.8 GHz (V_B = 10 V) with 100 % improvement. From the elimination of the long tail as observed in pulse response, the created current path takes effect and causes the bandwidth enhancement successfully.

The eye diagrams of PDs are measured and compared between floating V_B and V_B of 10 V as shown in Fig. 19 (a) and (b), respectively.



(a) (b)

Fig. 19 The eye diagrams which are measured with cable connected 10 Gbps TIA at data rate of 2.5 Gbs are compared between (a) floating V_B and (b) V_B of 10 V.

The measurement was carried out on PDs with RF cable connected 10 Gbps commercial TIA when optical power is -1 dBm at data rate of 2.5 Gb/s. These two eye diagrams all meet the masks of SONET OC-48. And the eye width and the peak-to-peak jitter are improved from 274 ps to 324 ps and from 172 ps to 122 ps, respectively. Finally the eye diagrams at higher data rates of 4 Gb/s and 5 Gb/s are demonstrated in Fig. 21 (a) and (b) to illustrate the capability of the proposed PD.

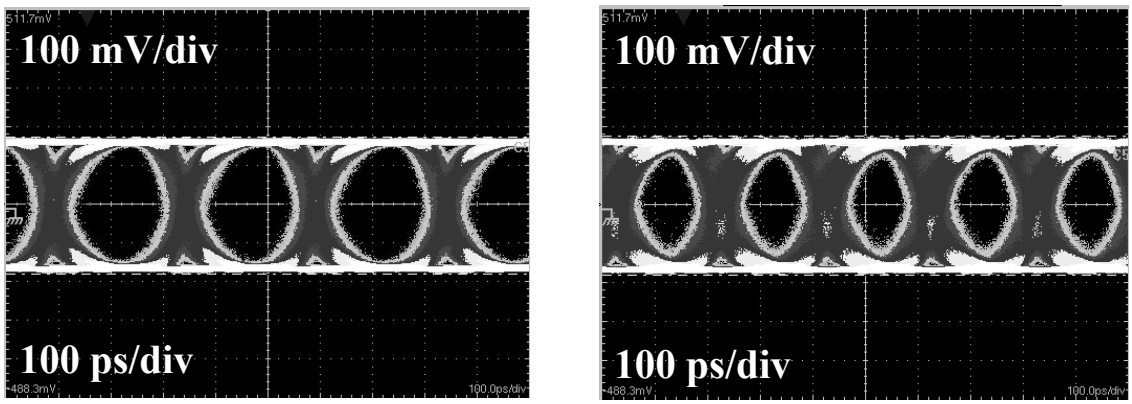


Fig. 20 The eye diagrams at higher data rates of (a) 4 Gb/s and (b) 5 Gb/s when the supplied V_B is 10 V.

4.1 Optical Receiver Performance

The monolithically integrated OEIC design in 0.18 μm CMOS technology which is based on the experience of previous designed PD is proposed in this section. The PD with body contact design is combined with TIA in this OEIC. In order to reduce the C_{PD} and achieve higher data rate operation, the active region of PD is decreased from 50×50 μm^2 to 20×20 μm^2. Except for reduced C_{PD}, the enlarged n-contact metal is used to shade n-region to prevent from the generation of slow holes and increase the response time.

The TIA consists of four stages. The first stage is common gate amplifier which has advantages of lower input resistance to decrease the effect from C_{PD} and lower noise figure to increase the sensitivity of the circuit. The following is three stages inverter amplifiers to amplify the signal. Furthermore, the feedback resistance is used to enlarge the bandwidth. The total area of this OEIC is 560×560 μm^2. The TIA with V_C = 2.0 V, V_D = -1.8 V and V_{PD} = -12.86 V demonstrates a transimpedance gain of 47 dBΩ and a bandwidth of 5.5 GHz. The measured O-E conversion frequency response of the optical receiver with different V_{PD} is shown in Fig. 21. Through the increased reverse bias, the O-E conversion -3 dB bandwidth of the optical receiver is increased from 1.05 GHz (V_{PD} = -3 V) to 3.8 GHz (V_{PD} = -13.06 V).

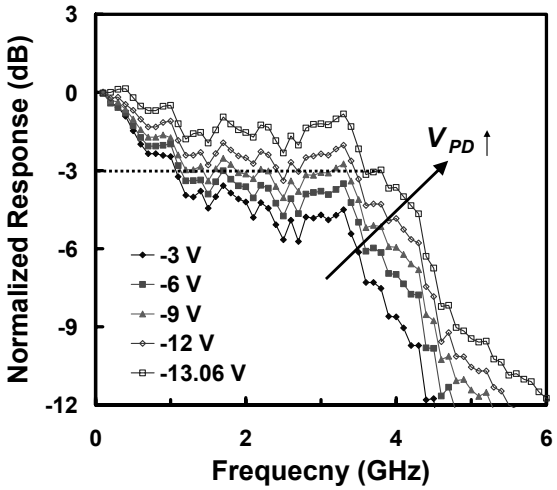


Fig. 21 The measured frequency response of the OEIC with different V_{PD}.

With increased V_{BP} (voltage difference between V_B and V_{PD}), the bandwidth is increased from 3.8 GHz (V_{BP} = 0V) to 4.3 GHz as shown in Fig. 22. This result shows the body current really takes effect on the PD and enhances the OEIC overall performance successfully. These results also verify the feasibility of high data rate monolithically integrated OEIC in standard CMOS technology.

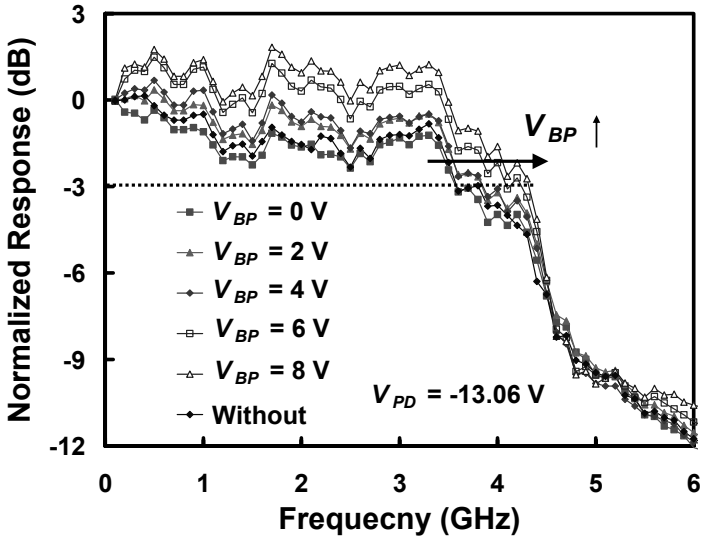


Fig. 22 The measured frequency response of the OEIC with different V_{BP}.

5. CONCLUSION

In this work, different Si PD structures are proposed to implement high speed optical receivers in standard bulk 0.18 μm Si CMOS technology. The designed block well in lateral p-i-n PD limits the photocarriers being mainly generated from the laterally depleted regions. The SMPD with -3 dB bandwidth of 590 MHz is integrated in optical receiver with adaptive analog equalizer and demonstrates a data rate of 3.125 Gbps. These two OEIC's demonstrate higher sensitivity as well as operating speed compared to the prior art [2].

Finally, the body contact design in PD eliminates the slow diffusion photocarriers by creating a new current path under the PD. A highest bandwidth of 2.8 GHz with 100 % improvement is obtained. The eye diagrams of PD with cable connected amplifiers at 2.5 Gbps, 4 Gbps and 5 Gbps are demonstrated. Furthermore, the O-E conversion bandwidth of the optical receiver is also increased from 3.6 GHz to 4.3 GHz. To our knowledge, these are the fastest Si PD and optical receiver fabricated by standard bulk CMOS process ever reported. And these superior results also lead to the possibility of 850nm Si OEIC applied to high data rate optical communication system.

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