A Sub-mW All-Digital Signal Component Separator With Branch Mismatch Compensation for OFDM LINC Transmitters

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***Abstract*—Linear amplification with nonlinear components (LINC) is an attractive technique for achieving linear amplification with high efficiency. This paper presents a sub-mW all-digital signal component separator (SCS) design for OFDM LINC transmitters, including a phase calculator and a digital-control phase shifter (DCPS) pair. In addition, a digital mismatch compensation scheme is proposed and integrated into the SCS to reduce the design complexity of the power amplifier. This chip is manufactured in a 90 nm standard CMOS process with an active area of 0.06 mm^2. The DCPS can generate phase-modulated signals at 100 MHz with 8-bit resolution and RMS error 9.33 ps (0.34°). The phase calculation can be performed at a maximum speed of 50 MHz using a 0.5 V supply voltage, resulting in a 73.88% power reduction. Comparing to state-of-the-art, the power consumption of the overall SCS is only 949.5 μW which minimizes the power overhead for an LINC transmitter. This SCS with the branch mismatch compensation provides a 0.02 dB gain and 0.15° phase fine-tune resolution without adding additional front-end circuits. Considering 1 dB gain and 10° phase mismatch, the system EVM of −29.81 dB and ACPR of −34.56 dB can still be achieved for 5 MHz bandwidth 64-QAM OFDM signals.**

***Index Terms*—Branch imbalance, efficiency, LINC, mismatch, OFDM, outphasing, SCS.**

I. Introduction

ORTHOGONAL frequency division multiplexing (OFDM) is an attractive technique for robust and high-speed data transmission in the multipath fading channel, and has been applied for several broadband wireless applications such as wireless local area networks (WLANs). However, OFDM signals suffer from large envelope variations when a number of independently modulated subcarriers are summed coherently. To avoid distortion during the amplification, the linear power amplifier (PA) is required to back off the operation point, resulting in considerable efficiency degradation. Accordingly, the transmitter is required to dissipate more DC power to achieve a specified transmitted power level. Linear amplification by nonlinear components (LINC) [1], also called outphasing [2], has been proposed to maintain the PA efficiency along with high quality linearity. As shown in Fig. 1, the basic concept of LINC involves converting the phase-and-amplitude-modulated signal to two phase-only-modulated signals by a signal component separator (SCS), which is then amplified using two high efficiency nonlinear PAs. Finally, the original signal can be reconstructed by combining these two amplified signals.

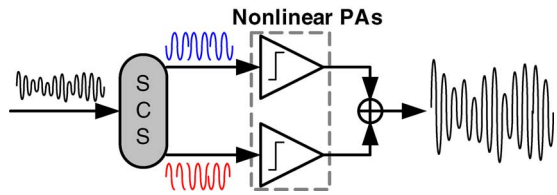

Fig. 1. LINC schematic.

Although LINC can improve the amplification efficiency, it requires an additional function block, SCS, and the power overhead and separation accuracy become additional design challenges. To separate accurately, digital implementation [3], [4] is assumed the most favorable choice. However, an LINC transmitter with the digital baseband SCS requires four digital-to-analog converters (DAC), and both digital calculations and DACs are operated with higher frequency due to the nonlinear separation process [5], resulting in considerable power dissipation. Several analog designs have been proposed to reduce power consumption [6]–[8], but demonstrate difficulty realizing accurate nonlinear mathematical functions and are sensitive to operation conditions. In addition, those published chips still cost tens-mW-order power consumption, a significant overhead for the transmitter. This work presents a sub-mW and all-digital SCS design for LINC transmitters. Instead of four DACs, this paper proposes two digital-control phase shifters (DCPS) with an automatic calibration to generate the phase-modulated signals. To reduce the digital signal processing (DSP) power, this chip can be globally operated at 0.5 V to save a large amount of power dissipation. Therefore, the proposed SCS solution can achieve both accurate separation and low power consumption for LINC transmitters.

Another limitation of LINC is the tight tolerance of the branch imbalance, resulting in unacceptable out-of-band radiation and in-band signal quality. The system requirements have been discussed by several authors [9], [10]. Approximate gain imbalance of 0.3–0.4 dB and phase imbalance of 2–3° can still be

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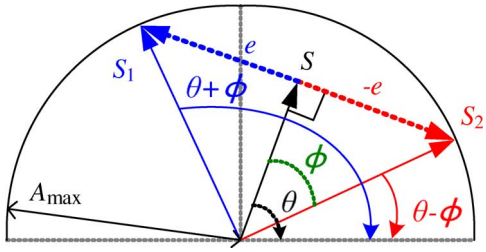

Fig. 2. Vector representation of the SCS.

tolerated, but are nearly impossible for practical implementations. Fortunately, several calibration schemes have been proposed to detect the gain and phase mismatch information accurately by digital processing [10], [11]; the mismatches can then be compensated for before the normal transmission. The phase mismatch can be compensated for by DSP functions or by adding delays to another branch. However, changing the magnitude before a nonlinear PA is useless because only the phase information can be recognized. Adding a high-resolution, gain adjustable capability for PA is required, resulting in higher design complexity and more efficiency loss. Accordingly, a compensation method to balance both gain and phase mismatches by assigning specified phases only is proposed [12], [13]. This work provides more performance analysis and integrates the digital compensation scheme in the SCS, extending the mismatch tolerance and reducing PA design complexity.

This paper is organized as follows. Section II introduces the basic LINC principle and the proposed SCS operation. In Section III, the branch mismatch compensation scheme in the SCS is provided. Chip implementation details are then described in Section IV. Section V shows the chip experimental results and performance comparisons, followed by the conclusion in Section VI.

II. LINC SCS Overview

A. SCS Principle

Denote the baseband signal as $S_b(t) = S_i(t) + jS_q(t)$, then the transmitted signal can be generally expressed as

$$S(t) = \mathrm{Re}\left\{(S_i(t) + jS_q(t))\, e^{jw_c t}\right\} = A(t)\cos\left(w_c t + \theta(t)\right) \tag{1}$$

where $A(t)$ and $\theta(t)$ are the envelope and phase given by

$$A(t) = \sqrt{S_i^2(t) + S_q^2(t)} \tag{2}$$

and

$$\theta(t) = \tan^{-1}\left(S_q(t)/S_i(t)\right) \tag{3}$$

respectively. Fig. 2 shows the vector representation of the separation process. One of the separation methods involves calculating the quadrature vector $e(t)$ by the following equation:

$$e(t) = -jS_b(t)\sqrt{\frac{A_{\max}^2}{A^2(t)} - 1} \tag{4}$$

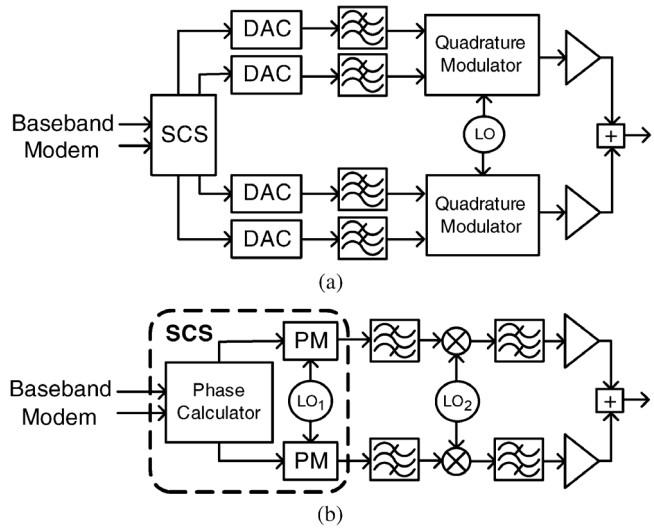

Fig. 3. LINC transmitter architecture with the digital SCS. (a) Direct up-conversion with baseband SCS. (b) Two-stage up-conversion with the phase-modulated based SCS.

where $A_{\max}$ is the peak amplitude of the signal envelope. The original baseband signal can then be expressed by the summation of two constant-envelope signals $S_{1b}(t)$ and $S_{2b}(t)$:

$$\begin{aligned} S_{1b}(t) &= 0.5\left(S(t) + e(t)\right) \\ S_{2b}(t) &= 0.5\left(S(t) - e(t)\right). \end{aligned} \tag{5}$$

Another separation type is the phase-modulated method. The signal $S(t)$ can be separated into two phase-modulated signals $S_1(t)$ and $S_2(t)$:

$$\begin{aligned} S_1(t) &= 0.5A_{\max}\cos\left(w_c t + \theta(t) + \phi(t)\right) \\ S_2(t) &= 0.5A_{\max}\cos\left(w_c t + \theta(t) - \phi(t)\right) \end{aligned} \tag{6}$$

where

$$\phi(t) = \cos^{-1}\left(A(t)/A_{\max}\right). \tag{7}$$

Because these two signals contain only phase information, they can be generated by two phase modulators (PMs) directly with the calculated phases, $\theta(t) + \phi(t)$ and $\theta(t) - \phi(t)$.

B. Proposed LINC System

The quadrature signal $e(t)$ can be calculated by a digital implementation with excellent accuracy, and the architecture is shown in Fig. 3(a). After separation in the SCS, two DACs and a quadrature modulator are used on each branch to transfer the digital SCS outputs from digital to analog domains and then up-converted to the radio frequency. However, the LINC system performance is sensitive to the I-Q mismatch and the DC offset of the nonideal quadrature modulators [14]. Therefore, the phase-modulated method is adopted in this work to avoid the need for nonideal quadrature modulators. The proposed LINC architecture with the digital SCS is shown in Fig. 3(b). The phases are calculated by the digital phase calculator and then through a digital-control PM pair. Note

that both quadrature modulators and DACs are not required in the proposed architecture. To achieve low power consumption with adequate phase resolution, this work proposes using two-stage up-conversion architecture. Instead of up-converting to the radio frequency directly, the phase-modulated signals are first generated by a digital-control PM pair at an intermediate frequency (IF) 100 MHz. These two output signals can then be up-converted to the desired radio frequency by two up-mixers. Finally, the signals can be amplified by two efficient PAs and then recombined.

Based on the OFDM-based baseband modem of our previous work for the wireless body area network (WBAN) application [15], a QPSK 64-point OFDM signal with 5 MHz bandwidth is adopted as the signal source in this paper. For performance comparisons and more general applications, the IEEE 802.11a/g 64-QAM 64-point OFDM signal format, having a stricter requirement for the transmitted signal quality, is also considered as the baseband input, except for the 1/4 scaled bandwidth in the following evaluations. Furthermore, the system specification is also referred to the standard, such as the error vector magnitude (EVM) -25 dB and the adjacent-channel power ratio (ACPR) -27 dB.

Because $S_1(t)$ and $S_2(t)$ are constant-envelope signals, the required bandwidth is much larger than the original baseband signal (more than $8\times$) [5]. Assuming the baseband signal is interpolated before the signal separation, the proposed digital phase calculator can be operated at a maximal 50 MHz, implying that the SCS outputs with 50 MHz bandwidth ($10\times$ the original signal bandwidth) can be obtained.

III. Branch Mismatch Compensation

The branch mismatch (including gain mismatch ΔG and phase mismatch $\Delta\phi$) introduces unacceptable in-band and out-band distortions [10]. Accordingly, several methods have been proposed to detect such mismatches [10], [11]. By sending specified testing patterns and adding a low-cost feedback down-converting path, the mismatch information can be calculated by simple digital process. The mismatch can then be eliminated by multiplying a complex scaling in a digital domain. However, scaling the signal magnitude for gain compensation only applies to linear PAs. To achieve higher amplification efficiency, LINC often chooses switching-mode PAs, but such PAs can only recognize the phase information. An extra high-resolution gain adjustment, such as a tunable supply voltage or bias voltage, is required, increasing the hardware cost and power dissipation. Consequently, this work proposes an SCS with a mismatch compensation capability, as shown in Fig. 4. Assuming the mismatch values can be detected accurately, this work integrates a digital compensation scheme with high tuning resolution into the SCS to balance both gain and phase mismatches by assigning specified phases, such that the PA mismatch tolerance can be extended and design complexity can be reduced.

To compensate for the phase mismatch caused by imbalanced FE circuits and PAs, a tunable delay chain on each branch is added to generate a specified delay difference in the SCS. According to a phase mismatch $\Delta\phi$, we add a specified codeword offset on one of the delay chains to generate a delay difference

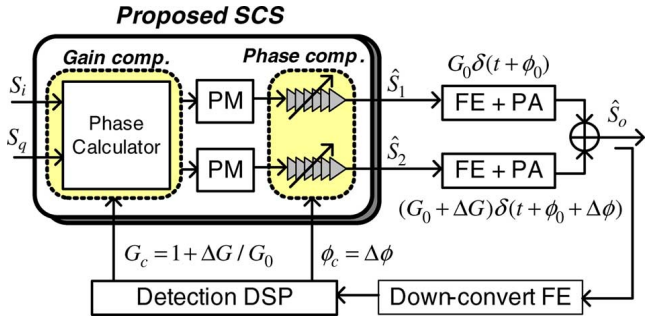

Fig. 4. Proposed SCS design with the branch mismatch compensation capability.

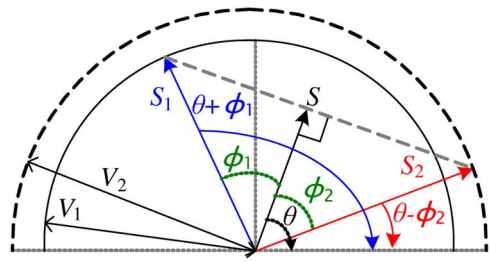

Fig. 5. Vector representation of the SCS with the gain compensation ($V_1 = A_{\max}, V_2 = A_{\max}G_c$).

$\phi_c = \Delta\phi$ between these two delay chains. Then the summation of the phase delays caused by the SCS, FE circuits, and PA on both branches can be balanced completely. Using Fig. 4 as an example, the phase delay of the lower branch is longer than that of the upper branch with $\Delta\phi$ difference; therefore, we can assign a larger codeword of the upper delay chain to introduce a longer delay to the SCS.

For gain compensation, the gain mismatch information provides feedback to the phase calculator and is balanced by assigning the specified phases. First, the representation of $S_1(t)$ and $S_2(t)$ in (6) is modified by adding two phase variables $\phi_1(t)$ and $\phi_2(t)$:

$$\begin{aligned} S_1(t) &= 0.5A_{\max}\cos\left(w_c t + \theta(t) + \phi_1(t)\right) \\ S_2(t) &= 0.5A_{\max}\cos\left(w_c t + \theta(t) - \phi_2(t)\right). \end{aligned} \tag{8}$$

Denote the gain ratio of two branches denoted as $G_c = 1 + \Delta G/G_0$; the gain mismatch problem can then be considered during the signal separation to satisfy the following quality:

$$S_1(t) + G_c S_2(t) = S(t). \tag{9}$$

The vector representation of (9) is shown in Fig. 5. Defining $V_1 = A_{\max}$ and $V_2 = A_{\max}G_c$, we can obtain following equations:

$$\begin{cases} V_1\cos\phi_1(t) + V_2\cos\phi_2(t) = 2A(t), \\ -V_1\sin\phi_1(t) + V_2\sin\phi_2(t) = 0. \end{cases} \tag{10}$$

By solving the equation, the closed-form expression of $\phi_1(t)$ and $\phi_2(t)$ can be derived:

$$\begin{aligned} \phi_1(t) &= \cos^{-1}\left(\frac{V_1^2 + 4A^2(t) - V_2^2}{4A(t)V_1}\right) \\ \phi_2(t) &= \cos^{-1}\left(\frac{V_2^2 + 4A^2(t) - V_1^2}{4A(t)V_2}\right). \end{aligned} \tag{11}$$

Denote $\hat{S}_1(t)$ and $\hat{S}_2(t)$ as the signals after both gain and phase mismatch compensation:

$$\begin{aligned}\hat{S}_1(t) &= 0.5A_{\max}\cos\left(w_c t + \theta(t) + \phi_1(t) + \phi_c\right)\\ \hat{S}_2(t) &= 0.5A_{\max}\cos\left(w_c t + \theta(t) - \phi_2(t)\right).\end{aligned} \tag{12}$$

The amplified signal with the proposed compensation denoted as $\hat{S}_o(t)$ can then be verified:

$$\begin{aligned}\hat{S}_o(t) &= G_0\hat{S}_1(t+\phi_0) + (G_0+\Delta G)\hat{S}_2(t+\phi_0+\Delta\phi)\\ &= G_0\left[S_1(t+\phi_0+\phi_c) + G_c S_2(t+\phi_0+\Delta\phi)\right]\\ &= G_0 S\left(t+\phi_0^*\right),\end{aligned} \tag{13}$$

which is the desired signal with a constant delay $\phi_0' = \phi_0 + \Delta\phi$. Therefore, the branch mismatch can be balanced by the proposed SCS design.

The only limitation of our compensation scheme is that the gain compensation occurring on signal magnitude $A(t)$ is less than $|V_2 - V_1|$; but the mismatch effect can still be minimized by setting two vectors in opposite directions. If $V_2 > V_1$, we can set $\phi_1 = \pi$ and $\phi_2 = 0$. Similarly, we set $\phi_1 = 0$ and $\phi_2 = \pi$ when $V_1 > V_2$. The remaining error signal is then $(|V_2 - V_1| - A(t))e^{j\theta(t)}$. Fig. 6 and Fig. 7 show the system EVM and ACPR for 8-bit quantized 64-QAM OFDM signals with gain mismatch effect, respectively. To satisfy the specification, the EVM performance is the main limitation. The performance is almost identical to the ideal case when the gain mismatch is less than 0.7 dB, and the tolerance can be extended from 0.4 dB to 2 dB without violating the specification by applying the proposed compensation scheme.

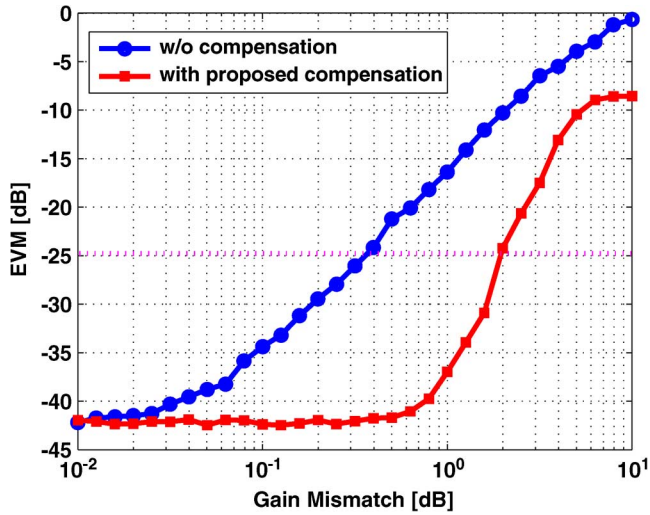

Fig. 6. EVM performance with the gain mismatch effect.

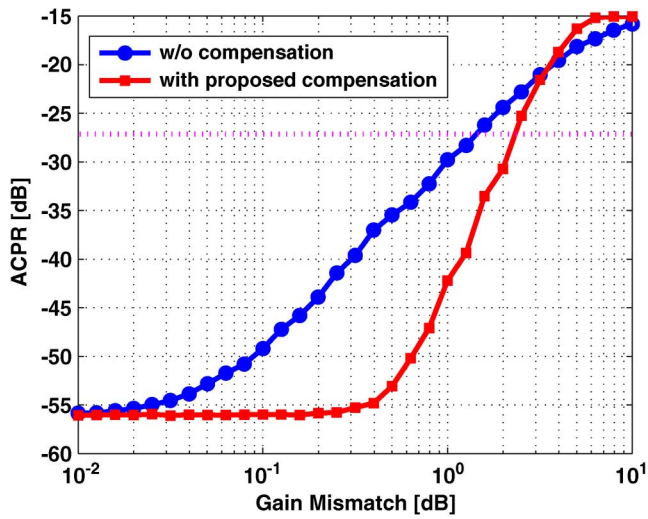

Fig. 7. ACPR performance with the gain mismatch effect.

IV. Chip Implementation

Fig. 8 presents the chip block diagram and detailed signal paths. The source signal from the baseband modem is 10× interpolated and quantized to 8 bits before the SCS. The phase calculator then receives the baseband source and calculates the 8-bit phase codeword P_1 and P_2 with 50 MHz operation speed. The mapper is then used to transfer the 8-bit phase codewords to 14-bit control codewords for the DCPS, which behaves as a PM to generate the phase-modulated signal at 100 MHz.

The register file is used to store some parameters and gain mismatch information that are assumed to be decided before system operation. With the branch mismatch values, the phase calculator and the DCPS can provide high-resolution gain and phase compensation capability, respectively. Furthermore, another PVT register is used to store the required parameters detected by an embedded automatic calibrator for the DCPS mapper.

A. Power Domain Partitions and Voltage Scaling

Due to the high operation speed of DSP functions, the dynamic power proportional to the operating frequency is significant. This work applies the voltage scaling scheme on all DSP functions to reduce the power dissipation. To achieve low power and accurate SCS simultaneously, this chip is partitioned into two independent power domains with different supply voltages. As shown in Fig. 8, the default domain uses 1.0 V to interface with IO pads, and the DCPS pair also uses 1.0 V to achieve accurate results. All DSP functions, including the phase calculator, codeword mappers, registers, and controller, are operated with 0.5 V supply voltage to save power consumption. Level shifters are added on all paths that cross the 0.5 V domain to the default domain.

To apply the voltage scaling scheme in the standard-cell-based design procedure, the cell behavior and timing information under 0.5 V supply voltage are simulated and re-calibrated. The cell library is reconstructed after picking out the cells that can work normally. With the reconstructed 0.5 V cell library, the proposed SCS design can be implemented by exploiting a standard-cell-based design procedure to ensure that the circuit is reliable.

B. Phase Calculator

The phase calculator realizes the nonlinear mathematical calculations of the $\theta(t)$, $\phi_1(t)$, and $\phi_2(t)$ which are described in the previous sections. For the gain compensation, this work uses 10 bits to express the gain mismatch value G_c, providing a minimal

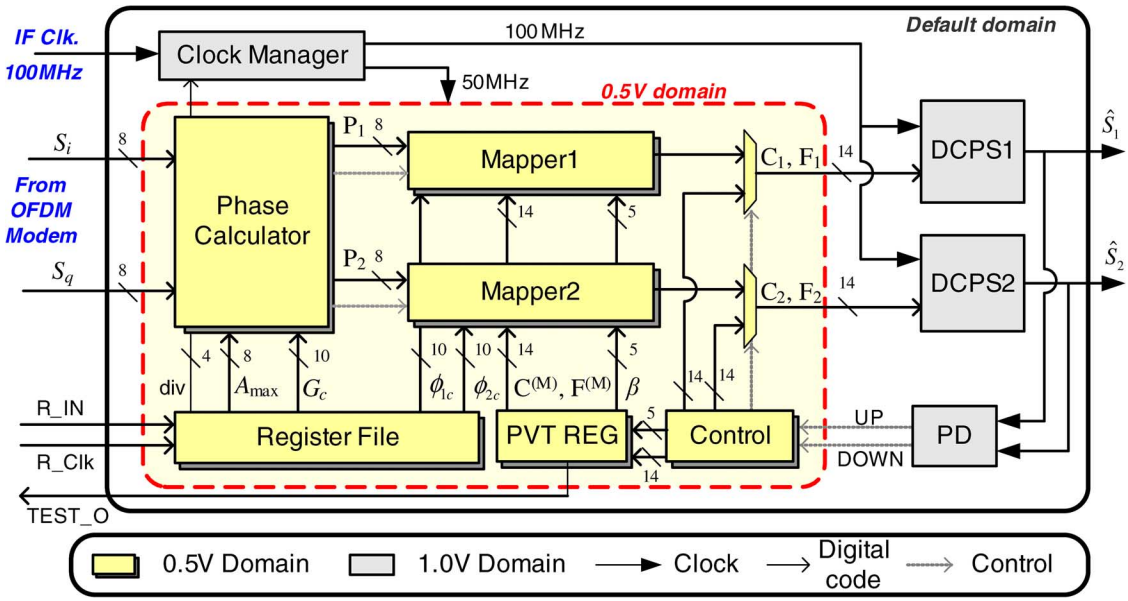

Fig. 8. Proposed SCS chip design with power domain partitions.

0.02 dB gain compensation resolution. Another system parameter for the phase calculation is the $A_{\max}$ value, which is decided by the trade-off between the clipped signal distortion and the combiner efficiency. Although the nonlinear PA achieves high efficiency, the overall amplification efficiency is still affected by the combiner efficiency related to the phase distribution of $\phi_1(t)$ and $\phi_2(t)$ [16]. Larger $A_{\max}$ value can avoid the signal clipping, but also increases the probability of small $\phi_1(t)$ values and sacrifices the average combiner efficiency. This design provides flexible $A_{\max}$ values for different system requirements and applications. Both G_c and $A_{\max}$ can be stored in the register file before the SCS operation; the SCS then computes the corresponding V_1 and V_2 values immediately for the phase calculation block.

Considering the increased transition time when using 0.5 V supply voltage, complex computations are difficult in meeting the timing requirement. For the phase calculation in (3) and (11), the critical path occurs on the long-bit divisions. Therefore, we use another expression to avoid the division operations to apply the voltage scaling scheme:

$$\begin{aligned}\theta(t) &= \tan^{-1}\exp\left(\log S_q(t) - \log S_i(t)\right)\\ \phi_1(t) &= \cos^{-1}\exp\left(\log\left(V_1^2 + 4A^2(t) - V_2^2\right)\right.\\ &\qquad \left. - \log\left(4A(t)V_1\right)\right)\\ \phi_2(t) &= \cos^{-1}\exp\left(\log\left(V_2^2 + 4A^2(t) - V_1^2\right)\right.\\ &\qquad \left. - \log\left(4A(t)V_2\right)\right). \end{aligned} \tag{14}$$

All of the divisions can then be replaced by the logarithm table to meet the 50 MHz operation requirement with 0.5 V supply voltage. Using an 8-bit division in $\theta(t)$ as an example, the synthesized propagation delay and area comparison is shown in Table I. The propagation delay of the division is over the target operation period of 20 ns when scaling to 0.5 V supply voltage. Using the modified expression, the propagation delay of the logarithm table is only 6.53 ns within allowable gate count increases. The other nonlinear operations, such as arctangent-exponential and arc-cosine-exponential functions, are also implemented by a reference table to reduce the propagation duration and computation complexity.

TABLE I
COMPARISONS BETWEEN DIVISION AND LOGARITHM TABLE

	1.0 V		0.5 V	
	Gate Count	Propagation	Gate Count	Propagation
Division	152	5.74 ns	152	22.49 ns
Log. table	279	1.82 ns	282	6.53 ns

C. DCPS and Mapper Design

Close-loop circuits have restrictions in achieving the multiphase generation with high-speed phase changing rate due to the long convergence duration. Therefore, an open-loop, digital-control delay line is suggested to provide the specific phases without convergence cycles. Fig. 9 shows the proposed DCPS structure. To achieve adequate delay range and fine-tune resolution under all processes, voltages, and temperature (PVT) conditions, the proposed delay lines use more control bits to achieve the requirement. This DCPS design contains two-stage delay-lines with a 9-bit coarse-tune codeword C and a 5-bit fine-tune codeword F to achieve adequate delay range and accuracy; and the delay-line is based on power-of-two architecture to avoid needing a complex codeword encoder. The digitally controlled varactors (DCV) [17] are applied to the fine-tune stage to generate ps-level resolution by adding small capacitance loading.

The relationship between the generated delay and two-stage codeword is shown in Fig. 10. With the phase codeword $P = k$, the output delay of DCPS can be expressed by $T_0 + kT_{ref}/256$, $k = 0, 1, \ldots, 255$, where T_0 is the constant delay and T_{ref} is the IF clock period. Denote the two-stage codewords corresponding to the delay $T_{2\pi} = T_0 + 255T_{ref}/256$ as $\mathrm{C}^{(\mathrm{M})}$ and $\mathrm{F}^{(\mathrm{M})}$, and the ratio of coarse-tune resolution T_C and fine-tune resolution

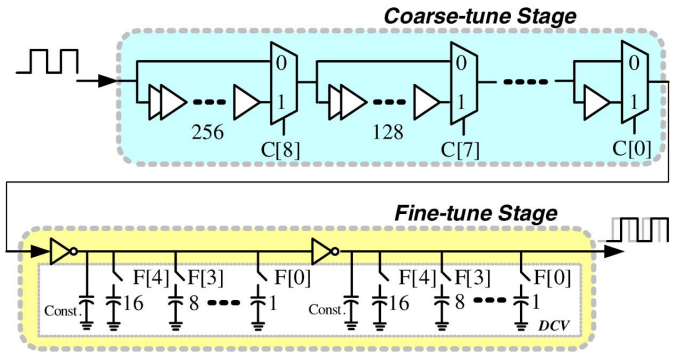

Fig. 9. Proposed DCPS design based on power-of-two architecture.

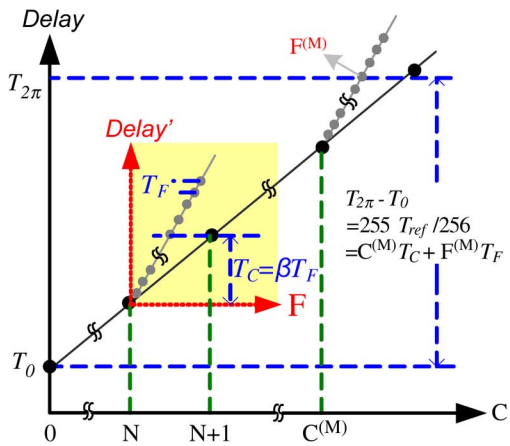

Fig. 10. Relationship between the output delay and the two-stage codewords C and F.

T_F as β. To generate the desired phase $2k\pi/256$, the mapper provides the DCPS coarse-tune codeword as

$$\mathrm{C} = \left\lfloor \frac{\mathrm{C}^{(\mathrm{M})}k}{256} \right\rfloor \tag{15}$$

and the fine-tune codeword as

$$\mathrm{F} = \left\lfloor \left(\frac{\mathrm{C}^{(\mathrm{M})}k}{256} - \left\lfloor \frac{\mathrm{C}^{(\mathrm{M})}k}{256} \right\rfloor \right) \beta + \frac{\mathrm{F}^{(\mathrm{M})}k}{256} \right\rfloor \tag{16}$$

where the first term is the compensation of the fractional part of coarse-tune codeword for delay accuracy enhancement.

Because the division with denominator 256 can be implemented by shifters, the complexity of the mapper is low. However, the $\mathrm{C}^{(\mathrm{M})}$, $\mathrm{F}^{(\mathrm{M})}$, and β values are influenced by PVT variations; therefore, a detection scheme to detect this information for the mapper before the normal operation is introduced in a later section.

The DCPS is delay-line based and can provide phase compensation capability. With the phase mismatch information, the DCPS pair can add the specified phase difference by adding a constant codeword offset on one of the branches to eliminate the phase delay imbalance. Additionally, high phase compensation resolution can be achieved according to the ps-level fine-tune capability of the DCPS.

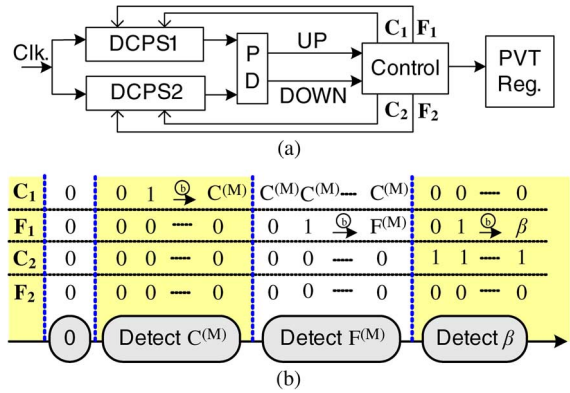

Fig. 11. (a) Proposed pre-calibration block diagram and (b) the behavior timeline.

D. DCPS Automatic Calibration Scheme

To detect the mapper parameters automatically, a calibration scheme is proposed. Taking advantage of the same property in the dual DCPSs, only an extra phase detector (PD) [18] is added to construct a delay-locked-loop (DLL) architecture, and the simplified block diagram is shown in Fig. 11(a).

The proposed scheme has three main states for $\mathrm{C}^{(\mathrm{M})}$, $\mathrm{F}^{(\mathrm{M})}$, and β value detection, respectively. The behavior timeline and corresponding codewords are shown in Fig. 11(b). For $\mathrm{C}^{(\mathrm{M})}$ detection, we first set $\mathrm{C}_2 = 0$ and $\mathrm{F}_2 = 0$ such that the output delay of DCPS2 is T_0; we then increase C_1 until the PD outputs "UP" and "DOWN" rise alternately, implying that the DLL converges. After that, $\mathrm{C}^{(\mathrm{M})} = \mathrm{C}_1$ can be decided. Similarly, $\mathrm{F}^{(\mathrm{M})}$ can also be detected by the same procedure. To detect β value, we set $\mathrm{C}_2 = 1$ and $\mathrm{F}_2 = 0$, to ensure that DCPS2 output delay is $T_0 + T_C$. Then, increasing F_1 from 0 with fixed $\mathrm{C}_1 = 0$, the DCPS1 output delay can be expressed as $T_0 + F_1 T_F$. When $\mathrm{F}_1 = \mathrm{F}^{(\mathrm{C})}$ and PD outputs "UP" and "DOWN" rise alternately, $T_0 + T_C = T_0 + \mathrm{F}^{(\mathrm{C})} T_F$ is implied. Because $T_C = \mathrm{F}^{(\mathrm{C})} T_F$, $\beta = \mathrm{F}^{(\mathrm{C})}$ can be concluded. Therefore, the required parameters can be detected by the proposed method with low extra overhead. The PVT is time varying; therefore, this calibration can be repeated before each transmission. To reduce the convergent cycles of the codeword tracking, the binary search scheme [18] is applied in this work. The required detection cycles of $\mathrm{C}^{(\mathrm{M})}$, $\mathrm{F}^{(\mathrm{M})}$, and β are 18, 10, and 10 in the worst case respectively, so the overall automatic calibration can be finished with less than 38 cycles.

V. Simulation and Experimental Results

The proposed SCS chip was fabricated using a 90 nm 1P9M standard CMOS process. Chips with three different process corners (FF, TT, and SS) specified by the factory were measured to verify the behavior. For the experimental environment, the measurement instruments included a LeCroy 4000A oscilloscope and a current-meter with a resolution of 100 pA. For further performance analysis, we used MATLAB and ADS to construct a simulation platform including the behavior model of FE components.

TABLE II
DCPS COARSE-TUNE AND FINE-TUNE OUTPUT DELAY

Corner	FF case	TT case	SS case
Constant delay	3.27 ns	3.63 ns	4.22 ns
Max. Coarse-tune Delay	14.90 ns	18.73 ns	22.23 ns
Max. Fine-tune Delay	0.09 ns	0.13 ns	0.17 ns
Coarse-tune Resolution	29.51 ps	37.76 ps	43.85 ps
Fine-tune Resolution	3.06 ps	4.21 ps	5.42 ps

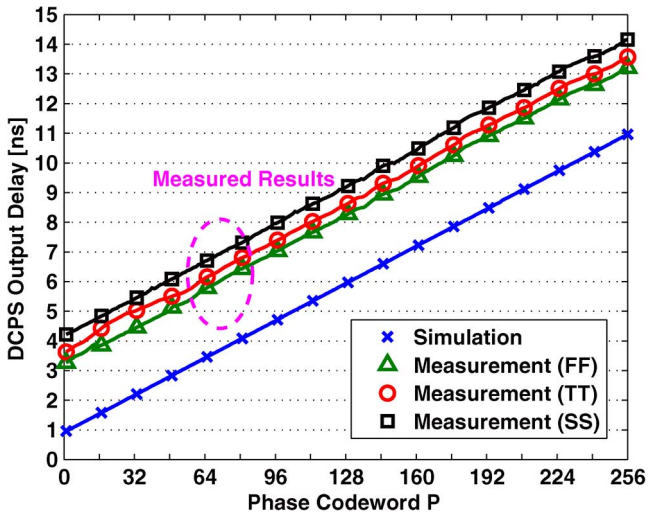

Fig. 12. DCPS output delay with different codeword P (target IF clock period 10 ns).

To verify the DCPS delay range, three different process corners chips were measured. The two-stage output delay and resolution are clearly shown in Table II. The maximal output delay of the coarse-tune range in three corners could cover the target IF clock period of 10 ns, and the fine-tune delay range could also cover the coarse-tune resolution. The average resolution of FF, TT, and SS cases were ps-level, not only helping more accurate codeword-to-delay mapping but also providing ps-level phase offset capability. Using the TT case operating at 100 MHz for example, the coarse-tune and fine-tune stages of the DCPS could provide additional maximal delays of 18.73 ns and 0.13 ns with a constant delay of 3.63 ns. The average resolutions of each stage were 37.76 ps and 4.21 ps, respectively, and the measured RMS jitter was 8.57 ps. The output delay could be fine-tuned by adding a specified codeword offset for phase compensation, and the minimal resolution of the DCPS implied a 0.15° phase adjustment capability.

By applying the proposed automatic detection scheme, the required parameters $C^{(M)}$, $F^{(M)}$, and β could be obtained and stored for mapper calculation. The measured DCPS output delay with the different codeword P is shown in Fig. 12 where 8-bit resolution with RMS error 9.33 ps (0.34°) could be achieved. The measured results are consistent with the simulation result except for the larger constant delay, because the IO pad delay was not considered during the simulation. The power consumption of the DCPS pair and PD was 912.9 μW at 100 MHz IF with 1 V supply voltage. Fig. 13 shows the measured output waveforms example when the baseband input is zero. The ideal output signal should be two vectors with opposite directions, indicating the 180° phase difference. The measured SCS correctly output the waveforms with a 180° phase difference between the two branches, and the phase difference was 5.003 ns which is close to the ideal value 5 ns.

To verify the LINC behavior with the proposed SCS chip and compensation scheme, the characteristic of the measured output waveform was fed back to an FE circuit model (including the filters and a nonlinear PA). Fig. 14 shows the simulated system spectrum at IF considering the branch mismatch effect; the spectrum without mismatch calibration is over the mask due to incomplete outphasing signal cancellation. With the proposed SCS and mismatch compensation scheme, the spectrum can pass the 1/4 scaled 802.11a mask due to the adopted 5 MHz symbol rate in this work. Both EVM -29.81 dB and ACPR -34.56 dB could be achieved, which satisfy the standard requirements of -25 dB and -27 dB, respectively.

Fig. 15 shows the microchip photo with power domain notations, and the active area of the DCP functions and the DCPS pair is only 0.06 mm^2. The power pads of the default domain and 0.5 V domain are separate; therefore, the power dissipation of the individual domain could be measured independently. The power consumption of the DSP blocks with 50 MHz operation speed is shown in Fig. 16. Note that the power dissipation was reduced from 140.1 μW to 36.6 μW by scaling the supply voltage to 0.5 V, resulting in 73.88% power reduction. The shmoo plot of the digital processing is shown in Fig. 17, demonstrating that the higher frequency is achievable as the supply voltage increases. Our target specification involves operating at 50 MHz with 0.5 V supply voltage.

The chip summary and comparisons are shown in Table III. The comparison does not include the digital SCSs [3] and [4] because they are implemented by field-programmable gate arrays (FPGA). This work proposes an all-digital and standard-cell-based design. Using a low-complexity DCPS pair instead of DACs, and scaling the supply voltage for DSP blocks, the overall chip consumes only 949.5 μW, a significant improvement compared to state-of-the-art chip solutions. For a fair comparison of the power consumption with different technologies, a normalized power factor $P_{\rm nor}$ is defined as

$$P_{\rm nor} = \frac{P_{\rm ori}}{V_{cc}^2} \tag{17}$$

where $P_{\rm ori}$ is the reported power before the normalization and V_{cc} is the supply voltage. As shown in the table, the normalized power factor of the proposed design is still the smallest compared to the state-of-the-art solutions. With the advantages of both technology scaling and low circuits complexity, the active area is also the smallest. The EVM performance is lower than [8] because we further consider the 8-bit baseband quantization error and branch mismatch effect. However, the EVM performance is still acceptable for the demonstrator systems.

Considering low power applications, such as the WBAN system in [12], we compare the power amplification cost of the conventional transmitter using a linear amplifier (Class-A) and the LINC technique. The circuits of a basic linear PA and Class-D PAs are implemented in ADS for performance

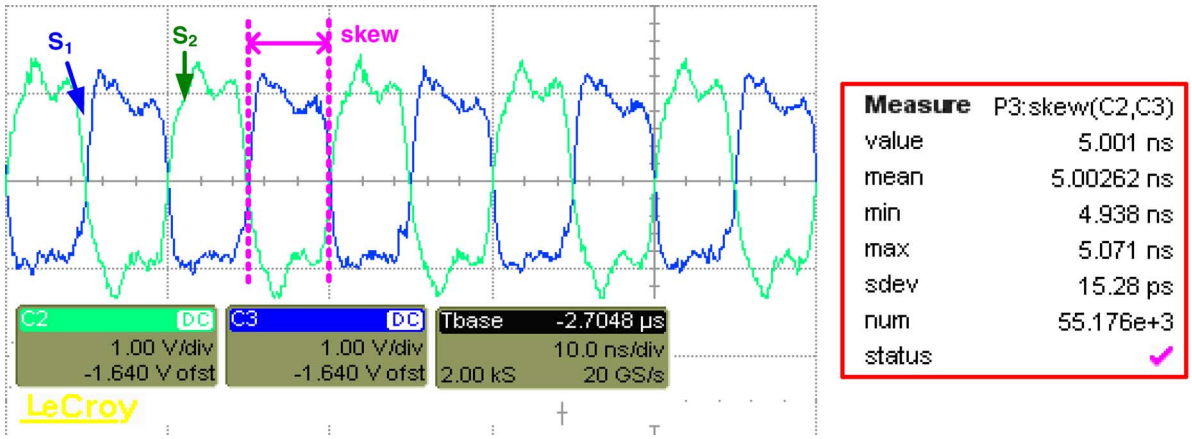

Fig. 13. Measured SCS output waveforms when the baseband input is zero.

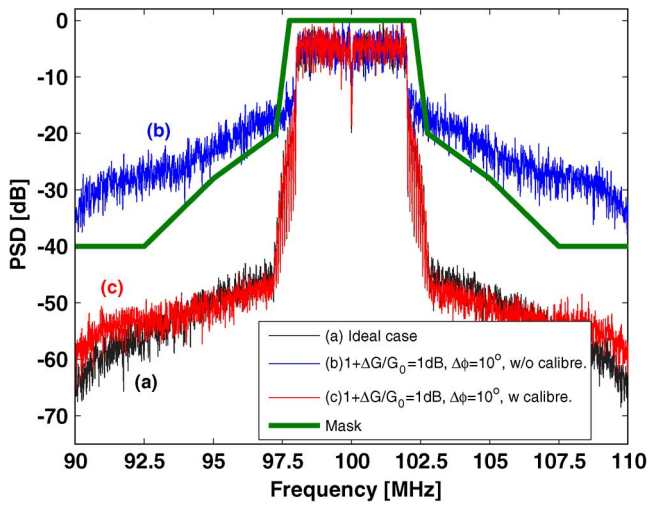

Fig. 14. Output signal spectrum.

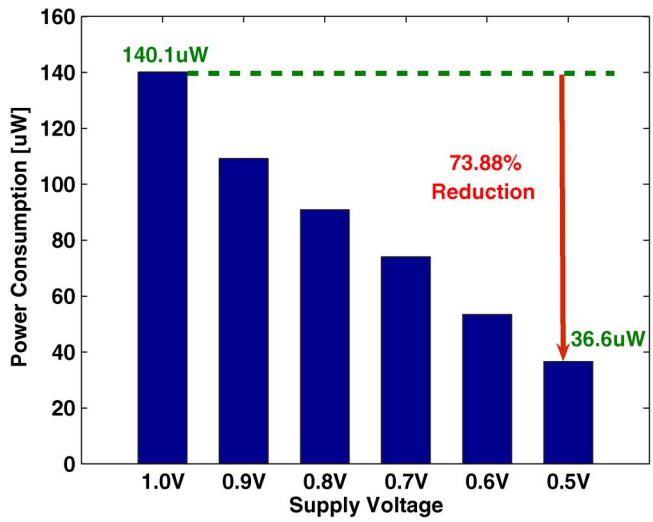

Fig. 16. Measured DSP blocks power with different supply voltages.

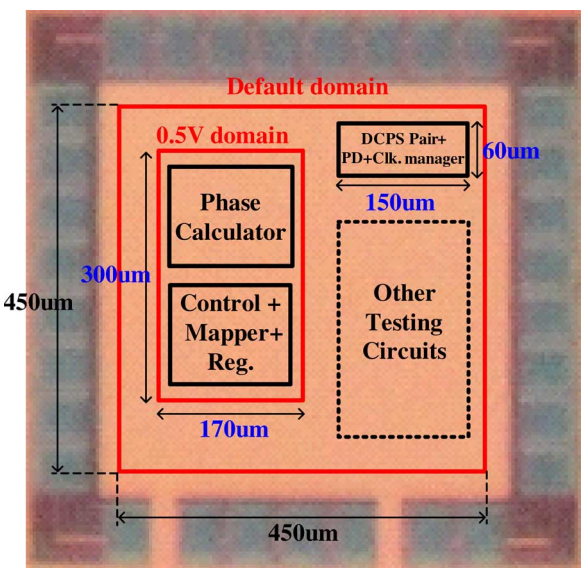

Fig. 15. Chip photograph.

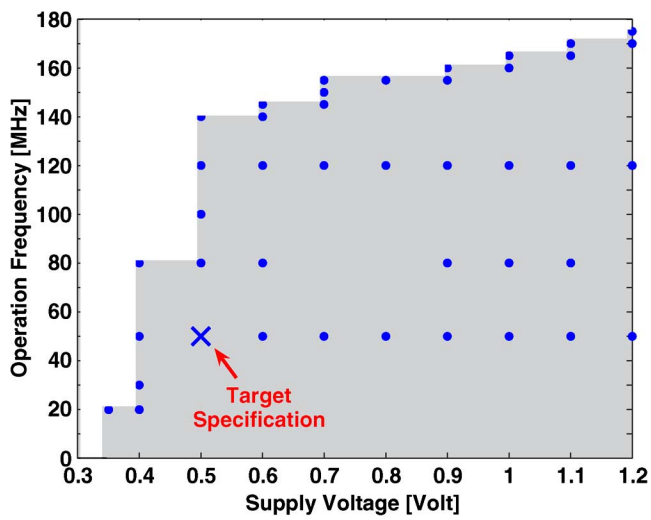

Fig. 17. Shmoo plot of the DSP blocks.

comparisons. According to the transmitted power of 0 dBm with 7 dB back-off operation, the simulated average efficiency of the Class-A PA is only 5.15%, implying a 19.42 mW average power dissipation on the linear PA, dominating the overall transmitter power. For the LINC technique, the average

TABLE III
CHIP SUMMARY AND COMPARISONS

	[6]	[7]	[8]	This work
Technology	0.8 um BiCMOS	0.35 um CMOS	0.25 um CMOS	90 nm CMOS
Design Strategy	Analog	Analog	Analog	All digital, Standard-cell
Supply Voltage	5.0 V	5.0 V	2.5 V	1.0 V/0.5 V
Operation Frequency	200 MHz IF	100 MHz IF	Baseband	100 MHz IF (50 MHz DSP)
Power Consumption	100 mW	80 mW	45 mW	0.95 mW
Normalized Power Factor	4	3.2	7.2	1.05
Signal Source	DQPSK	DQPSK/ OQPSK	64QAM OFDM	64QAM OFDM
EVM	N/A	N/A	-34 dB	-29.81 dB
Mismatch Compensation	No	No	No	Yes
Active Area (mm^2)	2.66(*)	0.61(*)	0.09	0.06

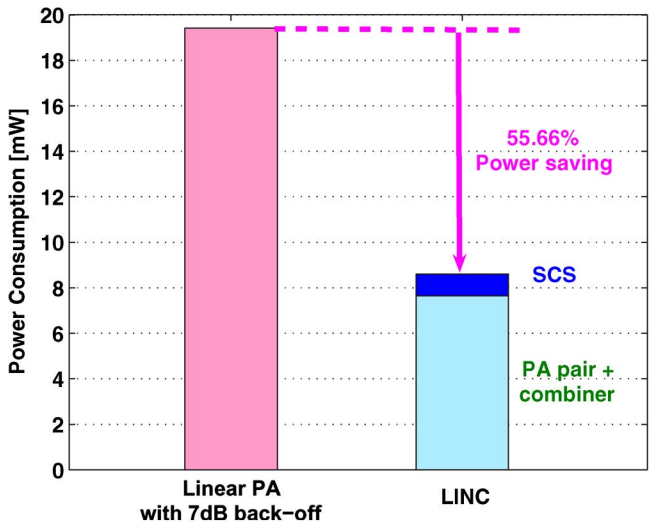

Fig. 18. Power consumption comparison of amplification blocks between conventional linear PA and LINC with the proposed SCS.

efficiency can be improved to 13.08%, leading to a power saving of 11.76 mW from the amplification blocks. Because the SCS is an additional overhead in the LINC transmitter, the power dissipation should also be considered, especially for the applications with low transmitted power. The power overhead of the state-of-the-art SCS designs in [6]–[8] are larger than the power saved. Because the proposed SCS costs less than 1 mW, the overall power saving of 10.81 mW can be achieved when applying the LINC technique with the proposed SCS design, resulting in a 55.66% power reduction, as shown in Fig. 18.

VI. CONCLUSION

An all-digital SCS design is presented in this work, and a branch mismatch compensation scheme is integrated to release the FE circuits and PA design complexity. The proposed low-complexity DCPS pair with an automatic calibration scheme can generate phase-modulated signals without DACs, and also provides high-resolution phase compensation capability. Moreover, the DSP circuits can achieve accurate nonlinear calculation and the power consumption is reduced by applying the voltage scaling. Therefore, a sub-mW and accurate LINC SCS can be achieved and applied to general OFDM systems to enhance amplification efficiency while maintaining similar link performance.

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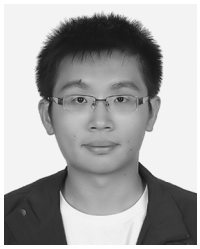

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