A Novel Nanoinjection Lithography (NInL) Technology and Its Application for 16-nm Node Device Fabrication

Hou-Yu Chen, Chun-Chi Chen, Fu-Kuo Hsueh, Jan-Tsai Liu, Shyi-Long Shy, Cheng-San Wu, Chao-Hsin Chien, Chenming Hu, Chien-Chao Huang, and Fu-Liang Yang

***Abstract*—For more than 45 years, photon- and electron-sensitive materials have been used to produce pattern-transfer masks in the lithographic manufacturing of integrated circuits. With the semiconductor technology feature size continuing to shrink and the requirements of low-variability and low-cost manufacturing, optical lithography is driven to its limits. In this paper, we report a novel nanoinjection lithography (NInL) technique that employs electron-beam-assisted deposition to form pattern-transfer hard mask in a direct-write deposit approach. By scanning the 4.6-nm-diameter electron beam while injecting a suitable organometallic precursor gas around the location of e-beam and just above the substrate, we form a high-density (pitch: 40 nm) high-uniformity (3-sigma linewidth roughness: 2 nm) hard mask for subsequent etching without using proximity-effect correction techniques. Furthermore, this technique can also directly deposit a metal pattern for interconnect or a dielectric pattern without the need for separate metal or dielectric deposition, photoresist etch-mask, and etching processes. The NInL approach simplifies the hard-mask creation or even metal or dielectric pattern creation process modules from five or tens of steps to only a single step. Therefore, it saves both photomask making and wafer processing costs. In addition, room-temperature NInL deposition of conductor/dielectric materials enables the fabrication of small versatile devices and circuits. For demonstration, we fabricated a functional 16-nm six-transistor static random access memory (SRAM) cell (area: occupying only 0.039 μm^2), 43% the size of the smallest previously reported SRAM cell, using the FinFET structure and a dynamic V_{dd} regulator approach. The NInL technique offers a new way of exploring low-volume high-value 16-nm complementary metal–oxide–semiconductor (CMOS) devices and circuit designs with minimal additional investment and obtains early access to extreme CMOS scaling.**

***Index Terms*—Direct-write, electron beam (e-beam), FinFET, nanoinjection lithography (NInL), static random access memory (SRAM).**

Manuscript received January 25, 2011; revised July 16, 2011; accepted July 22, 2011. Date of publication September 8, 2011; date of current version October 21, 2011. This work was supported in part by the National Science Council, Taiwan. The review of this paper was arranged by Editor R. Huang.

H.-Y. Chen and C.-H. Chien are with the Department of Electronics Engineering and the Institute of Electronics, National Chiao-Tung University, Hsinchu 300, Taiwan, and also with the National Nano Device Laboratory, Hsinchu 300, Taiwan (e-mail: henry0530@yahoo.com.tw).

C.-C. Chen, F.-K. Hsueh, J.-T. Liu, S.-L. Shy, C.-S. Wu, C.-C. Huang, and F.-L. Yang are with the National Nano Device Laboratory, Hsinchu 300, Taiwan.

C. Hu is with the Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720-1770 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TED.2011.2163938

I. Introduction

Although lithography has been a spectacularly successful enabler for semiconductor development, meeting the resolution requirements for the technology roadmap at 16 nm will extremely be difficult for optical lithography systems [1]–[4]. Based on the International Technology Roadmap for Semiconductors (ITRS) roadmap [1], the half pitch of key critical layers will be smaller than 22 nm when the technology node is beyond the 16-nm node. Although several techniques have been developed to demonstrate the extremely scaled static random access memory (SRAM) cell [5]–[7], the increasing production cost and process complexity are still the challenges for manufacturing. Among the patterning techniques, extreme ultraviolet (EUV) is a leading candidate due to its potentially lower cost than extending the conventional 193-nm deep-ultraviolet (DUV) lithography with the double-patterning approach [1]. In 2009, IMEC demonstrated the first 22-nm node SRAM using the EUV lithography and single patterning in the contact/metal critical layers [8]. In this pioneering work, the contact minimum pitch is 90 nm with 3-sigma linewidth roughness (LWR) of 2$\sim$3 nm, enabling the formation of dense array pattern without optical proximity correction (OPC) or resolution enhancement techniques (RETs). Furthermore, Veloso *et al.* report a record high-resolution 11-nm half pitch by using the EUV interference lithography [9]. However, EUV mask fabrication is still a challenge [4], and mask set price of up to three million US dollars is punitive for test chips and pilot productions in the 16-nm era. E-beam lithography, a maskless process, is an attractive lithography alternative—at least in the initial circuit-verification stage. Our experimental data have shown, however, that electron beam (e-beam) lithography suffers from LWR and the proximity effect when preparing high-density patterns. These problems arise from electron scattering in the photoresist, as shown in Fig. 1. The unwanted secondary electron scattering results in the loss of resolution. Although the 10-nm half pitch can be resolved [10], the high aspect ratio of the electron resist structures cause the resist lines to collapse, and the photoresist line-edge roughness is not satisfactory for device fabrication.

In this paper, we present a novel maskless and electron photoresist-free technology, which we have called nanoinjection lithography (NInL), and use it to fabricate the first reported 16-nm finely patterned SRAM devices. Indeed, using this NInL technique allows the rapid fabrication of nanometer-scaled

0018-9383/$26.00 © 2011 IEEE

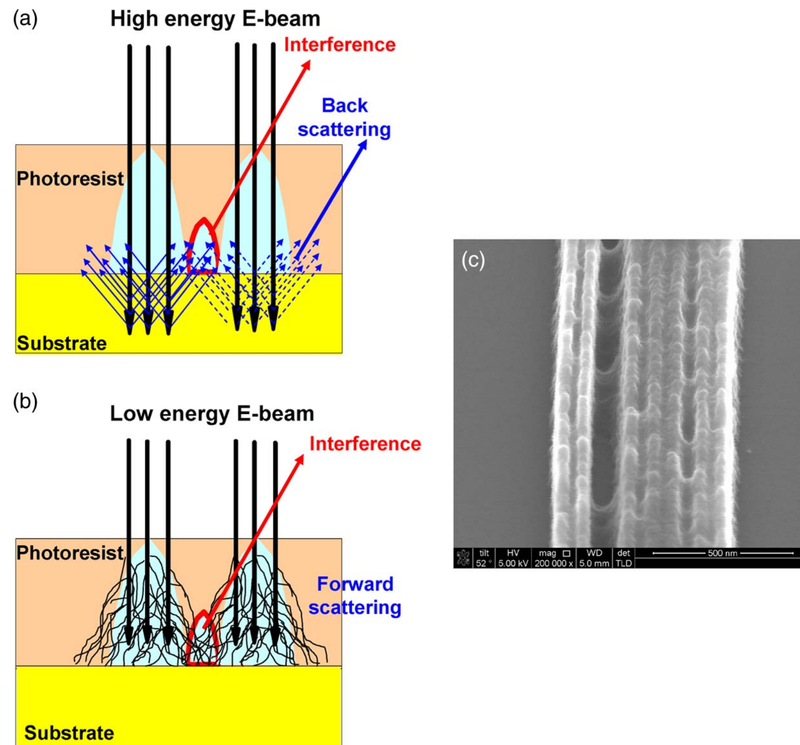

Fig. 1. Schematic and SEM top-view pictures of e-beam lithography. (a) Backscattering effect of a high-energy e-beam. (b) Forward scattering effect of a low-energy e-beam. (c) Effect of electron-scattering-induced interference with e-beam lithography.

devices with high pattern densities, low LWR, and minimal entry costs—ideal for the preliminary evaluation of the performance of ultrascaled devices. NInL directly deposits a pattern-transfer hard mask or metal interconnect and dielectric patterns on the substrate surface, depending on the precursor gas through electron-beam-assisted chemical reactions. Because material deposition is incited by the electron-gas reaction, the dimensional characteristics of the deposited feature are strongly dependent on the electron flux distribution, as well as the spatial distribution of the molecule dissociation. For an astigmatism- and aberration-free focused beam, the radial flux distribution incident on a plane surface can be described as a Gaussian, i.e.,

$$f(r) = \frac{I_p/e_o}{2\pi a^2} \exp\left(-\frac{r^2}{2a^2}\right)$$

where $f(r)$ is the number of electrons per unit area, a is the standard deviation, I_p is the beam current, and e_o is the elementary charge [11]. A small beam current results in a narrower full-width-at-half-maximum (FWHM) of the flux distribution, confining the electron flux to a tiny column. Another important factor determining the beam diameter is the acceleration voltage. After the electron distribution has been known, the deposition rate $R(r)$ as a function of the distance r from the center of the injected e-beam can be expressed as [12]

$$R(r) = Vn(r) \int_0^{E_0} \sigma(E) f(r, E) dE$$

where V is the volume of the decomposed molecule, $n(r)$ is the number of adsorbed molecules per unit surface, $\sigma(E)$ is the energy-dependent electron impact dissociation cross section, and E_o is the energy of the incident primary electrons. When the primary electrons impinge on the material, the resulting electron distribution $f(r, E)$ near the surface is a convolution of the primary beam spectrum with the backscattering and secondary electron spectra. Generally, the gas-assisted deposition rate depends on which electrons the molecular dissociation can be attributed. The relative influences of primary, backscattering, and secondary electrons on molecule interaction are still under investigation [12]. Although the smallest beam diameter can be obtained by increasing the beam energy and reducing the electron injection distance, the high-energy electrons impacting on the material surface could also cause damage due to, for example, crystalline amorphization during deposition. This electron incidence-induced damage could change the material properties. More importantly, it could penetrate into the material and damage structures at greater distances from the deposition region. One restriction on this kind of high-energy e-beam deposition occurs in metal–oxide–semiconductor field-effect transistor (MOSFET) gate electrode patterning using the high e-beam energy of NInL lithography. If the gate material thickness is less than 50 nm and 10-keV platinum (Pt) hard-mask deposition is used, the high-energy electron incidence causes gate dielectric damage in an active region underneath the gate electrode, leading to a high device gate current and destroying the device characteristics. Consequently, to precisely achieve the design rule requirements of the original layout, optimal processing conditions are required, including the e-beam energy, current, and deposition time. Although

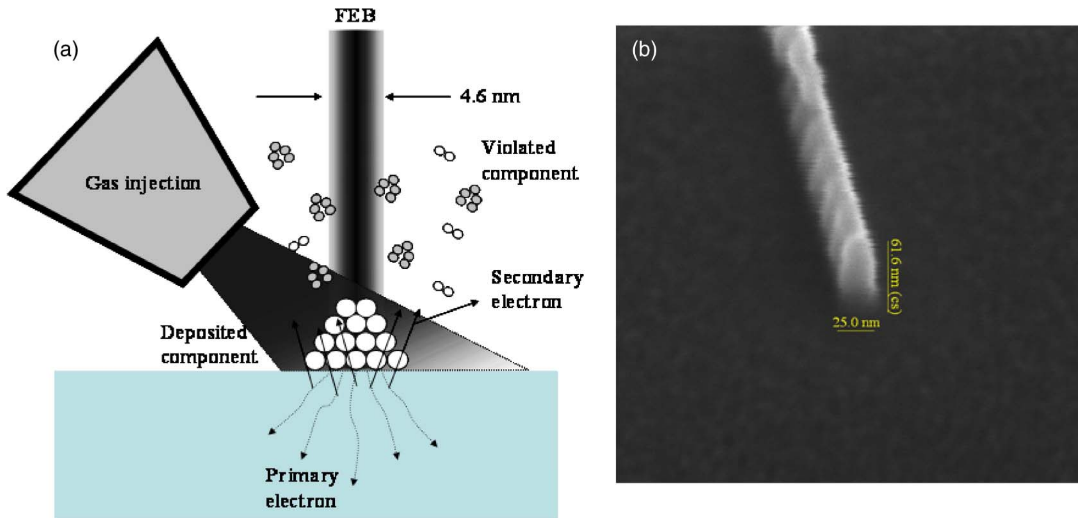

Fig. 2. (a) Principle of FEB-induced deposition. (b) 25-nm NInL hard-mask formation using FEB deposition. The e-beam energy is 5 keV, and the beam current is 0.4 nA, with $((CH_3)3CH_3C_5H_4Pt)$ as the precursor gas.

the throughput and compactness of the deposited material are key challenges, a low-energy low-current beam operation is preferable, particularly for device fabrication.

In the past, e-beam-assisted chemical reactions have been used to define nanometer-scale periodic lines or dots structure [13], [14] but not to fabricate MOSFETs. Here, we report the fabrication of a 6T-SRAM cell having an area of 0.039 μm^2 [15], which is 43% the size of the 22 nm-node SRAM previously reported [16]. SRAM device designs and SRAM cell circuit operations are also important for realizing such a small SRAM cell device. We used straight patterns for the active areas and gates of the SRAM cell to minimize stochastic device mismatch. This SRAM device features a nanowire FinFET channel to provide the best short-channel effect (SCE) and a single TiN gate for simple process integration. As the cell size decreases, using a high-beta-ratio SRAM cell design to obtain a sufficient static noise margin (SNM) becomes difficult because of increasing variations in device characteristics [17]. In this paper, we used the dynamic V_{dd} regulator (DVR) approach [19] to increase the signal-to-noise margin of the tiny SRAM cell.

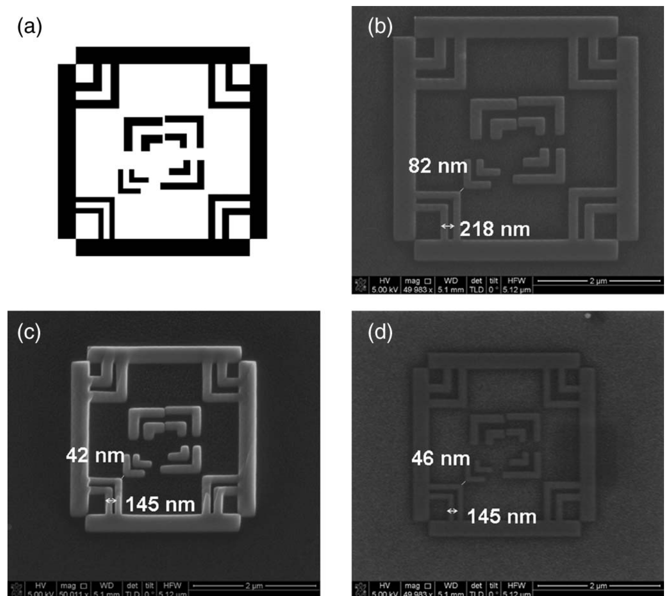

Fig. 3. (a) Layout with no OPC was employed for NInL lithography implementation. (b) NInL lithography hard-mask deposition using a 5-keV beam energy and 0.4-nA beam current. The Pt deposition thickness was set to 50 nm. The deposition area is defined to 4 μm $\times$ 4 μm. (c) NInL lithography hard-mask deposition using a 5-keV beam energy and 0.4-nA beam current. The Pt deposition thickness was set to 50 nm. The deposition area is defined to 3 μm $\times$ 3 μm. (d) NInL lithography hard-mask deposition using a 5-keV beam energy and 98-pA beam current. The Pt deposition thickness was set to 50 nm. The deposition area is defined to 3 μm $\times$ 3 μm.

II. Device Fabrication

The NInL technology is demonstrated with an electron/ion dual-beam system. This system uses e-beam energy to perform and localize chemical vapor deposition at specific locations by a direct-writing technique. Fig. 2(a) illustrates the focused electron beam (FEB)-induced deposition process. The gas nozzle of the system can inject a variety of organometallic precursor gases to deposit desired materials in a vacuum chamber. The injected gas molecules are adsorbed on the substrate surface and are dissociated by the impact of electrons. The energetic electrons decompose the organometallic molecules and release nonvolatile products such as metal atoms on the substrate surface. In this paper, $((CH_3)3CH_3C_5H_4Pt)$ organometallic precursor gas was selected for Pt hard-mask deposition, with a vacuum pressure of about the range of 3×10^{-6} torr. A gas nozzle is usually positioned 0.1 mm above the substrate surface at an angle. The precursor gas is produced by heating the liquid precursor. To obtain small patterns of the deposited material, a 5-keV 98-pA 4.6-nm-diameter e-beam was usually employed as the beam source rather than an ion beam. This process creates an etch hard mask that performs the function of the photoresist pattern in the conventional photolithography process for subsequent etching. Due to the lower energy of the e-beam, the deposited layer has high carbon content, with an atomic percentage close to 75% of the deposited Pt pattern layer [20]. The high-carbon-content composition of this deposited hard-mask material is similar to photoresist; hence,

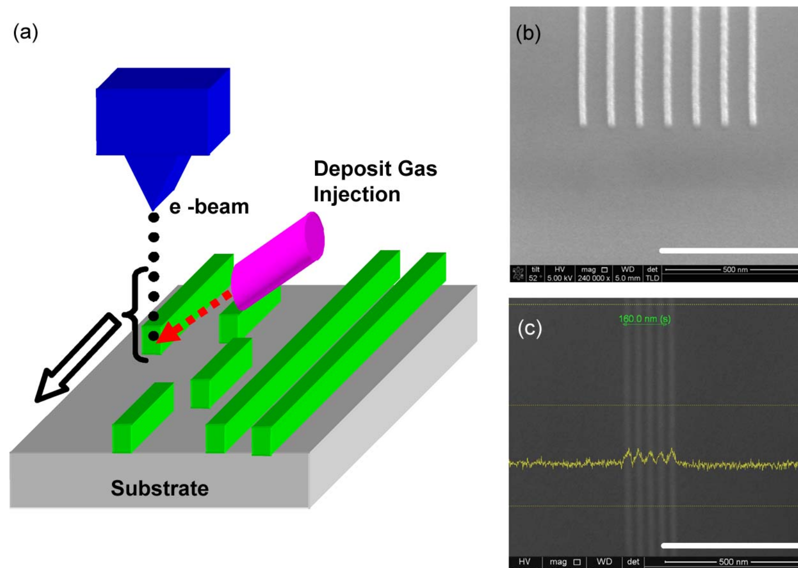

Fig. 4. (a) NInL uses the FEB deposition process. (b) 20-nm Pt line hard-mask deposition with a 90-nm pitch. (c) 20-nm Pt line hard-mask deposition with a 40-nm pitch.

the same chemicals and equipment of photoresist stripping in the metal–oxide–semiconductor (MOS) process can be applied for NInL hard-mask removal. The thickness of the hard mask is determined by the beam dwell time and other process posse settings of the deposition process. Fig. 2(b) shows the deposited Pt hard mask with an aspect ratio of 2.5 and a 25-nm linewidth pattern. Fig. 3 shows the e-beam current effect on Pt hard-mask deposition at a Poly-Si substrate. A significant resolution improvement on the deposited Pt hard mask can be achieved by reducing the beam current while maintaining the beam energy. The hard mask is suitable for the high-selectivity etching process. After loading the layout design into the control computer of the system, the holder stage precisely moves to perform the pattern deposition to transfer the required layout onto the substrate. Fig. 4 shows different line/space pitch patterns fabricated with this NInL. Because the hard mask is deposited onto the substrate, problems that are associated with photoresist exposure and development are alleviated, and a 20-nm line/spacing pitch can be obtained with superior line-edge roughness. In conventional optical lithography, to correct image errors due to diffraction and process effects, OPC is the technique that is commonly used to improve the edge placement integrity of the original design. Without OPC, the resist patterns contain irregularities, which may significantly alter the electrical properties of devices. By using NInL, 30-nm line-end spacing with excellent critical dimension (CD) control can easily be achieved without OPC or other RETs, such as scattering bar insertion. Fig. 5 shows the benefit of using NInL for multiple nanowire patterning. Even when the source–drain (S/D) spacing shrinks to 70 nm for series resistance reduction and the nanowire pitch decreases to 40 nm to obtain large MOSFET channel for an increase of effective width, the shape of the hard mask shows clean separation of the lines. This condition effectively reduces the nanowire width variation and increases the nanowire device density compared to the optical lithography patterning approach. Therefore, it shows that the costly OPC is not necessary.

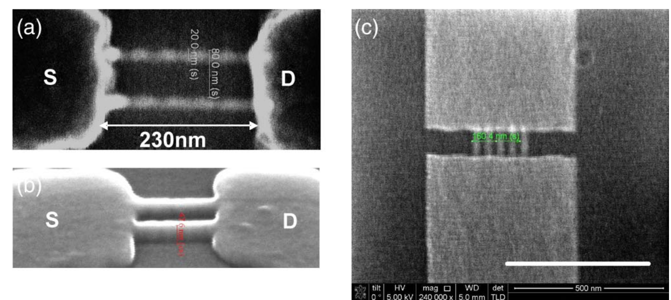

Fig. 5. SEM top view of high-density nanowire devices. (a) NInL Pt hard-mask deposition. (b) After Si pattern etch. The nanowire pitch is 80 nm, and the S/D distance is 230 nm. (c) NInL hard-mask deposition with a 40-nm nanowire pitch, where the S/D distance is 70 nm. No proximity effect correction is applied.

For SRAM fabrication, this paper used (100) surface and 30-nm-thickness p-type silicon silicon-on-insulator (SOI) wafers as substrates. Prior to the active-area definition, wafers were chemically cleaned in hydrofluoric (HF) acid and rinsed with deionized water. The wafers then went through to NInL for hard-mask Pt deposition. Fig. 6 illustrates the active-area patterning process flow. After the NInL hard-mask deposition, the wafers were subjected to Si etch in a TCP9400 plasma etcher at a chamber pressure of 8×10^{-3} torr with HBr reaction gas. After the etching, hard-mask removal was performed using reactive ion etching with O_2 plasma, followed by wet etchant cleaning using H_2SO_4 and H_2O_2. Thermal oxidation and hydrogen annealing followed by oxide stripping was applied to reduce etch damage and corner rounding. This process achieved a high-density nanowire channel with a 64-nm minimum pitch, as shown in Fig. 6(d). After nanowire formation, 1.6-nm oxynitride was grown as the gate dielectric. TiN metal deposition and then NInL hard-mask creation were performed for gate electrode definition. After the TiN gate etching, a 25-nm oxide layer was deposited using NInL. This low-temperature oxide layer acted as a spacer. Wafers then underwent deep S/D implantation using arsenic at 7 keV and a dose of $1 \times$

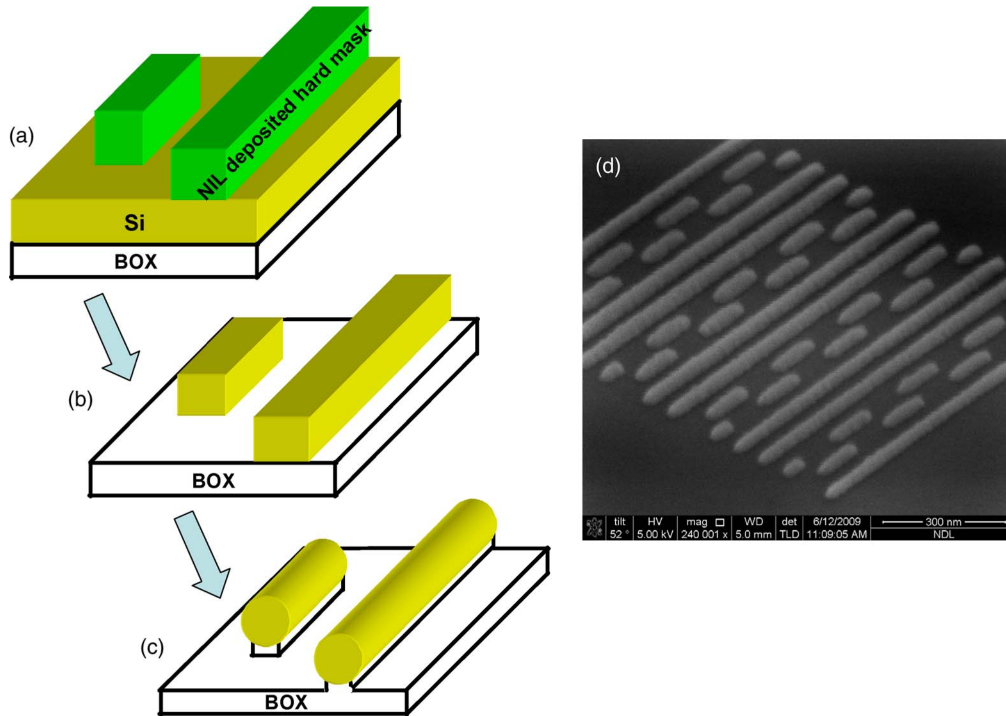

Fig. 6. Process flowchart of nanowire formation. (a) NInL hard-mask deposition. (b) Si etch. (c) Formation of a nanowire channel. (d) Tilt-angle SEM view of the Si nanowire array.

TABLE I
COMPARISON OF THREE LITHOGRAPHY TECHNOLOGIES

<table>
<tr><th></th><th>EUV</th><th>E-beam Lithography</th><th>Nano Injection Lithograpgy (This work)</th></tr>
<tr><td>Photo Mask issue</td><td>1. Defect repair.
2. Mask costly.</td><td colspan="2">Maskless</td></tr>
<tr><td>Photoresist process issue</td><td>1. EUV resist induced flare effect.
2. Polymer P.R. related line width roughness.
3. Proximity effect</td><td>1. Polymer P.R. related line width roughness.
2. Tradeoff exposure throughput with resolution and proximity effect.</td><td>Photoresist Free
(Potential drawback:
High-energy electron impinge induced damage.)</td></tr>
<tr><td>Patterning process steps</td><td colspan="2">1. Blanket hard mask deposit
2. Resist coating.
3. Exposure
4. Develop
5. Resist stripping</td><td>One step
(Potential drawback:low throughput for large area patterning.)</td></tr>
</table>

10^{15} cm^{-2} for a negative-channel field-effect transistor (nFET) and BF_2 at 7 keV and a dose of 1×10^{15} cm^{-2} for a positive-channel field-effect transistor (pFET). NInL e-beam-deposited oxide served as an implant mask. The oxide hard mask was stripped using XeF_2 precursor gas in the NInL system after implantation. A 1000 °C 10-s rapid thermal annealing (RTA) for dopant activation was performed. Finally, Pt was deposited by NInL as the metal interconnect and contact pad for electrical measurements.

III. RESULTS AND DISCUSSION

Table I shows the benefits of NInL compared to advanced lithography. Three key features make NInL more attractive than optical, EUV, or e-beam lithography for low-volume fabrication at 16-nm node technology and beyond. First, this approach requires no mask and no photoresist or electron resist, which reduces the number of process steps from five to only one, as shown in Table I. Second, photoresist-free surface reaction technology is less influenced by light/electron interference and

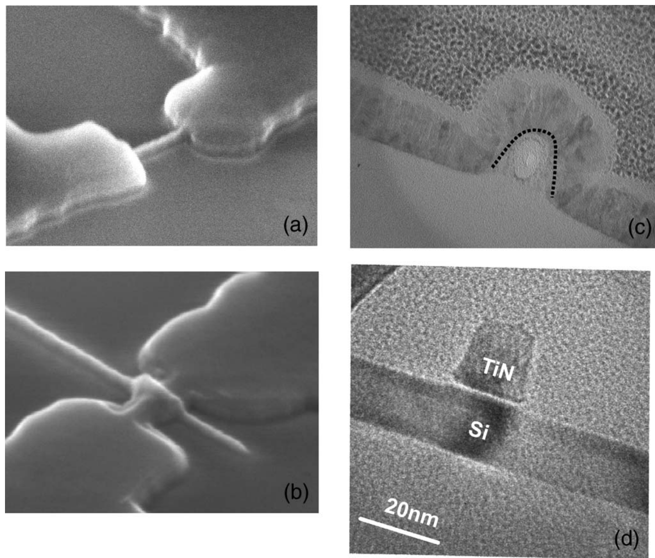

Fig. 7. (a) Tilt-angle view of the Si nanowire channel formation. (b) Tilt-angle view of the Si nanowire after gate patterning and a locally defined spacer deposition. (c) Cross-sectional TEM view showing the silicon nanowire covered with an omega-shaped TiN gate. (d) Cross-sectional TEM view of an 18-nm TiN gate.

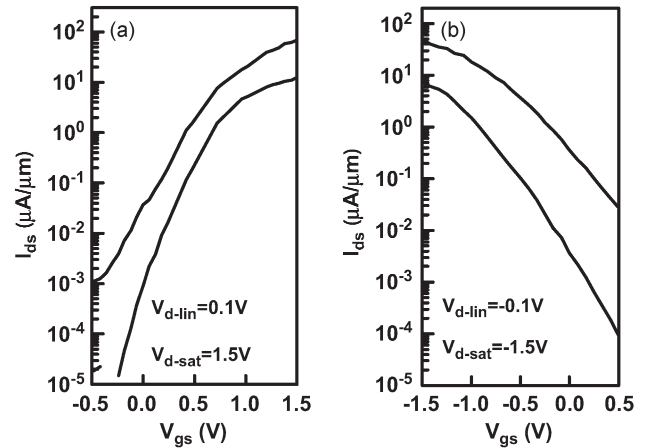

Fig. 8. (a) nFET nanowire FinFET device I_d–V_g characteristics. (b) pFET nanowire FinFET device I_d–V_g characteristics.

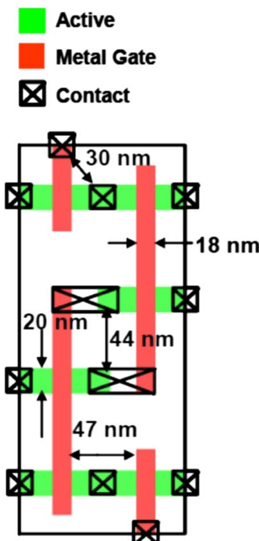

Fig. 9. Cell layout of a 0.039-μm^2 6T SRAM and key design rules.

scattering, thus producing less proximity effects and better space resolution. Third, the additional cost of eliminating the aforementioned proximity effect by "double exposure" for high-density circuits [5], [21], [22] is eliminated. The double-exposure approach also increases the stochastic device variation. To achieve shorter channel devices, nanowire or multiple gate devices are the attractive candidates due to their superior SCE immunity for ultrascaled devices. A nearly surrounding gate structure with scaled channel dimensions can prevent the drain-side electric field from penetrating the channel without requiring a heavily doped channel [23]. Hence, it is beneficial for device V_t uniformity. Fig. 6 shows scanning electron microscope (SEM) pictures of the device fabrication steps. Fig. 7(a) shows a tile angle-view SEM picture of the active area after hard-mask removal and after the formation of the silicon nanowire channel. Fig. 7(b) shows the tile angle-view SEM picture of a device after TiN gate patterning and local spacer region defined with NInL deposition. To obtain better SCE control, tetraethyl orthosilicate (TEOS)-based oxide was deposited as a spacer using e-beam-assisted chemical reaction with an extremely low thermal budget. Fig. 7(c) and (d) shows TEM pictures of the nanowire channel and TiN gate region featuring an 18-nm gate length. Fig. 8(a) and (b) shows nFET/pFET nanowire devices I_d–V_g characteristics. To obtain an adequate SNM of the low-beta-ratio SRAM, the device threshold voltages (V_t) are designed to be low for pFET and high V_t for nFET. In this paper, conventional silicidation is not applied. Instead, good improvement is made to the device performance, and SCE is obtained by using ultrashallow junction formation, a novel silicide process, and super annealing [16]. For the SRAM cell layout design, a symmetrical cell, as illustrated in Fig. 9, with simple straight patterns for the active areas and gates is applied to maximize the advantage of the low LWR advantage of NInL. Fig. 10(a) shows a top-view SEM image of a NInL-patterned SRAM gate array. For low critical dimension variation of the SRAM devices, 2-nm 3-sigma LWR of the 18-nm gate length is obtained. Fig. 10(b) shows the top-view SEM image of the SRAM cell after gate etching. There are no double-exposure and etching processes applied, again reducing the process complexity and device variability. Fig. 10(c) shows that the active region to gate and Pt contact overlays are well controlled using a close neighbor cell alignment mark and due to its interconnect using NInL Pt interconnect deposition. There are no bird's beaks, even with very narrow spacing, when using NInL. Due to the critical linewidth requirement of SRAM metal routing, NInL-deposited Pt is employed for the interconnect material, i.e., a Pt pattern is deposited with the NInL technology as interconnects rather than hard masks, as shown in Fig. 10(d). However, compared to the conventional deposited Pt, the NInL Pt has higher carbon content. The sheet resistance is 9.9 μm, which is several times higher than the conventional metal conductors. To fulfill the resistance requirement for the high-performance circuit, a thermal treatment or improved precursor may improve the sheet resistance. As the cell size and operating voltage decreases, using a high-beta-ratio design to achieve sufficient cell stability becomes difficult

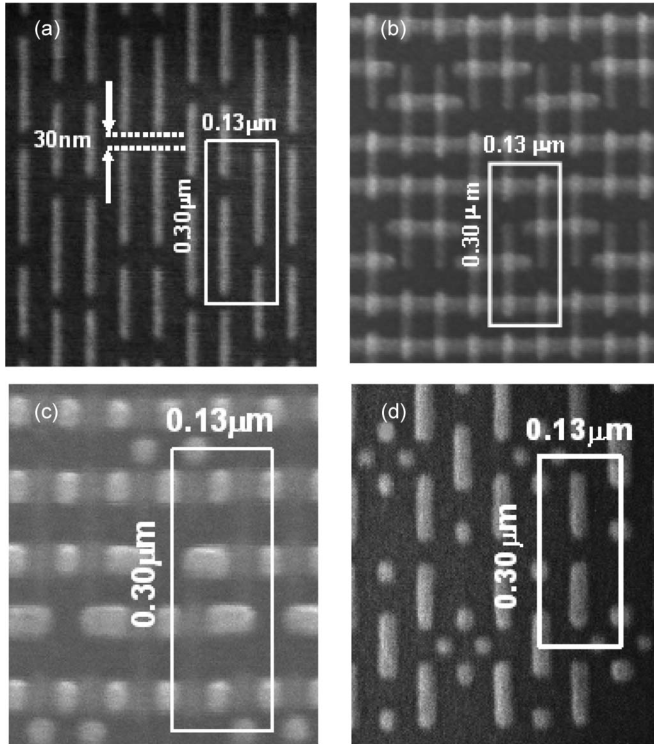

Fig. 10. SEM top views of (a) 6T- SRAM gate hard mask with 30-nm gate-to-gate spacing and 2-nm LWR formed by single NInL patterning, (b) 6T SRAM after gate etching, (c) three critical-layer superposition showing the active region, metal gate, and contact, and (d) metal-1 local interconnects.

due to increased variations in the device characteristics. The device variations are attributed to the CD control, LER, SCE control, and intrinsic dopant fluctuation, all contributing to the threshold voltage mismatch between the neighboring cell transistors and degrading SNM [17], [18]. In this paper, the SRAM cell with a straight active area is employed to minimize the V_t mismatch due to the geometry effect. However, the SNM of the cell is impacted due to the reduced beta ratio. To accommodate the low-beta-ratio cell design, this paper employs a DVR for SNM enhancement [19]. In contrast to the 8T-SRAM design [17], this DVR approach enhances the SNM by raising the cell voltage during read operations. Fig. 11 shows the simulation results and schematic to illustrate the benefit of the DVR. This process requires no cell and process changes, and the cell area is smaller than the 8T SRAM. These features are attractive to the scaled SRAM design. Fig. 12(a) shows the experimental results of a 0.039-μm^2 cell SNM with a 1.5-V DVR voltage. The simulation results indicate that SNM can further be improved after process optimization for external resistance and leakage reduction. Fig. 12(b) shows that the DVR provides a better SNM for a 6T-SRAM cell, particularly at lower V_{dd}.

Despite its simplicity and versatility, NInL lithography still has one critical challenge for mass production, which is throughput. Currently, NInL lithography uses similar exposure doses and is as high throughput as e-beam lithography, which uses hydrogen silsesquioxane (HSQ) as a resist for miniature pitch patterning. Although the throughput is not comparable with productive optical lithography, the high-resolution performance, lower investments, and lower maintenance costs make this technology attractive for low-volume CMOS devices

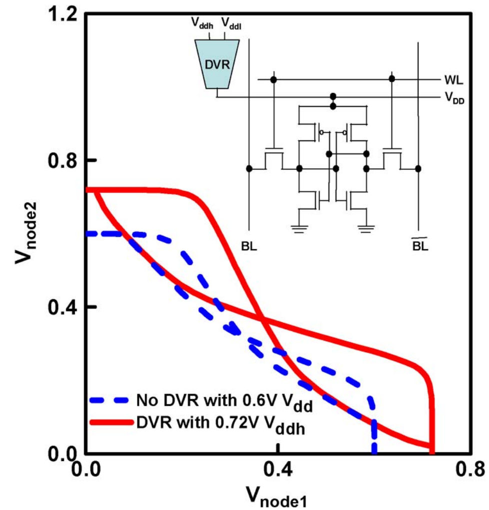

Fig. 11. 6T-SRAM SNM improvement by the DVR. The inset shows the schematic of the DVR.

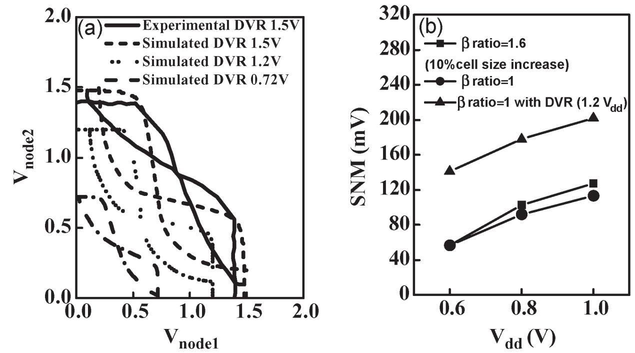

Fig. 12. (a) Measured and simulated butterfly curves of the 0.039-μm^2 6T SRAM. (b) Simulated SNM versus V_{dd} for various beta ratios with and without the DVR. The DVR greatly increases SNM, particularly at low V_{dd}.

and circuit design demonstrations. Because NInL lithography requires no photoresist intermediate, it increases freedom for mix-lithography applications that combine optical lithography and gas-assisted deposition. Fig. 5(a) shows a mix-lithography example using I-line lithography and NInL lithography for nanowire and its S/D pad patterning. For the layout combining both large and fine patterns such as S/D pad, i-line lithography can be used first to form a large pattern. The fine pattern can subsequently be obtained using NInL lithography. From SEM investigation after an anisotropic etching process, which is shown in Fig. 5(b), the result shows that NInL-lithography-deposited Pt layers have etch selectivity comparable to Pt layers produced through a photoresist. Thus, mix lithography can save the processing time of NinL. On the other hand, in a dual-beam system, ion-beam-induced deposition can be employed to save the processing time for some specific patterning. Fig. 13 shows the Si nanowire device metal-gate patterning using the dual-beam deposition approach. In this case, low-energy e-beam deposition can be used for ultrascaled gate hard-mask deposition. Conversely, ion-beam-induced deposition can be used for the gate electrode pad formation for test probe landings. Because the device pads were normally located in the isolation region, the energetic-ion incident would not damage the device active area. Furthermore, as the deposition rate increased in ion-beam

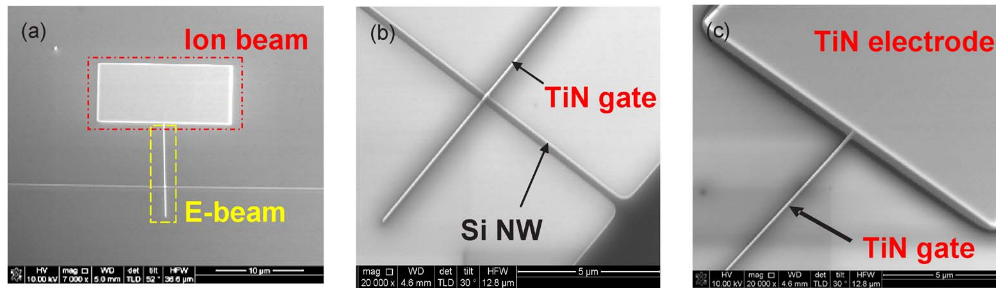

Fig. 13. (a) Tilt-angle SEM view of Pt hard-mask deposition using dual beams for nanowire device gate patterning. (b) Tilt-angle SEM view after TiN etching. The resulting TiN gate pattern is obtained by using e-beam-deposited Pt as an etch hard mask. (c) Tilt-angle SEM view of the device gate to electrode pad region after TiN etching.

deposition, the processing time and steps could significantly be reduced by dual-beam deposition for ultrascaled device fabrication.

IV. Conclusion

This paper has successfully demonstrated a maskless photoresist- and electron resist-free one-step patterning technology called NInL, with 16-nm SRAM fabrication. The NInL technique has demonstrated a nonoptical patterning capability of 40-nm line pitch and less than 2-nm 3-sigma LWR without employing proximity effect correction techniques. The NInL technology employs a similar exposure dose as in high throughput compared to the e-beam lithography using HSQ as a resist. NInL is a versatile technology. It can deposit a hard mask for a subsequent etch step, or it can directly deposit a metal pattern for interconnects or a dielectric pattern. Its simplicity and versatility makes NInL a promising technology for early evaluation or low-volume fabrication of 16-nm devices and circuits. By integrating the NInL technique, a single TiN gate material, and a nanowire FinFET device structure, a record area size of 0.039 μm^2 for a functional 6T-SRAM cell is demonstrated. To accommodate low-beta-ratio cell design and achieve good SNM, a DVR is employed to enhance the SNM, which is particularly beneficial for low-V_{dd} operation. NInL is a low-cost low-throughput option for device and circuit verification at the 16-nm node and beyond.

Acknowledgment

The authors would like to thank the National Nano Device Laboratories (NDL), Hsinchu, Taiwan, where research work for this paper was performed.

References

[1] *Semiconductor Industry Association (SIA), International Technology Roadmap for Semiconductors*, SIA: San Jose, CA, 2009.

[2] T. Ito and S. Okazaki, "Pushing the limits of lithography," *Nature*, vol. 406, no. 31, pp. 1027–1031, Aug. 2000.

[3] M. Kameyama, M. McCallum, and S. Owa, "Evolution of wavelength shrinkage in lithography," *Proc. SPIE*, vol. 7281, pp. 728 102-1–728 102-6, May 2009.

[4] B. Wu and A. Kumar, "Extreme ultraviolet lithography: A review," *J. Vac. Sci. Technol. B*, vol. 25, no. 6, pp. 1743–1762, Nov. 2007.

[5] V. S. Basker, T. Standaert, H. Kawasaki, C.-C. Yeh, K. Maitra, T. Yamashita, J. Faltermeier, H. Adhikari, H. Jagannathan, J. Wang, H. Sunamura, S. Kanakasabapathy, S. Schmitz, J. Cummings, A. Inada, C.-H. Lin, P. Kulkarni, Y. Zhua, J. Kuss, T. Yamamoto, A. Kumara, J. Wahl, A. Yagishita, L. F. Edge, R. H. Kim, E. Mclellan, S. J. Holmes, R. C. Johnson, T. Levin, J. Demarest, M. Hane, M. Takayanagi, M. Colburn, V. K. Paruchuri, R. J. Miller, H. Bu, B. Doris, D. McHerron, E. Leobandung, and J. O'Neill, "A 0.063-μm^2 FinFET SRAM cell demonstration with conventional lithography using a novel integration scheme with aggressively scaled fin and gate pitch," in *VLSI Symp. Tech. Dig.*, 2010, pp. 19–20.

[6] M. A. Guillorna, J. Chang, A. Pyzyna, S. Engelmann, E. Joseph, B. Fletcher, C. Cabral, Jr., C.-H. Lin, A. Bryant, M. Darnon, J. Ott, C. Lavoie, M. Frank, L. Gignac, J. Newbury, C. Wang, D. Klaus, E. Kratschmer, J. Bucchignano, B. To, W. Graham, I. Lauer, E. Sikorski, S. Carter, V. Narayanan, N. Fuller, Y. Zhang, and W. Haensch, "Trigate 6T SRAM scaling to 0.06 μm^2," in *IEDM Tech. Dig.*, 2009, pp. 961–963.

[7] M. A. Guillorn, J. Chang, A. Pyzyna, S. Engelmann, M. Glodde, E. Joseph, R. Bruce, J. A. Ott, A. Majumdar, F. Liu, M. Brink, S. Bangsaruntip, M. Khater, S. Mauer, I. Lauer, C. Lavoie, Z. Zhang, J. Newbury, E. Kratschmer, D. P. Klaus, J. Bucchignano, B. To, W. Graham, E. Sikorski, V. Narayanan, N. Fuller, and W. Haensch, "A 0.021-μm^2 trigate SRAM cell with aggressively scaled gate and contact pitch," in *VLSI Symp. Tech. Dig.*, 2011, pp. 64–65.

[8] A. Veloso, S. Demuynck, M. Ercken, A. M. Goethals, S. Locorotondo, F. Lazzarino, E. Altamirano, C. Huffman, A. De Keersgieter, S. Brus, M. Demand, H. Struyf, J. De Backer, J. Hermans, C. Delvaux, B. Baudemprez, T. Vandeweyer, F. Van Roey, C. Baerts, D. Goossens, H. Dekkers, P. Ong, N. Heylen, K. Kellens, H. Volders, A. Hikavyy, C. Vrancken, M. Rakowski, S. Verhaegen, M. Dusa, L. Romijn, C. Pigneret, A. Van Dijk, R. Schreutelkamp, A. Cockburn, V. Gravey, H. Meiling, B. Hultermans, S. Lok, K. Shah, R. Rajagopalan, J. Gelatos, O. Richard, H. Bender, G. Vandenberghe, G. P. Beyer, P. Absil, T. Hoffmann, K. Ronse, and S. Biesemans, "Demonstration of scaled 0.099-μm^2 FinFET 6T-SRAM cell using full-field EUV lithography for (sub-) 22-nm node single-patterning technology," in *IEDM Tech. Dig.*, 2009, pp. 301–304.

[9] V. Auzelyte, C. Dais, P. Farquet, D. Gruetzmacher, L. J. Heyderman, S. Olliges, C. Padeste, P. K. Sahoo, T. Thomson, A. Turchanin, C. David, and H. H. Solak, "Extreme ultraviolet interference lithography at the Paul Scherrer Institut," *J. Micro/Nanolith. Mems MOEMS*, vol. 8, no. 2, pp. 021 204-1–021 204-10, Jun. 2009.

[10] H. Duan, D. Winston, J. K. W. Yang, B. M. Cord, V. R. Manfrinato, and K. K. Berggren, "Sub-10-nm half-pitch electron-beam lithography by using poly(methyl methacrylate) as a negative resist," *J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct.*, vol. 28, no. 6, pp. C6 C58–C6 C62, Nov. 2010.

[11] T. E. Allen, R. R. Kunz, and T. M. Mayer, "Monte Carlo calculation of low-energy electron emission from surfaces," *J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct.*, vol. 6, no. 6, pp. 2057–2060, Nov. 1988.

[12] I. Utke, P. Hoffmann, and J. Melngailis, "Gas-assisted focused electron beam and ion beam processing and fabrication," *J. Vac. Sci. Technol. B: Microelectron. Nanometer Struct.*, vol. 26, no. 4, pp. 1197–1276, Jul. 2008.

[13] W. F. van Dorp, B. van Someren, C. W. Hagen, and P. Kruit, "Approaching the resolution limit of nanometer-scale electron-beam-induced deposition," *Nano Lett.*, vol. 5, no. 7, pp. 1303–1307, Jul. 2005.

[14] L. van Kouwen, A. Botman, and C. W. Hagen, "Focused electron-beam-induced deposition of 3-nm dots in a scanning electron microscope," *Nano Lett.*, vol. 9, no. 5, pp. 2149–2152, May 2009.

[15] H.-Y. Chen, C.-C. Chen, F.-K. Hsueh, J.-T. Liu, C.-Y. Shen, C.-C. Hsu, S.-L. Shy, B.-T. Lin, C.-S. Wu, C.-H. Chien, C. Hu, C.-C. Huang, and F.-L. Yang, "16-nm functional 0.039- μm^2 6T-SRAM cell with nano injection lithography, nanowire channel, and full TiN gate," in *IEDM Tech. Dig.*, 2009, pp. 958–961.

[16] B. S. Haran, A. Kumar, L. Adam, J. Chang, V. Basker, S. Kanakasabapathy, D. Horak, S. Fan, J. Chen, J. Faltermeier, S. Seo, M. Burkhardt, S. Burns, S. Halle, S. Holmes, R. Johnson, E. McLellan, T. M. Levin, Y. Zhu, J. Kuss, A. Ebert, J. Cummings, D. Canaperi, S. Paparao, J. Arnold, T. Sparks, C. S. Koay, T. Kanarsky, S. Schmitz, K. Petrillo, R. H. Kim, J. Demarest, L. F. Edge, H. Jagannathan, M. Smalley, N. Berliner, K. Cheng, D. LaTulipe, C. Koburger, S. Mehta, M. Raymond, M. Colburn, T. Spooner, V. Paruchuri, W. Haensch, D. McHerron, and B. Doris, "22-nm-technology-compatible fully functional 0.1-μm^2 6T-SRAM cell," in *IEDM Tech. Dig.*, 2008, pp. 625–628.

[17] L. Chang, D. M. Fried, J. Hergenrother, J. W. Sleight, R. H. Dennard, R. K. Montoye, L. Sekaric, S. J. McNab, A. W. Topol, C. D. Adams, K. W. Guarini, and W. Haensch, "Stable SRAM cell design for the 32-nm node and beyond," in *VLSI Symp.Tech. Dig.*, 2005, pp. 128–129.

[18] F. L. Yang, J. R. Hwang, and Y. Li, "Electrical characteristic fluctuations in sub-45-nm CMOS devices," in *Proc. IEEE CICC*, 2006, pp. 691–694.

[19] F.-S. Lai and C.-F. Lee, "On-chip voltage downconverter to improve SRAM read/write margin and static power for subnano CMOS technology," *IEEE J. Solid-State Circuit*, vol. 42, no. 9, pp. 2061–2070, Sep. 2007.

[20] C. C. Huang, C. C. Chen, F. K. Hsueh, C. Y. Shen, C. C. Hsu, C. S. Wu, H. Y. Chen, and F. L. Yang, "Sub-15-nm nanowire FETs and nanogap devices fabricated by electron-beam nano injection lithography (EBNIL)," in *Proc. Eur. MRS Conf.*, Spring 2010, p. 12.5.

[21] S. Natarajan, M. Armstrong, M. Bost, R. Brain, M. Brazier, C.-H. Chang, V. Chikarmane, M. Childs, H. Deshpande, K. Dev, G. Ding, T. Ghani, O. Golonzka, W. Han, J. He, R. Heussner, R. James, I. Jin, C. Kenyon, S. Klopcic, S.-H. Lee, M. Liu, S. Lodha, B. McFadden, A. Murthy, L. Neiberg, J. Neirynck, P. Packan, S. Pae, C. Parker, C. Pelto, L. Pipes, J. Sebastian, J. Seiple, B. Sell, S. Sivakumar, B. Song, K. Tone, T. Troeger, C. Weber, M. Yang, A. Yeoh, and K. Zhang, "A 32-nm logic technology featuring 2nd-generation high-k + metal-gate transistors, enhanced channel strain and 0.171- μm^2 SRAM cell size in a 291-Mb array," in *IEDM Tech. Dig.*, 2008, pp. 941–944.

[22] S. Y. Wu, C. W. Chou, C. Y. Lin, M. C. Chiang, C. K. Yang, M. Y. Liu, L. C. Hu, C. H. Chang, P. H. Wu, C. I. Lin, H. F. Chen, S. Y. Chang, S. H. Wang, P. Y. Tong, Y. L. Hsieh, P. Y. Tong, J. J. Liaw, K. H. Pan, C. H. Hsieh, C. H. Chen, J. Y. Cheng, C. H. Yao, W. K. Wan, T. L. Lee, K. T. Huang, C. C Chen, K. C. Lin, L. Y. Yeh, K. C. Ku, S. C. Chen, C. W. Chang, H. J. Lin, S. M. Jang, Y. C. Lu, J. H. Shieh, M. H. Tsai, J. Y. Song, K. S. Chen, V. Chang, S. M. Cheng, S. H. Yang, C. H. Diaz, Y. C. See, and M. S. Liang, "A 32-nm CMOS low-power SoC platform technology for foundry," in *IEDM Tech. Dig.*, 2007, pp. 263–266.

[23] F. L. Yang, D. H. Lee, H. Y. Chen, C. Y. Chang, S. D. Liu, C. C. Huang, T. X. Chung, H. W. Chen, C. C. Huang, Y. H. Liu, C. C. Wu, C. C. Chen, S. C. Chen, Y. T. Chen, Y. H. Chen, C. J. Chen, B. W. Chan, P. F. Hsu, J. H. Shieh, H. J. Tao, Y. C. Yeo, Y. Li, J. W. Lee, P. Chen, M. S. Liang, and C. Hu, "5-nm-gate nanowire FinFET," in *VLSI Symp. Tech. Dig.*, 2004, pp. 196–197.

Hou-Yu Chen, photograph and biography not available at the time of publication.

Chun-Chi Chen, photograph and biography not available at the time of publication.

Fu-Kuo Hsueh, photograph and biography not available at the time of publication.

Jan-Tsai Liu, photograph and biography not available at the time of publication.

Shyi-Long Shy, photograph and biography not available at the time of publication.

Cheng-San Wu, photograph and biography not available at the time of publication.

Chao-Hsin Chien, photograph and biography not available at the time of publication.

Chenming Hu, photograph and biography not available at the time of publication.

Chien-Chao Huang, photograph and biography not available at the time of publication.

Fu-Liang Yang, photograph and biography not available at the time of publication.