Read Characteristics of Independent Double-Gate Poly-Si Nanowire SONOS Devices

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***Abstract*—This paper investigates the read operation of poly-Si nanowire silicon–oxide–nitride–oxide–silicon devices with independent double-gate (IDG) configuration. The device features oxide–nitride–oxide (ONO) stack as the charge storage medium in one of the two gated sides with pure oxide in the other. Owing to the IDG feature, the shift in the device's transfer characteristics due to a change in the amount of storage charges can be sensed with two different modes, which have one of the two gates applied with a sweeping bias (driving gate) and the other with a fixed bias (control gate). Our analysis and experimental data show that a larger memory window is obtained when the gate of the ONO side is used as the driving gate. Moreover, the memory window of this mode is essentially independent of the bias applied to the control gate. Based on this finding, a novel Flash structure featuring IDG cells with a common control gate is proposed.**

***Index Terms*—Independent double gate (IDG), nanowire (NW), poly-Si, read disturb, silicon–oxide–nitride–oxide–silicon (SONOS).**

I. Introduction

RECENTLY, driven by the tremendous increase in the demand of portable electronic products, the market of semiconductor nonvolatile memory, which is dominated by the floating-gate (FG) Flash technology, has been rapidly growing. However, the aggressive scaling of FG Flash devices has encountered some serious challenges, including reliability issues caused by stress-induced leakage current, as well as critical short-channel and FG coupling effects [1]–[4]. Several types of devices with a nonvolatile property, including phase-change memory [5], ferroelectric and magnetoresistive memory [6], [7], and silicon–oxide–nitride–oxide–silicon (SONOS) [8]–[11] memory have been proposed to overcome these scaling issues. Among these options, SONOS devices built with a multiple-gate (MG) poly-Si nanowire (NW) channel are very appealing due to their great potential for realizing 3-D monolithic integration of memory devices. A good example is the bit-cost scalable (BICs) Flash technology with the advantage of ultrahigh density and reduced bit cost [12], [13]. These previous studies have shown that the use of an ultrathin NW channel can help relieve inherent threshold voltage $V_{\rm th}$ fluctuation problem caused by the grain boundaries contained in the poly-Si film. On the other hand, the adoption of MG schemes can enhance the gate controllability and increase the device's immunity to the short-channel effects. Among a number of MG configurations, the independent double-gate (IDG) scheme is particularly worth studying [14]–[18]. Such scheme provides high flexibility in $V_{\rm th}$ adjustment; therefore, the demands for high ON-state current $I_{\rm on}$ and low OFF-state current $I_{\rm off}$ are achievable [14]. Recently, we have proposed and developed a novel IDG NW poly-Si thin-film transistor [15]–[17] and also applied it to forming a SONOS device [18]. In our study, an oxide–nitride–oxide (ONO) was used as the gate dielectric for one of the independent gates, whereas a gate oxide layer was used for the other gate. Our study showed that greatly enhanced program/erase (P/E) speed can be obtained with appropriate IDG bias conditions as the channel is sufficiently thin [18]. A similar IDG SONOS structure can be found in the work of Walker [19] who demonstrated that the read–pass disturb can be suppressed. In this paper, we further study the read characteristics of IDG NW poly-Si SONOS devices. Special attention is paid on the operation of different read modes and the impact on memory window. Based on the results, a novel scheme is proposed for future high-density Flash memory application.

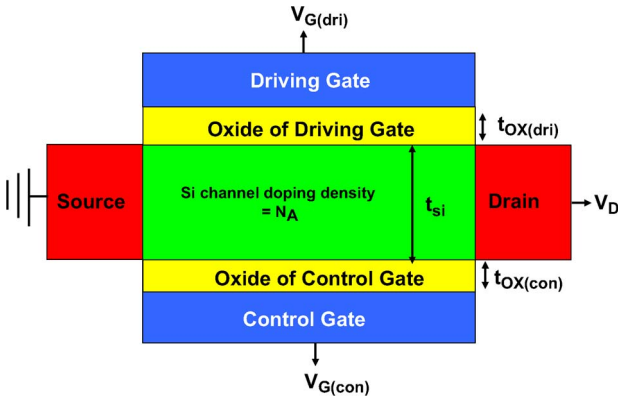

Fig. 1. Schematic structure of the n-type IDG device for analysis.

II. Theoretical Analysis

The 2-D simplified structure of the n-type IDG silicon device is shown in Fig. 1. During measurements, the gate bias applied to the driving gate is swept to obtain the transfer characteristics, whereas a fixed voltage is applied to the control gate [18]. Fig. 2 illustrates the simplified $V_{\rm th}$ characteristics of the device

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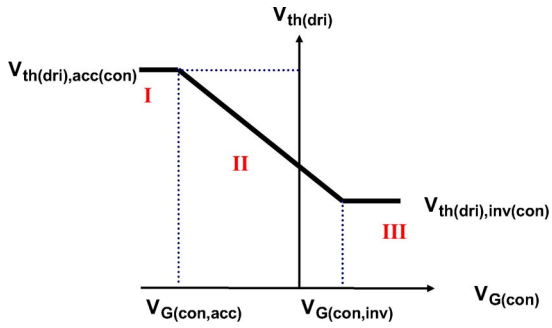

Fig. 2. $V_{\mathrm{th(dri)}}-V_{G(\mathrm{con})}$ characteristics of the n-type IDG device. Three distinctly different regions corresponding to various channel surface conditions of the control gate side can be defined.

$V_{\mathrm{th(dri)}}$ as a function of the control gate bias $V_{G(\mathrm{con})}$. According to the theory developed by Lim and Fossum [20], [21], the above V_{th} characteristics can be divided into three regions, as indicated in the figure. In regions I and III, the channel surface of the control gate side is respectively accumulated and inverted; thus, the V_{th} of the driving gate is pinned at $V_{\mathrm{th(dri)},\mathrm{acc(con)}}$ and $V_{\mathrm{th(dri)},\mathrm{inv(con)}}$ and can be expressed as

$$V_{\mathrm{th(dri)},\mathrm{acc(con)}} = V_{\mathrm{FB(dri)}} + \left(1+\frac{C_{\mathrm{si}}}{C_{\mathrm{ox(dri)}}}\right)2\phi_B - \frac{Q_{\mathrm{depl}}}{2C_{\mathrm{ox(dri)}}} \tag{1}$$

$$V_{\mathrm{th(dri)},\mathrm{inv(con)}} = V_{\mathrm{FB(dri)}} + 2\phi_B - \frac{Q_{\mathrm{depl}}}{2C_{\mathrm{ox(dri)}}} \tag{2}$$

respectively, where $V_{\mathrm{FB(dri)}}$ is the flatband voltage of the driving gate, $C_{\mathrm{si}} = \varepsilon_0\varepsilon_{\mathrm{si}}/t_{\mathrm{si}}$ is the silicon depletion capacitance, $Q_{\mathrm{depl}} = qN_At_{\mathrm{si}}$ is the total charges in the depleted Si film, $\phi_B = (kT/q)ln(N_A/n_i)$ is the Fermi potential of the Si channel, and $C_{\mathrm{ox(dri)}} = \varepsilon_0\varepsilon_{\mathrm{ox}}/t_{\mathrm{ox(dri)}}$ is the gate oxide capacitance of the driving gate. In addition, N_A is the doping density in the silicon film, t_{si} is the thickness of the silicon film, kT/q is the thermal energy, and n_i is the intrinsic carrier concentration. In region II, the channel surface of the control gate side is depleted, and the $V_{\mathrm{th(dri)}}$ can be adjusted by the applied $V_{G(\mathrm{con})}$. Boundaries of these regions are at $V_{G(\mathrm{con,acc})}$ and $V_{G(\mathrm{con,inv})}$, which represent the onsets of the accumulated and inverted surfaces of the control gate, respectively, and can be expressed as

$$V_{G(\mathrm{con,acc})} = V_{\mathrm{FB(con)}} - \frac{C_{\mathrm{si}}}{C_{\mathrm{ox(con)}}}2\phi_B - \frac{Q_{\mathrm{dep}}}{2C_{\mathrm{ox(con)}}} \tag{3}$$

$$V_{G(\mathrm{con,inv})} = V_{\mathrm{FB(con)}} + 2\phi_B - \frac{Q_{\mathrm{dep}}}{2C_{\mathrm{ox(con)}}} \tag{4}$$

where $V_{\mathrm{FB(con)}}$ and $C_{\mathrm{ox(con)}} = \varepsilon_0\varepsilon_{\mathrm{ox}}/t_{\mathrm{ox(con)}}$ are the flatband voltage of the control gate and oxide capacitance, respectively. As $V_{G(\mathrm{con})}$ increases from $V_{G(\mathrm{con,acc})}$ to $V_{G(\mathrm{con,inv})}$, $V_{\mathrm{th(dri)}}$ is linearly decreased from $V_{\mathrm{th(dri)},\mathrm{acc(con)}}$ to $V_{\mathrm{th(dri)},\mathrm{inv(con)}}$; therefore, the V_{th} of the driving gate in region II can be expressed as

$$V_{\mathrm{th(dri)},\mathrm{depl(con)}} = V_{\mathrm{th(dri)},\mathrm{acc(con)}} - \left(\frac{C_{\mathrm{si}}C_{\mathrm{ox(con)}}}{C_{\mathrm{ox(dri)}}\left(C_{\mathrm{si}}+C_{\mathrm{ox(con)}}\right)}\right)\left(V_{G(\mathrm{con})}-V_{G(\mathrm{con,acc})}\right). \tag{5}$$

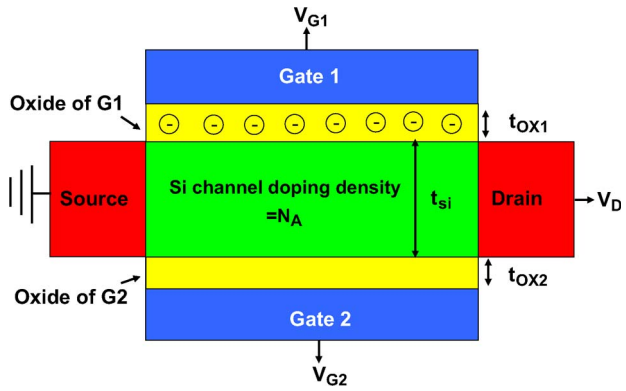

Fig. 3. Schematic structure of the n-type IDG devices with extra negative charges incorporated in the gate oxide of G1.

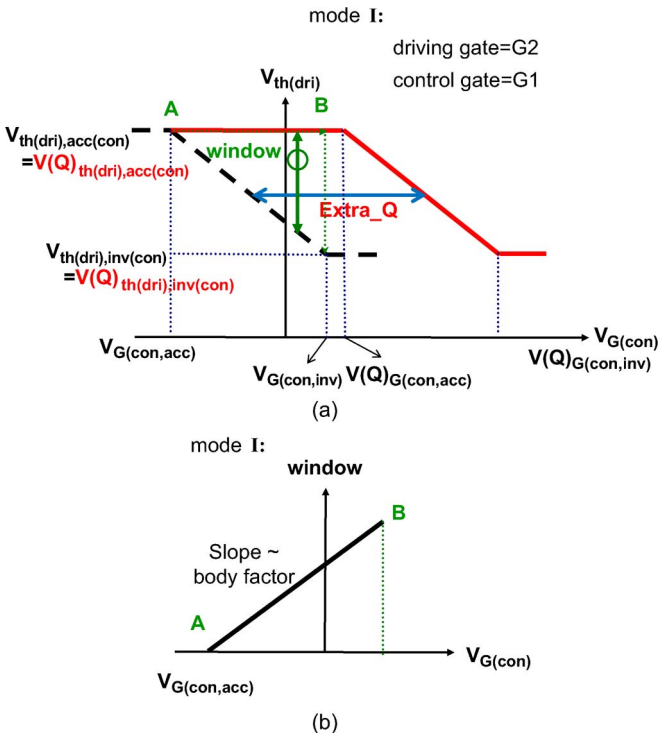

Fig. 4. (a) $V_{\mathrm{th(dri)}}$ versus $V_{G(\mathrm{con})}$ characteristics and (b) memory window versus $V_{G(\mathrm{con})}$ read in mode I with or without extra charges incorporated.

Furthermore, its slope is defined as the body factor β, which is expressed as

$$\beta = \frac{C_{\mathrm{si}}C_{\mathrm{ox(con)}}}{C_{\mathrm{ox(dri)}}\left(C_{\mathrm{si}}+C_{\mathrm{ox(con)}}\right)}. \tag{6}$$

Next, we consider another situation shown in Fig. 3, which has two independent gates denoted as gate 1 (G1) and gate 2 (G2), and an amount of negative charges is contained in the gate oxide of G1. Since the two gates can be independently operated, two read modes can be applied. In mode I, the device is driven by G2, whereas G1 serves as the control gate to adjust $V_{\mathrm{th(dri)}}$. The $V_{\mathrm{th2(dri)}}-V_{G1(\mathrm{con})}$ characteristics in mode I are shown in Fig. 4(a), where the solid and dashed lines are individually related to the cases with and without the aforementioned extra fixed charges. The dashed line is the same as the one shown in Fig. 2. As shown in the figure, the $V_{\mathrm{th2(dri)}} - V_{G1(\mathrm{con})}$

curve with the extra charges shows a parallel shift toward the positive direction of the applied bias of G1, which serves as the control gate in mode I. This is because of the positive shift of the G1's flatband voltage resulting from the incorporated fixed charges at the gate oxide of G1. According to (3) and (4), the voltages correspond to the onsets of the accumulated and inverted surfaces of G1 with negative charges contained in the gate oxide of G1, which are denoted as $V(Q)_{G1(\mathrm{con,acc})}$ and $V(Q)_{G1(\mathrm{con,inv})}$, can be expressed as [23]

$$V(Q)_{G1(\mathrm{con,acc})} = V_{G1(\mathrm{con,acc})} - \frac{qQ}{C_{\mathrm{ox1}}} \tag{7}$$

$$V(Q)_{G1(\mathrm{con,inv})} = V_{G1(\mathrm{con,inv})} - \frac{qQ}{C_{\mathrm{ox1}}} \tag{8}$$

$$Q = \frac{\int_0^{t_{\mathrm{ox1}}} x\rho\, dx}{t_{\mathrm{ox1}}} \tag{9}$$

where t_{ox1}, x, and ρ individually mean the oxide thickness of G1, position, and charge density of the charges in the gate oxide of G1. The difference in V_{th} between the two characteristic curves in Fig. 4(a) is defined as the memory window. Due to the right shift caused by the incorporated charges, the memory window operated in the region between points A and B is shown in Fig. 4(b), which shows a linear relation with respective to the bias of control gate V_{G1}. In addition, its slope is determined by body factor β [see (6)]. Therefore, the memory window can be expressed as

$$\Delta V_{\mathrm{th}} = \beta\left(V_{G1} - V_{G1(\mathrm{con,acc})}\right) \tag{10}$$

$$\beta(\text{body factor}) = \frac{C_{\mathrm{si}}C_{\mathrm{ox1}}}{C_{\mathrm{ox2}}(C_{\mathrm{si}} + C_{\mathrm{ox1}})}. \tag{11}$$

Next, we examine the properties of mode II in which G1 and G2 serve as the driving and control gates, respectively. In other words, the roles of G1 and G2 in mode I are switched in the present case. The $V_{\mathrm{th1(dri)}}$–$V_{G2(\mathrm{con})}$ characteristics in mode II are shown in Fig. 5(a), where the solid and dashed lines are respectively related to the cases with or without negative charges contained in the gate oxide of G1. It should be noted that the extra fixed charges contained in the gate oxide of G1 have no influence on the surface conditions of the channel gated by G2. This means that the voltages corresponding to the onsets of the accumulated and inverted surfaces of the channel gated with G2 remain unchanged. However, it indeed affects the threshold voltage as G1 serves as the driving gate. As a result, a parallel shift toward the positive direction of the threshold voltage (y-axis) is observed in Fig. 5(a). Furthermore, the associated threshold voltages with negative charges contained in the gate oxide of G1 in mode II at the onsets of accumulation and inversion of the channel gated with G2, i.e., $V(\mathrm{Q})_{\mathrm{th1(dri),acc2}}$ and $V(\mathrm{Q})_{\mathrm{th1(dri),inv2}}$, respectively, can be expressed as

$$V_{\mathrm{th1(dri),acc2(con)}}(Q) = V_{\mathrm{th1(dri),acc2(con)}} - \frac{qQ}{C_{\mathrm{ox1}}}, \tag{12}$$

$$V_{\mathrm{th1(dri),inv2(con)}}(Q) = V_{\mathrm{th1(dri),inv2(con)}} - \frac{qQ}{C_{\mathrm{ox1}}}. \tag{13}$$

Fig. 5(b) shows the memory window operated in the region between points A and B shown in Fig. 5(a), which has no dependence on the gate bias of the control gate owing to

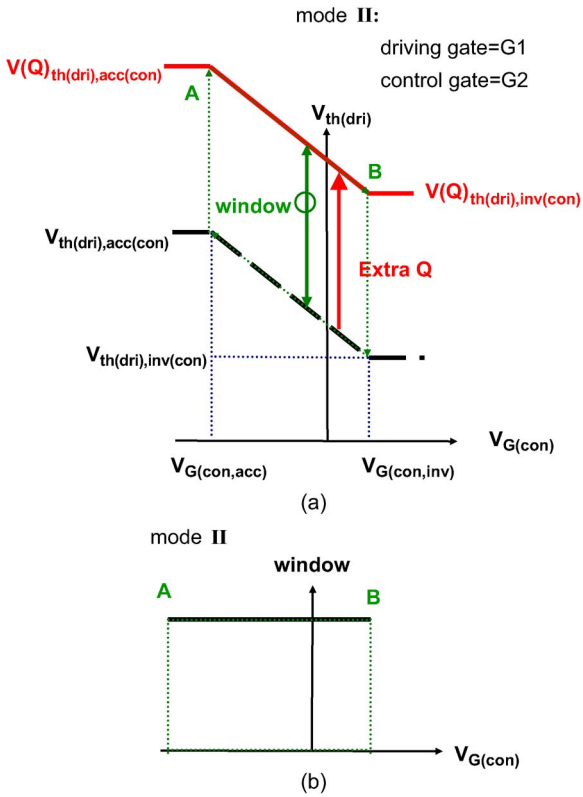

Fig. 5. (a) $V_{\mathrm{th(dri)}}$ versus $V_{G(\mathrm{con})}$ characteristics and (b) memory window versus $V_{G(\mathrm{con})}$ read in mode II with or without extra charges incorporated.

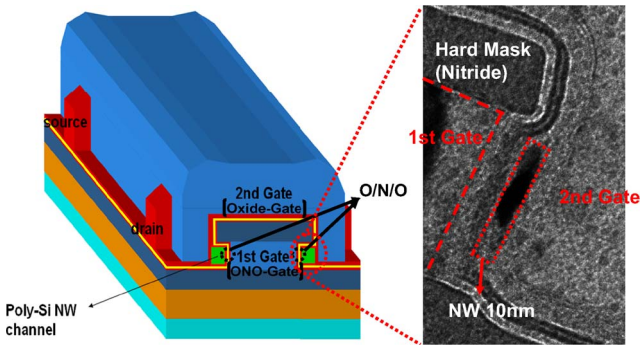

Fig. 6. Stereo view of the n-type IDG poly-Si NW SONOS device characterized in this paper. ONO and oxide are used as the gate dielectrics of the first and second gates, respectively.

the upward parallel shift with incorporation of electrons. The memory window is

$$\Delta V_{\mathrm{th}} = -\frac{qQ}{C_{\mathrm{ox1}}} \tag{14}$$

which is proportional to the amount of charges incorporated.

III. Experimental Results and Discussion

We employ a novel scheme that was previously developed [18] to explore the characteristics of the IDG SONOS devices and verify the theoretical model derived in the previous section. The schematic of the investigated structure and the cross-sectional transmission electron microscopic (TEM) image of a fabricated device are shown in Fig. 6. As shown in the figure,

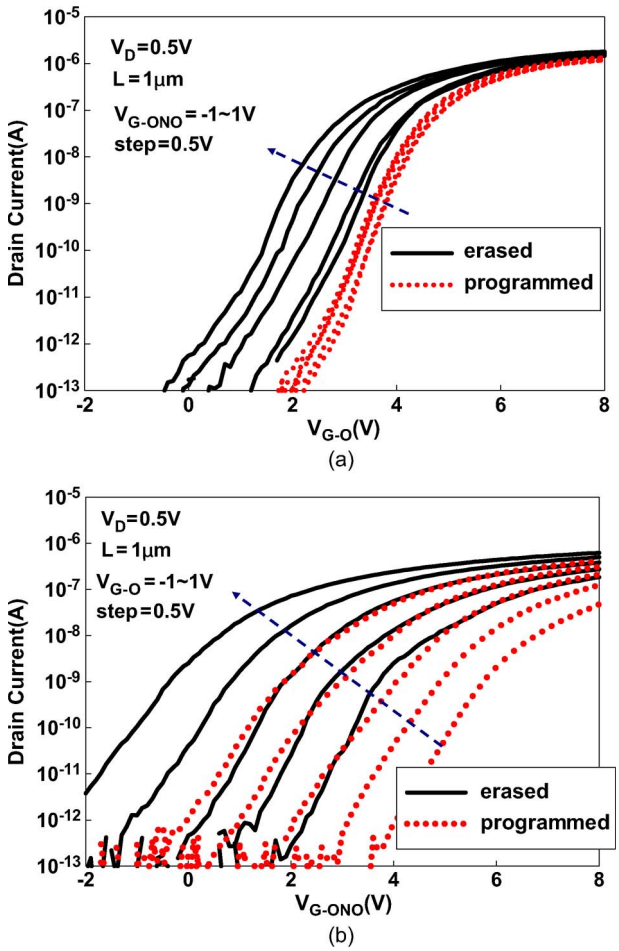

Fig. 7. Measured transfer characteristics of (dotted lines) the programmed and (solid lines) erased states in (a) mode I and (b) mode II.

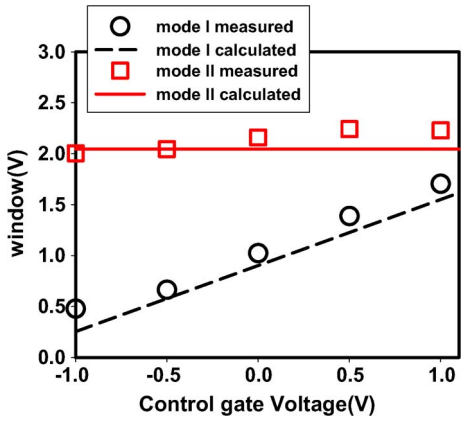

Fig. 8. Memory window's read in modes I and II. The dash and solid lines refer to calculated results for modes I and II, respectively, and the circle and square symbols are the extracted results from the transfer characteristics shown in Fig. 7(a) and (b), respectively.

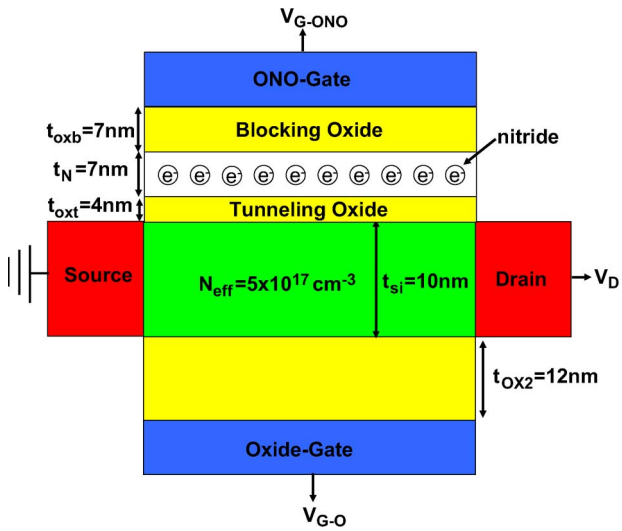

Fig. 9. Two-dimensional schematic structure of the n-type IDG poly-Si NW SONOS device, including detailed device parameters applied in the calculation.

the poly-Si NW channels are horizontally sandwiched by two independent gates denoted as the first and second gates. Basically, the structure and its fabrication flow are the same as those described in our previous work [16], except the replacement of the gate oxide of the first gate by an ONO (4 nm/7 nm/7 nm) stack. Thicknesses of the NW Si channel and the gate oxide of the second gate are 10 and 12 nm, respectively. In the following discussion, for simplicity, the first gate and its gate bias are denoted as the ONO gate and $V_{G-\mathrm{ONO}}$, respectively, whereas the second gate and its gate bias are the oxide gate and V_{G-O}, respectively. The device is programmed and erased using Fowler–Nordheim tunneling by applying a high gate bias to the ONO gate while the oxide gate, source, and drain are grounded. As aforementioned, due to the flexibility offered by the IDG configuration, two read modes depending on the choice of the driving gate are feasible. The I_D–V_G characteristics of the programmed and erased states measured under modes I and II are shown in Fig. 7(a) and (b), respectively. Programming was executed with $V_{G-\mathrm{ONO}} = 15$ V, $V_{G-O} = 0$ V, and $t = 5$ ms, and erasing was executed with $V_{G-\mathrm{ONO}} = -12$ V, $V_{G-O} = 0$ V, and $t = 20$ ms. The memory window is defined as the V_{th} difference between the erased and programmed states. Fig. 8 shows the results of the memory window for the two read modes extracted from the data shown in Fig. 7(a) and (b). Fig. 9 shows the simplified 2-D schematic SONOS structure with certain amount of electrons contained in the nitride layer. Detailed device parameters for the analysis are also included. In the figure, N_{eff} is the effective channel doping concentration resulting from the grain-boundary trapping centers in the poly-Si film [22] and is estimated to be about 5×10^{17} cm^{-3} [15].The difference of the present structure from that shown in Fig. 3 is the replacement of the gate oxide of G1 by the ONO stack; thus, the analytical form of the memory window given in (10) and (14) for modes I and II, respectively, can be applied if a modification in the oxide capacitance of G1 is made. The revised form, which is denoted as effective C_{ox1}, is expressed as

$$C_{\mathrm{ox1(eff)}} = \frac{\varepsilon_0 \varepsilon_{\mathrm{ox}}}{t_{\mathrm{oxt}} + \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_N} \times t_N + t_{\mathrm{oxb}}} \tag{15}$$

where t_{oxt}, t_N, and t_{oxb} are the thicknesses of the tunneling oxide, nitride, and blocking oxide, respectively, and ε_N is the nitride dielectric permittivity. As the amount of the trapped

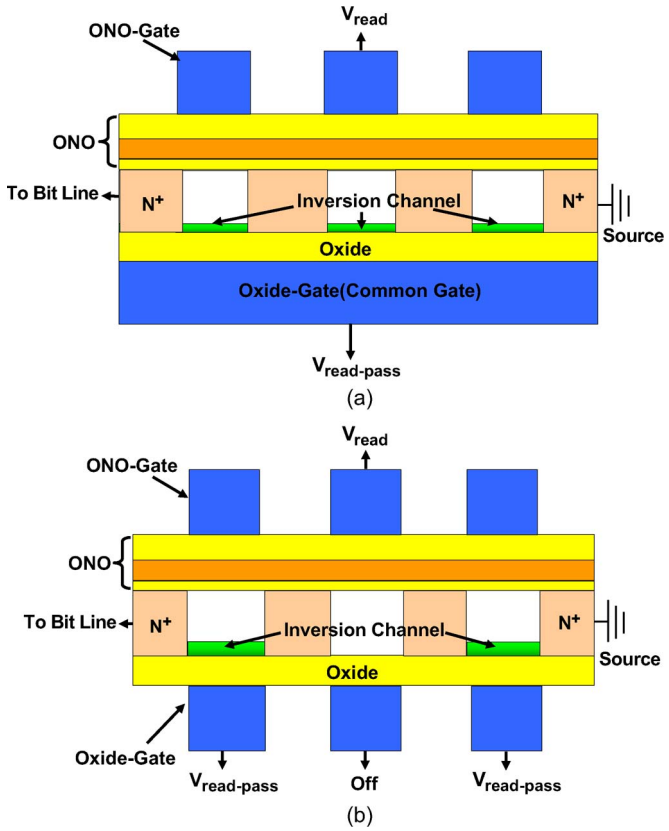

Fig. 10. (a) Proposed Flash structure consisted of a series string of IDG SONOS cell devices and a common control gate. (b) Previous structure consisted of a series string of IDG SONOS cell devices. Each cell has its own control gate.

electrons in the nitride layer shown in Fig. 9 is taken into account, (14) can be modified into the following form [24]:

$$\Delta V_{\rm th} = qQ_{\rm tot}\left(\frac{t_{\rm Box}}{\varepsilon_0\varepsilon_{\rm ox}} + \frac{t_N - x_{\rm mean}}{\varepsilon_0\varepsilon_N}\right) \tag{16}$$

$$Q_{\rm tot} = \int_0^{t_N} \rho\, dx \tag{17}$$

$$x_{\rm mean} = \frac{1}{Q_{\rm tot}}\int_0^{t_N} \rho x\, dx \tag{18}$$

where $Q_{\rm tot}$, $x_{\rm mean}$, $t_{\rm box}$, t_N, and ρ are the total amount of trapped electrons, trapped electrons' mean vertical position in the nitride, thickness of the blocking oxide, thickness of the nitride, and charge density of trapped electrons, respectively. By substituting the device parameters shown in Fig. 9 to the above equations, the individual memory windows in modes I and II can be calculated, and theoretical results are shown and compared with the experimental data in Fig. 8. According to the work of Lue *et al.* [24], most of the trapped electrons in the nitride layer distribute close to the middle of nitride. Therefore, $x_{\rm mean}$ and $Q_{\rm tot}$ used in the above calculation are set to be 3.5 nm and 5×10^{12} cm^{-2}, respectively. As shown in Fig. 8, the calculated results well describe the measured memory windows extracted from the I_D–V_G characteristics shown in Fig. 7(a) and (b).

The above theoretical analysis and experimental data indicate that the read operation of an IDG SONOS device prefers the mode with the ONO gate serving as the driving gate and the oxide gate as the control gate. Such a read mode acquires a memory window, which is larger than the other mode and independent of the bias applied to the control gate. Based on these features, we proposed a new SONOS Flash structure shown in Fig. 10(a). Before describing its major features and advantages, we first review a previous structure developed by Walker [19], as shown in Fig. 10(b). The cell devices in such a structure also adopt an ONO gate for charge storage and an oxide gate underneath the channel. During read operation, the oxide gates of the cells, except for the one to be accessed, are applied with a bias $V_{\rm read-pass}$ in order to reduce the parasitic series resistance. Such scheme can eliminate the necessity of applying a high bias to the ONO gates of the cells neighboring the accessed cell. As a result, the read–pass disturb can be effectively suppressed. One major issue associated with such a structure is the alignment of the top ONO gate to the bottom oxide gate in the cell devices, making fabrication complicated. Such a constraint can be relieved with the proposed scheme shown in Fig. 10(a), in which the SONOS cells in the series string share a common bottom oxide gate. During read operation, the common bottom oxide gate serves as the control gate and is applied with $V_{\rm read-pass}$, whereas the top ONO gate for the cell to be accessed is applied with $V_{\rm read}$. The top ONO gates of the neighboring cells are either floating or with a low voltage. Such a scheme is feasible because, based on the above analysis, the memory window is independent of $V_{\rm read-pass}$ applied to the bottom oxide gate. With the present scheme, not only the merit of the previous structure shown in Fig. 10(b) in eliminating the read–pass disturb can be retained but also the fabrication can be greatly simplified since the aforementioned demand on the precise alignment of the top and bottom gates can be lifted. Additional advantages of the proposed structure include the following: 1) Similar to the conventional DG structure [19]–[25], the common bottom gate provides electrostatically enhanced short-channel effect control, which is helpful for device scaling. 2) The P/E efficiency can be improved as an appropriate bias is applied to the bottom control gate, as has been demonstrated in one of our previous studies [18]. 3) Although not clearly depicted in Fig. 10(a), it is possible to eliminate the n^+ source/drain (S/D) regions by adopting the junction-free (JF) scheme that has been recently proposed [26], [27]. Such a scheme skips the S/D implant steps and utilizes the fringe field from the neighboring gates to induce an inversion layer in the junctionless S/D areas and reduce the series resistance therein. As the present IDG configuration adopts the JF scheme, fabrication can be further simplified. Moreover, the series resistance is expected to be lower than the previous JF versions [26], [27] as an appropriate bias is applied to the common gate. 4) Fabrication involves mainly mature poly-Si preparation techniques and has low thermal budget, making it suitable for monolithic 3-D integration. In addition, the concept is not restricted to the planar scheme shown in Fig. 10(a). If some modifications are made, it can be also applied to 3-D Flash structures with vertical-channel cell devices, such as the BICs [12], [13].

IV. Conclusion

The operation mechanisms of IDG poly-Si NW SONOS devices are characterized. The theoretical analysis indicates that the memory window is larger and independent of the bias applied to the control gate as the gate of the charge storage side is used as the driving gate for sensing $V_{\rm th}$. Such predictions are confirmed with the experimental results. Based on the above finding, a novel scheme containing a series string of JF SONOS cell devices with a common control gate is proposed for monolithic 3-D Flash application. Such a scheme can retain the inherent merits associated with the IDG configuration, such as good control over the short-channel effects, improved P/E efficiency, and suppressed read disturb. Furthermore, the implementation of the common control gate and JF features can greatly simplify the device fabrication and thus advancing the feasibility of poly-Si NW devices for future 3-D nonvolatile memory manufacturing.

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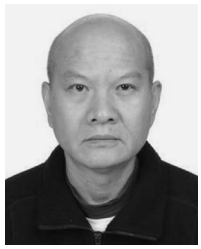

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