Effects of Channel Width and Nitride Passivation Layer on Electrical Characteristics of Polysilicon Thin-Film Transistors

Chia-Chun Liao, Min-Chen Lin, Tsung-Yu Chiang, and Tien-Sheng Chao

***Abstract*—SiN passivation layers were found to yield better performance, suppress the kink effect, and improve the gate leakage current and gate-induced drain leakage (GIDL) of polysilicon thin-film transistors (TFTs). The SiN passivation layers deposited under different deposition conditions possess different characteristics due to their varying passivation effect. A physical mechanism is proposed to explain the double-hump phenomenon induced by incomplete trap passivation. Based on the analysis of width dependence, the better performance of the samples with SiN passivation layers was attributed not only to radical passivation of the defect states but also to radical passivation of preexisting defects in the gate oxide. Furthermore, using SiN passivation layers improves immunity to positive gate bias stress, negative gate bias stress, and hot-carrier stressing. Moreover, the manufacturing processes are simple (without the long processing time plasma treatment requires) and compatible with TFT processes.**

***Index Terms*—Gate-induced drain leakage (GIDL), grain boundary, intragrain, kink effect, radical.**

I. Introduction

RECENTLY, polycrystalline silicon (poly-Si) thin-film transistors (TFTs) have attracted much attention due to their application in active-matrix liquid crystal displays. Furthermore, there has been increasing interest in developing techniques for optimizing poly-Si TFTs because such devices are promising for high vertical density components in applications where the high mobility of single-crystal MOSFETs is not mandatory. The transfer characteristics of poly-Si TFTs strongly depend on defects in the intragrain, grain boundary, and the gate dielectric. The deep states, which originate from the dangling bonds in grain boundaries, influence the threshold voltage and the subthreshold swing, whereas tail states, which originate from the intragrain defects, affect the field-effect mobility and the minimum leakage current [1], [2]. In order to achieve superior characteristics for poly-Si TFTs, many techniques to optimize the device performance by reducing the trap density or increasing the grain size of polysilicon have been proposed [3]. Therefore, passivation of these defects may improve the threshold voltage, subthreshold swing, and mobility characteristics.

Hydrogen passivation by hydrogen plasma treatment has been proposed as an effective way to improve TFT performance. However, poly-Si TFTs with hydrogen plasma treatment suffer a severe hot-carrier issue due to weak Si–H bonds. Therefore, NH_3, F, and N_2 have been proposed to improve the immunity of the hot carrier by creating strong bonds, which are more difficult to break than Si–H bonds during hot-carrier stressing [4]–[8]. Nevertheless, the additional time necessary for plasma treatment is an important issue to overcome.

Silicon nitride film is one of the most promising materials for coating and passivation films used in electronic devices and mechanical parts [9]. It has been reported that SiN layers can improve the performance of bulk-silicon MOSFETs [10], fully depleted silicon-on-insulator MOSFETs [11], and amorphous Si (a-Si) TFTs [12]. Furthermore, using a silicon nitride passivation layer is effective for suppression of the I–V kink in heterojunction field-effect transistors since the radicals can passivate defects, leading to a reduction in the trapping/detrapping process [13]. It has been reported that using a plasma-deposited SiN layer as a high-concentration diffusion source of atomic hydrogen is a promising approach for improving the performance of poly-Si TFTs [14]. However, few complete investigations of poly-Si TFTs with SiN passivation layers have been reported.

On the other hand, an appropriate choice of molecular fraction of nitrogen mixed with hydrogen is known to be effective in further enhancing the improvement in the plasma discharge [15]. However, the effect of the flow rate of different reactant gases on the deposition of the SiN layer for passivation of poly-Si TFTs has yet to be systematically investigated. In studying the impact of SiN deposition conditions on single-crystal MOSFETs, Lu *et al.* proposed that reducing the flow rate of the diluent gas as nitrogen results in better improvement in the interface state due to passivation by hydrogen radicals [16]. In this paper, we find that the deposition conditions of the SiN passivation layers affect the characteristics of the poly-Si TFT.

Plasma passivation requires a very long hydrogenation time ($>$ 4 h) to passivate the strain-bond-related tail state [2]. To enable fabrication of useful transistors without additional processing time, this paper investigates the effects of SiN passivation layers on the electrical characteristics of TFTs. The deposition

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TABLE I
REACTANT AND DILUENT GAS FLOW RATES USED TO INVESTIGATE THE EFFECT OF DIFFERENT NITRIDE PASSIVATION LAYERS

	N_2-low	N_2-med	N_2-high	SiH_4-high
N_2 (sccm)	50	100	1000	100
NH_3 (sccm)	6	6	6	6
SiH_4 (sccm)	50	50	50	100

time of the nitride passivation layer is less than 10 min, enabling significant passivation of the tail state, deep state, and trap inside the gate dielectric. As a result, TFTs with SiN passivation layers not only exhibit improved initial TFT performance but also enhanced immunity to positive gate bias stress (PGBS), negative gate bias stress (NGBS), and hot-carrier stressing.

II. EXPERIMENTS

The poly-Si TFTs studied in this paper were prepared as follows: an a-Si film of 500 Å was deposited at 500 °C by low-pressure chemical vapor deposition (CVD) on thermally oxidized wafers. The wafers were annealed at 600 °C for 24 h to transform the amorphous film into poly-Si, and the poly-Si films were patterned into active islands. After removal of the surface oxide, 30-nm-thick tetraethyl orthosilicate (TEOS) oxide was deposited at 680 °C. A 2000-Å-thick poly-Si layer was deposited and patterned as the gate electrode, which also serves as the mask for self-aligned implantation. The source/drain and gate regions were then implanted by phosphorous (15 keV at 5×10^{15} cm^{-2}) and activated at 600 °C for 24-h annealing in a N_2 ambient. The SiN layers were deposited under four different deposition conditions by plasma-enhanced CVD (PECVD) with the same thickness of 3000 Å. The control sample was skipped in this step. Power, pressure, and temperature were set at 100 W, 137 Pa, and 300 °C, respectively. Table I shows the reactant and diluent gas flow rates used to investigate the effect of the nitride passivation layer. The samples were labeled N_2-low, N_2-med, N_2-high, and SiH_4-high. A 2000-Å PECVD oxide was then deposited at 300 °C in 2.5 min for all TFTs capped with a nitride passivation layer. For comparison, a PECVD oxide (5000 Å) passivation layer was deposited at 300 °C in 6.3 min on the control sample. Hence, all samples have passivation layers of identical thickness. After patterning of the contact holes, aluminum was deposited by physical vapor deposition and patterned as the probe pads to complete the TFT devices. For comparison, some devices underwent post-SiN-deposition thermal annealing in nitrogen at 350 °C for 60 min.

III. RESULTS AND DISCUSSION

A. Performance

Fig. 1 shows the I_D–V_G curves of n-channel TFTs for the control sample and the samples with the SiN passivation layer. The channel length and width are both 10 μm. It is evident that n-channel TFTs exhibit improved performance with the capped SiN layer, as compared to control samples. The threshold

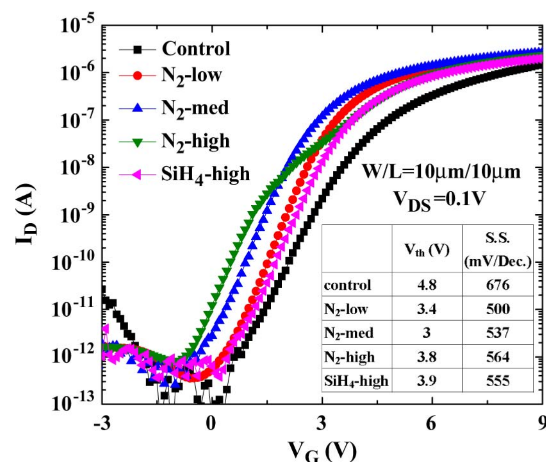


Fig. 1. Transfer characteristics (I_D–V_G) of n-channel TFTs with different passivation layers.

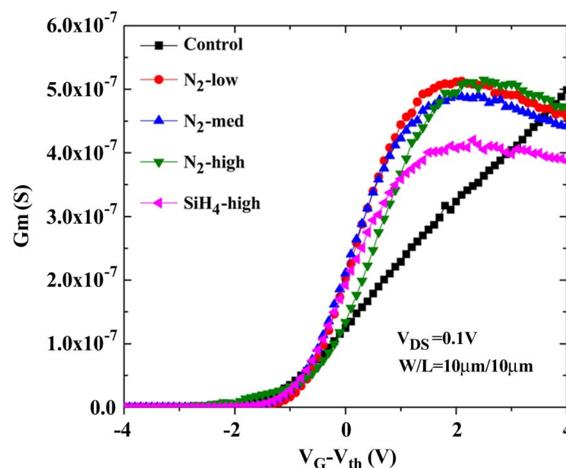


Fig. 2. Transconductance of n-channel TFTs with different passivation layers.

voltage and subthreshold swing are improved compared to the control sample, meaning that using SiN passivation appears to effectively terminate the dangling bonds in the poly-Si and SiO_2/poly-Si interface. Furthermore, the gate-induced drain leakage (GIDL) is suppressed for the poly-Si TFTs with SiN capping compared to the control sample, which is attributed to trap passivation. The N_2-high sample possesses the highest subthreshold swing, whereas the SiH_4-high sample possesses the lowest peak transconductance, as shown in Fig. 2. In contrast, the control sample possesses no peak transconductance due to the hole trapping. The N_2-med and N_2-low samples possess better transfer characteristics.

The aforementioned results indicate that the deposition conditions of SiN passivation layers affect the characteristics of poly-Si TFTs. Both the NH_3 and N_2 plasma passivation processes effectively improve TFT transfer characteristics by plasma discharge. However, NH_3 plasma treatment is more effective than N_2 plasma treatment because the hydrogen radicals are most effective for passivating the grain boundary and trap states [6]–[8]. In this paper, during the deposition of SiN, the hydrogen and nitrogen radicals diffuse and passivate intragrain and grain-boundary trap state in poly-Si by forming Si–H and Si–N bonds. The reactant gas of NH_3 can generate the hydrogen

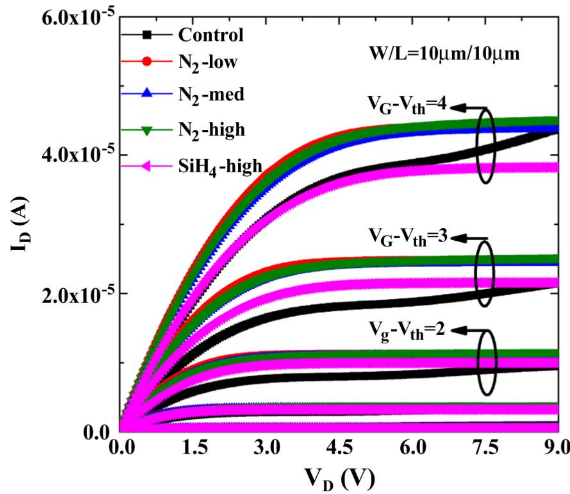


Fig. 3. Output characteristics (the I_D–V_D curve) of n-channel TFTs with different passivation layers.

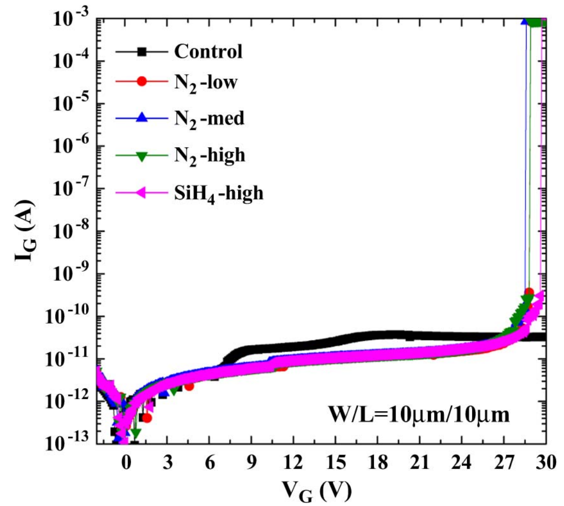


Fig. 4. Gate leakage current of n-channel TFTs for all samples.

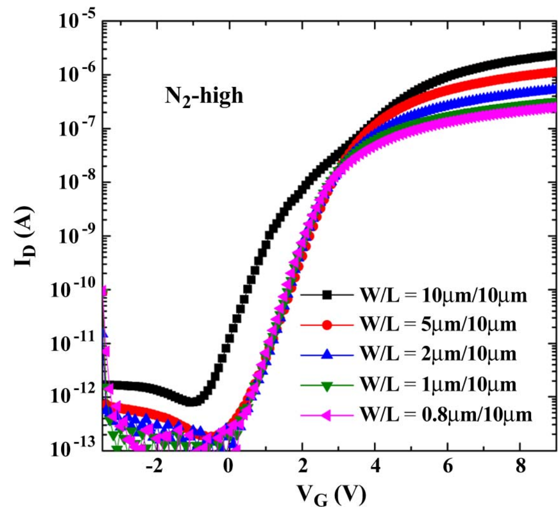


Fig. 5. Transfer characteristics (I_D–V_G) for the N_2-high sample with different channel widths.

and nitrogen radicals, and the reactant gas of N_2 plasma can generate only the nitrogen radicals. As a result, the deposition condition of SiN has a significant influence on the generation of radicals and on poly-Si TFT device performance.

Fig. 3 shows the drain-current-versus-drain-voltage (I_D–V_D) characteristics of all n-channel poly-Si TFTs. There are three distinct features of these characteristics. At low overdrive voltage, all samples capped with SiN exhibit better performance than the control sample due to passivation of the tail state. As the overdrive voltage is further increased, however, the control sample has better performance than the SiH_4-high sample due to hole trapping at higher gate voltage (discussed later). At higher drain biases, the "kink" effect is much more pronounced for the control sample than its counterparts. We believe that trap passivation is responsible for the suppressed kink effect. There are several models for the explanation of pronounced kink effect by trap. Kim *et al.* demonstrated that the kink effect depends on the nature of surface states [17]. Hack and Lewis proposed that the presence of grain boundaries or traps in poly-Si TFTs significantly enhanced the kink effects in poly-Si TFTs, as compared to single-crystal counterparts [18]. Kumar *et al.* predicted that the local electric field near the irregular surface due to grain boundaries can be appreciably greater than the average electric field, which can initiate additional impact ionization [19]. Thus, the reduced trap induced by the radicals is a reasonable explanation for the suppression of the kink effect.

A high-quality gate oxide and interface between the gate oxide and the poly-Si channel are critical for transfer characteristics. Due to the nature of TEOS oxide, there are more dangling bonds and weak Si–O and Si–Si bonds in the bulk oxide and in the interface between the gate oxide and the poly-Si channel. Fig. 4 shows the gate leakage characteristics for all samples. The TFTs capped with SiN layers possess lower leakage than the control sample, indicating that using SiN passivation layers is an effective way to improve gate oxide quality. It has been reported that large amounts of nitrogen exist in oxynitride films. This enables formation of strong $\mathrm{Si} \equiv \mathrm{N}$ bonds in the oxynitride/poly-Si interface, which can improve gate leakage and charge trapping [20], [21]. Furthermore, NH_3 and H_2 plasma treatments are effective in improving gate leakage [22]. Thus, passivation of defects in the bulk oxide, nitrogen pileup at the oxide/poly-Si interface, and improved interface state condition by nitrogen radicals are responsible for improving gate leakage during SiN deposition. As a result, using SiN passivation layers enables termination of both traps in the poly-Si channel and preexisting traps in the gate oxide by radicals.

B. Width Dependence of TFT Capped Nitride Passivation

The transfer characteristics of the N_2-high sample exhibit a double hump, as shown in Fig. 1, implying that hydrogen and nitrogen radical propagation is less effective. In order to clarify the double-hump phenomenon of the N_2-high sample, we compared the transfer characteristics of the N_2-high samples of different channel widths, as shown in Fig. 5. The double hump in the subthreshold region indicates the secondary conduction path for the device with a width of 10 μm. As the width is scaled down, the double-hump phenomenon is suppressed.

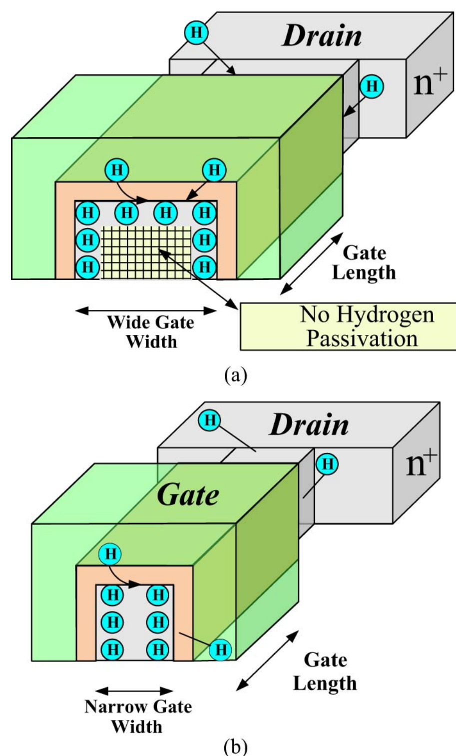


Fig. 6. (a) Cross section of n-channel TFTs with wider channel widths. Incomplete trap passivation is also indicated and is responsible for the double-hump phenomenon. (b) Cross section of n-channel TFTs with narrower channel widths. Complete trap passivation appears to suppress the double-hump phenomenon.

A physical mechanism is proposed to explain the early turn-on phenomenon for the device with a width of 10 μm. It is noted that the number of defects and available radicals affects the efficiency of passivating defects [1]. Trap passivation is not complete for the entire poly-Si channel for devices with a wider channel width, as shown in Fig. 6(a). A portion of the poly-Si channel, which was passivated by nitrogen or hydrogen radicals, has a lower local threshold voltage than the unpassivated portions of the channel, resulting in a nonuniform threshold voltage. Moreover, the nonuniform threshold voltage exhibits the early turn-on phenomenon. As the channel width is scaled down, the portion of the poly-Si channel without passivation by radicals is minimized, as shown in Fig. 6(b), and the double-hump phenomenon is suppressed since the radicals can diffuse and passivate the trap effectively.

In order to clarify the width effect on the devices' electrical characteristics, a detailed investigation of the parameters of the poly-Si TFTs is necessary. Again, the threshold voltage, subthreshold swing, and maximum mobility strongly depend on the grain, grain boundaries, and interface properties. As shown in Fig. 7(a), TFTs capped with SiN passivation layers possess better subthreshold swing than the control sample for all dimensions, and the N_2-low and SiH_4-high samples have the lowest subthreshold swing. All samples with SiN passivation layers possess saturated features. These results indicate that passivation of the deep state in the grain boundary is efficient; hence, the decrease in the subthreshold swing is less dependent on the variation in channel width. Fig. 7(b) demonstrates the threshold voltage as a function of width. Threshold voltage $V_{\rm th}$ is defined as the gate voltage required to achieve a normalized drain current of $I_D = (W/L) \times 100$ nA at $V_{DS} = 0.1$ V. The threshold voltage of the control sample decreases as the width is scaled down since the gate control is further increased with decreasing of the channel width due to corner portion domination [23]. In contrast, the improvement in the threshold voltage increases as the width shrinks for TFTs with capped SiN passivation layers. Wu *et al.* found that the subthreshold swing monotonically decreases with hydrogenation, similar to the response of the threshold voltage [2]. However, the improvement in the subthreshold swing does not display strong dependence on the channel width in this paper. Thus, we believe that not only increased passivation of the deep state but also increased passivation of preexisting defects in the gate oxide are the mechanisms by which the threshold voltage improves as the width is scaled down. It has been reported that the dominant pathway for hydrogen diffusion into the active poly-Si film may be through the gate oxide, where the diffusivity of hydrogen is much higher than in the poly-Si layer [1], [24]. Thus, passivation of the preexisting traps by hydrogen or nitrogen radicals is reasonable. As the channel width is scaled down, the portion of the poly-Si channel without passivation by radicals is minimized, resulting in more radical pileups at the oxide/poly-Si interface. Passivation of preexisting traps in the gate oxide becomes more efficient as channel width narrows, which is responsible for the improvement in the threshold voltage. The increase in mobility, along with the channel width decrease, is observed in Fig. 7(c). Two mechanisms may explain mobility's dependence on the channel width. The first mechanism is the improvement in the interface state condition and enhanced passivation of the tail state in the poly-Si channel film at narrow channel widths. The second possible cause is the lower impact of the grain boundaries. At wider channel width, the SiH_4-high sample has the lowest mobility, meaning that the SiH_4-high sample has the lowest tail state passivation among all samples. The mobility for all TFTs capped with the SiN passivation layer becomes comparable at narrow channel widths. We believe that passivation of the tail state by the SiN passivation layer increases as the width falls, becoming similar for all nitride conditions at narrow channel widths, because the defects can be effectively passivated when a sufficient number of radicals is supplied.

In general, the improvements in threshold voltage and mobility by nitride passivation become more significant as channel width is scaled down, because hydrogen or nitrogen radicals can terminate the strain bonds and more efficiently passivate the preexisting defects in the bulk oxide and interface. Moreover, the H_2 plasma easily passivates dangling bonds in the grain boundaries to reduce the midgap deep states, whereas a very long hydrogenation time (> 4 h) is required to passivate the strain-bond-related tail state [2]. This theory is consistent with the effect of using a SiN passivation layer. In this paper, using a SiN passivation layer passivates the deep states and the strain-related tail state. Passivation of the deep states is rapidly saturated since the improvement in the subthreshold swing stays almost constant for all channel widths. On the other hand, the difference in mobility decreases for TFTs with different SiN passivation layers as the width is scaled down, meaning that

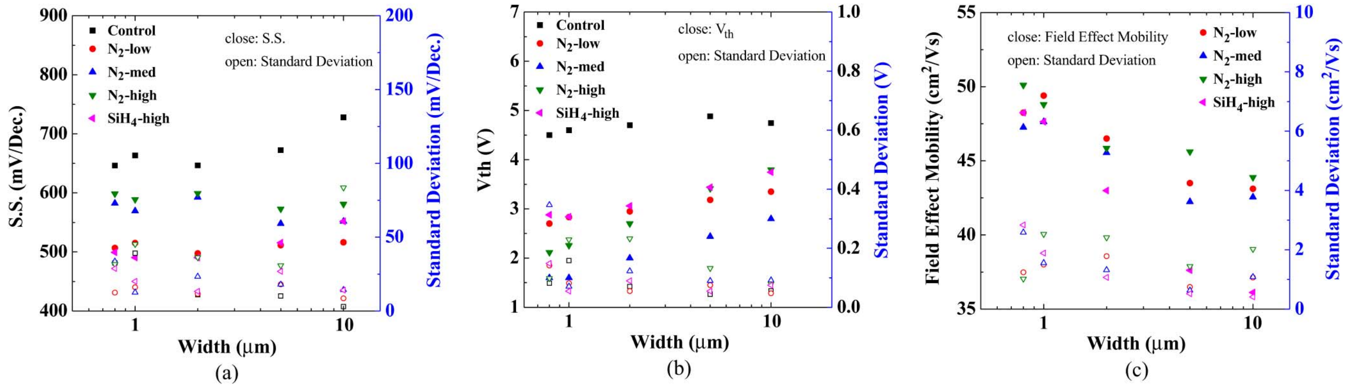


Fig. 7. (a) Variation of subthreshold swing as a function of channel width for $L = 10\ \mu$m with different passivation layers. (b) Variation of threshold voltage as a function of channel width for $L = 10\ \mu$m with different passivation layers. (c) Variation of field mobility as a function of channel width for $L = 10\ \mu$m with different passivation layers.

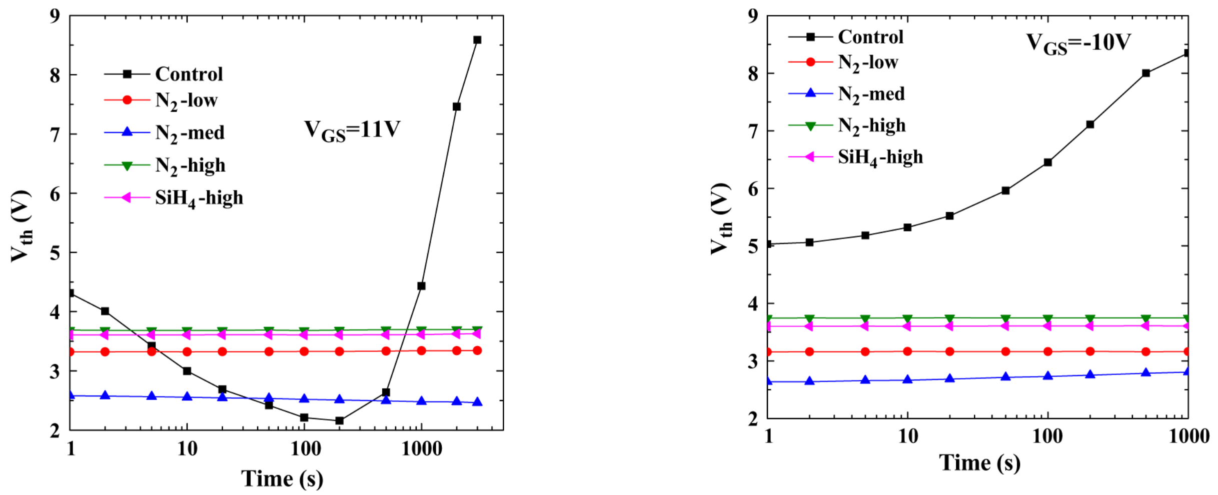


Fig. 8. Threshold voltage shift as a function of stress time for n-channel TFTs under PGBS as $V_{GS} = 11$ V.

Fig. 9. Threshold voltage shift as a function of stress time for n-channel TFTs under NGBS as $V_{GS} = -10$ V.

passivation of the tail state is slow compared to passivation of the deep state.

C. PGBS, NGBS, and Hot-Carrier Stressing

Another important issue in poly-Si TFTs is reliability. The PGBS, NGBS, and hot-carrier stressing often degrade the reliability of TFT devices. PGBS was carried out at $V_{DS} = 0$ V and $V_{GS} = 11$ V for 3000 s to examine the device reliability, as shown in Fig. 8. Tunneling of hot holes from the gate into the substrate may be responsible for positive charge trapping in the control sample during the initial stressing period, and electron trapping would then become the dominant trapping mechanism [25]. By contrast, samples capped with SiN passivation layers have smaller shift in threshold voltage than the control sample. NGBS was carried out at $V_{DS} = 0$ V and $V_{GS} = -10$ V for 1000 s to examine the device reliability, as shown in Fig. 9. The control sample exhibits significant electron trapping, whereas TFTs capped with SiN passivation layers show improved electron trapping. These results show that using SiN passivation layers can improve the immunity of PGBS and NGBS.

Fig. 10(a) shows the dependence of dc hot-carrier degradation at a drain voltage V_D of 18 V on overdrive voltage $(V_G - V_{\mathrm{th}})$ for all samples, where I_{on} is a drain current I_D at V_G of 9 V and $V_D = 0.1$ V, $I_{\mathrm{on}0}$ is the initial value of I_{on}, and ΔI_{on} is the decrease in I_{on} after 1000 s of stress. For bulk silicon, the worst dc hot-carrier degradation occurs when stress condition V_G is about half of V_D. However, the worst case stress condition of the TFT is lower than that of the bulk silicon. Toyota *et al.* found that the worst stress condition is $V_{GS} = 2$ V at $V_{DS} = 10$ V [26]. In this paper, we found the lowest degradation at $V_{GS} - V_{\mathrm{th}} = 5$ V. Thus, we believe that the significant degradation of drain current below $V_{GS} - V_{\mathrm{th}} = 5$ V is attributable to hot-carrier-induced damage, and the degradation of drain current above $V_{GS} - V_{\mathrm{th}} = 5$ V is attributable to PGBS-induced damage. In contrast, samples capped with SiN passivation layers show slight variation in the drain current (below 5%). The threshold voltage shift and the relative variation of transconductance of TFTs with and without SiN passivation layers are shown in Fig. 10(b) and (c), respectively. Samples capped with SiN passivation layers exhibit improved threshold voltage shift and mobility degradation. The improved immunity of hot-carrier stressing for samples with SiN passivation layers is comparable to that for samples with plasma treatment in the literature [27], [28].

We found that TFTs capped with SiN passivation layers show improved immunity to PGBS, NGBS, and hot-carrier stressing. We believe that this improvement is due to passivation of

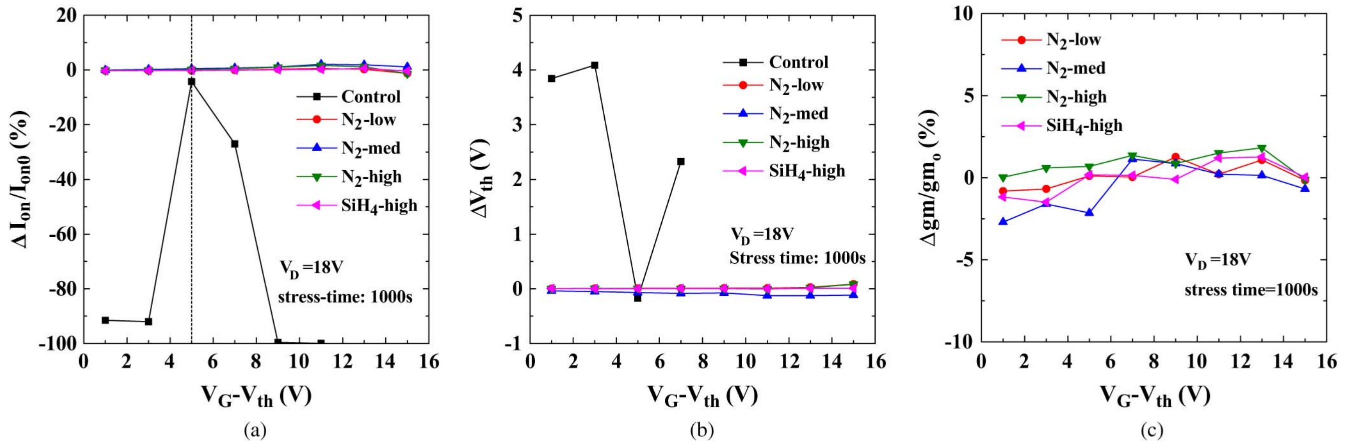
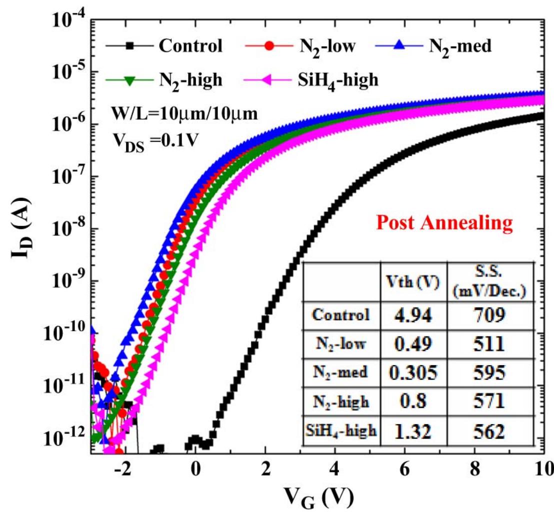


Fig. 10. (a) Dependence of I_{on} degradation under dc stress on gate voltage for all samples. (b) Dependence of V_{th} degradation under dc stress on gate voltage for all samples. (c) Dependence of transconductance degradation under dc stress on gate voltage for all samples.



	Vth (V)	S.S. (mV/Dec.)
Control	4.94	709
N2-low	0.49	511
N2-med	0.305	595
N2-high	0.8	571
SiH4-high	1.32	562

Fig. 11. Transfer characteristics (I_D–V_G) of n-channel TFTs with different passivation layers after postannealing.

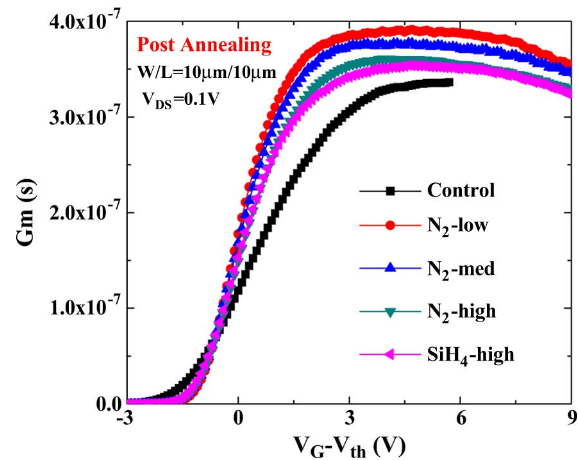


Fig. 12. Transconductance of n-channel TFTs with different passivation layers after postannealing.

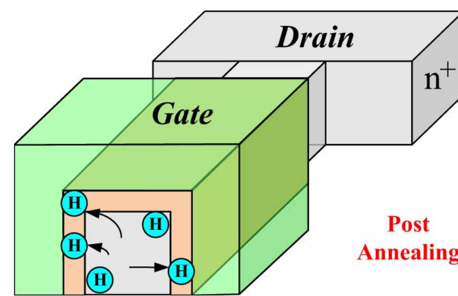


Fig. 13. Mechanism of hydrogen instability induced by postannealing.

traps in the grain boundaries, intragrain, and TEOS oxide with strong Si $\equiv$ N bonds during deposition of the SiN passivation layer [29].

D. *Post-*SiN*-Deposition Thermal Annealing*

It has been reported that the improvement by using hydrogen radicals to passivate the defects would degrade during postannealing, indicating the limits on thermal cycling after the hydrogenation process [30]. Fig. 11 shows the I_D–V_G curves of n-channel TFTs for the control sample and the samples with the SiN passivation layers after post-SiN-deposition thermal annealing. The channel length and width are both 10 μm. The threshold voltage would decrease after postannealing for samples with the SiN passivation layers; however, the threshold voltage of the control sample is comparable to the original value. In addition, the characteristics of subthreshold swing are relatively insensitive to postannealing. Fig. 12 shows the characteristics of transconductance after post-SiN-deposition thermal annealing. For TFTs with the SiN passivation layers, the treatment of postannealing would degrade the transconductance and passivation of tail states, indicating that using SiN passivation layers also suffers the limits on thermal cycling after the deposition of SiN. A physical mechanism is proposed to explain the hydrogen instability induced by postannealing, as shown in Fig. 13. We believe that postannealing would break passivation of tail states created by hydrogen, as compared with deep states, because hydrogen bonding in dangling bonds is far stronger than in the tail states (about 2 eV) [2]. The break of passivation of tail states would induce the degradation of transconductance. The hydrogen may diffuse into the gate oxide, and decrease the threshold voltage subsequently.

IV. Conclusion

Using an SiN passivation layer has been found to yield better performance, suppress the kink effect, and improve GIDL for poly-Si TFTs without the long hydrogenation time required by plasma treatment. TFTs capped with different SiN passivation layers show differences in their performance improvements since different mechanisms are involved. We found that moderating the N_2 flow rate can make a better improvement than moderating the SiH_4 flow rate due to better improvement in mobility. Additionally, a mechanism to explain the double-hump phenomenon induced by incomplete trap passivation for SiN deposited with high flow rates of nitrogen has been proposed.

All samples with SiN passivation layers exhibit saturated improvement of the subthreshold swing. However, the characteristics of mobility become comparable across all samples at narrow channel widths. This shows that the subthreshold swing improvement, which is affected by the deep states, has a more rapid response to radical diffusion than the mobility improvement induced by tail state passivation.

Furthermore, using SiN passivation layers exhibits excellent reliability characteristics. We believe that passivation of traps in the grain boundaries, intragrain, and TEOS oxide with strong $Si \equiv N$ bonds is responsible for the improved gate leakage and reliability.

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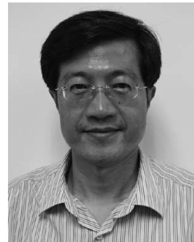

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