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Effective Mobility Enhancement by Using Nanometer Dot Doping in Amorphous IGZO Thin-Film Transistors

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With a high mobility (>10 $cm^2 V^{-1} s^{-1}$) and a low threshold voltage (<5 V) in low-temperature processes, transparent oxide semiconductor thin-film transistors (TOS TFTs) have drawn considerable attention due to their applications on flexible displays, level shifters, drivers, and pixel-driving circuits for active-matrix organic light-emitting-diode (AMOLED) displays.[1–3] In addition to display applications, amorphous indium gallium zinc oxide (a-IGZO) TFTs are also promising for the development of radio-frequency identification (RFID) tags, smart cards, and other types of flexible electronics. When TOS TFTs are developed for a low-power high-frequency circuit, high electron mobility and a low parasitic capacitance are required. Most TFTs fabricated with ZnO, SnO_2, In_2O_3, IGZO, or other semiconducting oxide thin films exhibit electron mobilities smaller than 35 $cm^2 V^{-1} s^{-1}$.[4–6] Recent reports on transparent oxide nanowire transistors (NWTs) have demonstrated high electron mobilities approximately 70 to 4000 $cm^2 V^{-1} s^{-1}$.[7–9] The quasi-1D structure of NWTs may reduce low-angle carrier scattering to produce high electron mobility.[9] However, the fabrication process of NWTs has poor reproducibility and is still not practical for real-world applications. Because TOS transistors are transparent, developing TOS circuits on windows is appealing. Particularly, for modern buildings or trains with series of windows, TOS RFID circuits on windows can deliver various types of signals through a low-power transmission system. In this type of application, the dimension of the transparent transistor can be large because an integrated circuit on a small chip is not necessary. A low-cost production method for delivering a high-performance TOS transistor is a critical challenge.

Here, a nanostructure to improve the effective mobility in a-IGZO TFTs is proposed. A large channel dimension of 1000 μm, defined by a shadow mask, is utilized. The nanostructure is developed using a low-cost, lithography-free process to produce abundant nanometer-scale dot-like doping in a-IGZO channel. The new method, called nanodot doping (NDD) increases the effective electron mobility to a level 19 times higher than that of the control and the intrinsic electron mobility is also 10 times higher than that of the control. This study demonstrates a process utilizing self-organized polystyrene spheres with a diameter of 200 nm to fabricate a porous gate structure. Ar plasma treatment through the porous gate performs dot-like doping on a-IGZO channel region. A top-gate self-aligneda-IGZO TFT with an effective field-effect mobility as 79 $cm^2 V^{-1} s^{-1}$ (an intrinsic electron mobility as 39.6 $cm^2 V^{-1} s^{-1}$) is realized. The top-gate (TG) self-aligned structure also eliminates the overlaps between the gate electrode and the source/drain contacts, which are known to suppress the parasitic capacitance and increase the response speed. The influences of dot and doping concentrations on device performance are also discussed. The application of NDD treatment on conventional bottom-gate (BG) a-IGZO TFTs is also demonstrated. After NDD treatment, a twofold improvement in electron mobility in a conventional bottom-gate a-IGZO TFT is observed.

Top-gate (TG) structures with NDD and without NDD (named STD hereafter) were fabricated. Two device structures called "TG-STD" (top-gate without NDD) and "TG-NDD" (top-gate with NDD) are depicted in **Figure 1**a,b, respectively. The scanning electron microscopy (SEM) image of the cross-sectional view of the channel region of TG-NDD device is shown in Figure 1c. Openings with 200 nm diameter can be observed in the channel region.

The process flow of fabricating TG-NDD is shown in **Figure 2**a. A 30-nm-thick a-IGZO (3-in. circular target: In:Ga:Zn = 1:1:1 at%) was deposited by radio-frequency (RF) sputtering onto a precleaned glass substrate through a shadow mask to form the active layer at room temperature. During the sputtering, the RF power and chamber pressure were 100 W and 9 mTorr, while the Ar flow rate was maintained at 30 sccm. The annealing process was then performed at 400 °C in a nitrogen furnace for 90 min. A 4000 Å cross-linkable poly(4-vinyl phenol) (PVP) was spin-coated on the a-IGZO surface and then cross-linked at 200 °C for 60 min in air to serve as the gate insulator. The capacitance and the relative dielectric constant of PVP are 13.2 nF cm^{-2} and 3.5, respectively. Poly(melamine-*co*-formaldehyde) (methylated, Aldrich, $M_w \approx 511$) was utilized as a crosslinking agent for PVP. The surface of PVP was made hydrophilic by short-time exposure to a 50 W O_2 plasma before submerging the substrate into 2000 Å, positively charged polystyrene spheres (Merck, K6–020) diluted in an ethanol solution at 0.2 or 0.8 wt%. The SEM images of the PVP with 0.2 or 0.8 wt% PS sphere concentrations are shown in Figure 2b,c, respectively. By counting the PS spheres in the SEM images in Figure 2b,c, the concentration of dots per area is estimated to be 6.8×10^6 mm^{-2} for 0.8 wt% PS spheres and 4.8×10^6 mm^{-2} for 0.2 wt% PS spheres, respectively.

The polystyrene spheres were adsorbed on the PVP surface to serve as the shadow mask. After submerging the substrate for 3 min in a polystyrene sphere solution, the substrate was then transferred into a beaker with boiling isopropyl alcohol solution for 10 s. The substrate was immediately blown dry to form 2D columnar arrays. A 1000 Å Al was evaporated as a metal gate electrode. After removing the polystyrene spheres

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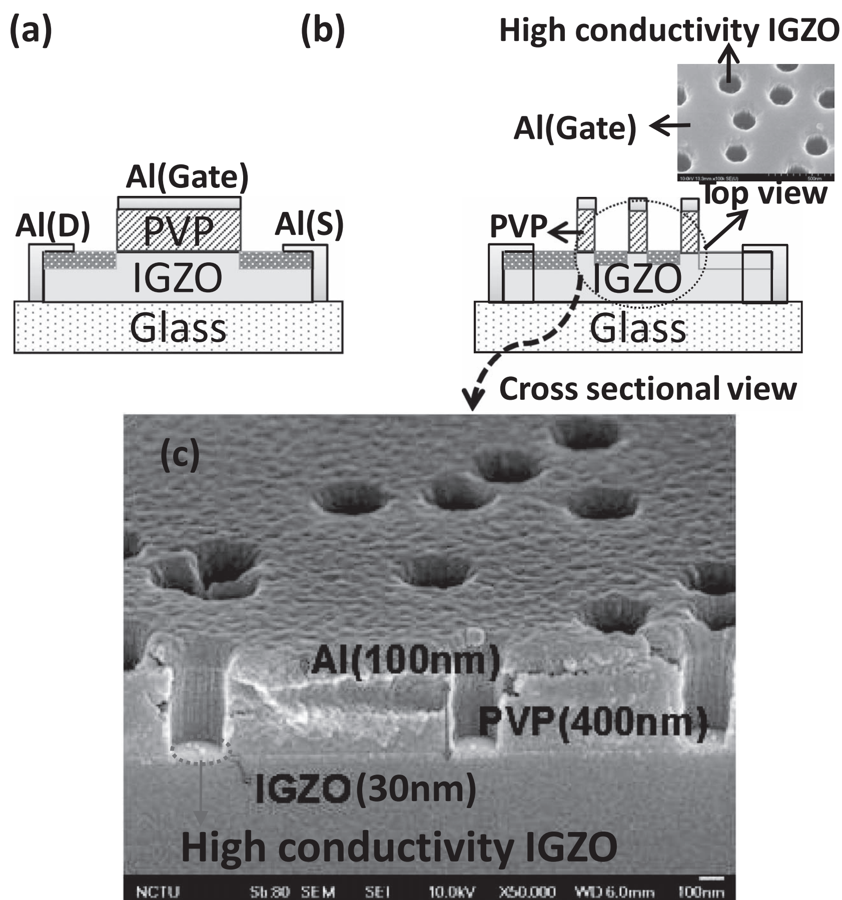

Figure 1. The schematic device structures of a) STD (standard) and b) TG-NDD a-IGZO TFTs. c) The SEM image of the cross-sectional view of the TG-NDD a-IGZO TFTs.

using an adhesive tape (Scotch, 3M), the PVP at sites without Al coverage was removed after 8 min of 150 W O_2 plasma treatment. The source/drain region and the bare channel region (without PVP coverage) was then treated with Ar plasma to increase the conductivity. Finally, a 100-nm-thick layer of Al used as a source/drain metal was evaporated at room temperature through a shadow mask. The Ar plasma treatment on the source/drain regions of the a-IGZO active layer lowered the series resistance between the source/drain metal pads and the induced channel under the gate region. After Ar treatment, a self-aligned structure was formed. The channel width is defined by the edge of the a-IGZO pattern. For top-gate device (TG-STD and TG-NDD), the channel length is defined by the edge of the gate electrode. Due to the confinement of the a-IGZO pattern, there is no current spreading outside the channel region. The channel width and length of the top gate devices are listed in **Table 1**. For TG-STD, the process flow is similar to that depicted in Figure 2(a) except that the PS sphere absorption process is removed.

Figure 3a shows the resistivity of the a-IGZO thin film as a function of the Ar plasma exposure time. The resistivity of a-IGZO film is drastically reduced from $>10^5$ Ω cm to 3.85 Ω cm during the Ar plasma treatment. Also, from the result of O 1s X-ray photoelectron spectroscopy (XPS) spectra for a-IGZO thin film (not shown), the relative concentrations of oxygen vacancies (*Vö*, peak centered at ≈531.4 eV) in IGZO films is increased from 20.18% to 24.67% after the Ar plasma treatment. (the relative concentrations of oxygen vacancies in IGZO films is calculated by the area integration of O 1s (*Vö*) peak to the area integration of each O 1s peak).[10] In previous reports, it has been found that the Ar-plasma-treated surface exhibits higher In concentration, lower Ga concentration, and lower Zn concentration than does the untreated sample.[11] The In-rich surface contributes to the formation of a region with high electron concentration because the weak bonds between the In ions and oxygen are more likely to generate carriers than the Ga–O bonds or Zn–O bonds.[12] The variation in the cation composition (In, Ga, and Zn), however, was not the only reason for the dramatic decrease in the resistivity after Ar plasma treatment. The increase in oxygen deficiency after the Ar ion bombardment was a critical factor in causing the drastic resistivity change.[11]

The transfer characteristics of TG-STD devices with different Ar plasma treatment durations are compared in Figure 3b. In Figure 3b, device channel width is 3000 μm and the channel length is 1000 μm. In this top-gate device, the Ar plasma treatment produces the source and drain regions with high electron concentration. Without the Ar plasma treatment, the offset regions between the gate-induced-channel and the source/drain electrodes are highly resistive. As a result, no turn-on characteristics can be observed. After a suitable Ar plasma treatment (for example, the 3 min treatment depicted in Figure 3b), the conductivity in the offset regions becomes high enough to serve as the source and drain regions. The transistor exhibits normal transfer characteristics. When the Ar plasma treatment time increases to 5 min, the leakage current increases because the sidewall of the PVP layer is damaged by the Ar ions. When the Ar plasma treatment time increases to 10 min, the thin IGZO film is damaged due to the etching effect caused by the Ar ion bombardment. No turn-on characteristics can be observed.

The transfer characteristics of TG-NDD (PS 0.8 wt%) device with different Ar plasma treatment durations are shown in Figure 3c. Device channel width is 3000 μm and the channel length is 1000 μm. In addition to forming the conductive source and drain regions, Ar plasma treatment in TG-NDD devices also produces a nanometer-scale dot-like doping in IGZO front channel surfaces. When the Ar plasma time is 3 min, the device exhibits superior transfer characteristics. The on current is higher than 0.1 mA, the off current remains lower than 1 nA, the effective field-effect mobility is 79 $cm^2 V^{-1} s^{-1}$, the subthreshold swing is 1.2 V $decade^{-1}$, and the threshold voltage is –2.94 V. When the Ar plasma time increases to 5 min, both the

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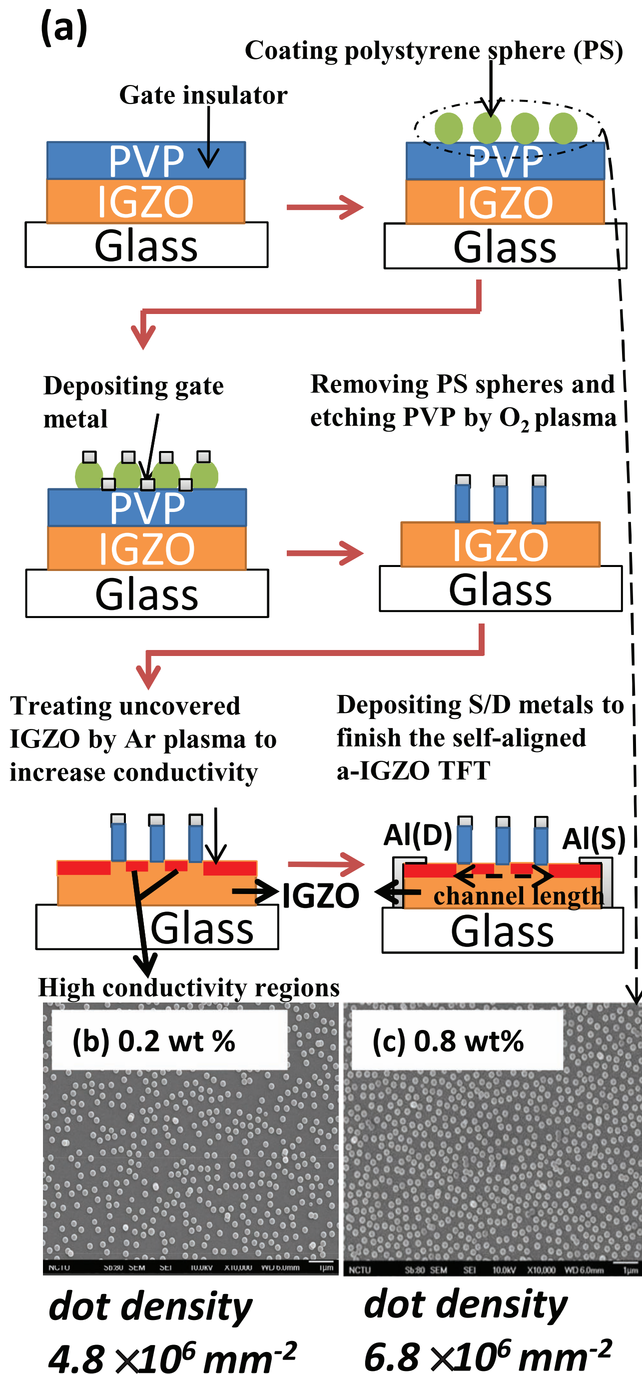

Figure 2. a) The processes flow of the TG-NDD (top-gate with nano-dot doping) a-IGZO TFT. The SEM images of the PVP substrate adsorbed with b) 0.2 wt% and c) 0.8 wt% polystyrene spheres. The diameter of the spheres is 200 nm.

source to drain leakage current and the gate leakage current are raised. Figure 3d shows the output characteristics (drain current (I_D) as a function of drain voltage (V_D)) of TG-NDD (PS 0.8 wt%) a-IGZO TFT with channel width and length of 3000 μm and 1000 μm, respectively. The transistor operates in the enhancement mode. I_D increases linearly with increasing V_D at low V_D, and saturates at higher V_D.

The influences of the nanodot concentration on the device performance are studied by fabricating TG-NDD devices with different PS sphere densities. The SEM images of the low-density PS sphere mask (PS 0.2 wt%) and the high-density PS sphere mask (PS 0.8 wt%) are shown in Figure 2b,c, respectively. The transfer characteristics and the root square of the drain current plotted as a function of gate bias of TG-STD, TG-NDD (PS 0.2 wt%), and TG-NDD (PS 0.8 wt%) are compared in **Figure 4** when channel width and length are 3000 μm and 1000 μm, respectively. In Table 1, we listed the threshold voltage, the maximum field-effect mobility, the average mobility, the standard deviation of the mobility, the subthreshold swing, and the on/off current ratio for the TG-STD and TG-NDD devices with different W/L (width/length) ratios (3, 3.3, and 10). The TG-STD devices, the TG-NDD with high density dots (produced with 0.8 wt% polystyrene spheres), and the TG-NDD with low density dots (produced with 0.2 wt% polystyrene spheres) are compared. The TG-NDD structure obviously increases the field-effect mobility when we increase the concentration of the doping dots. High effective field-effect mobility (71.7 to 87.4 cm^2 V^{-1} s^{-1}) can be obtained for TG-NDD with high density dots and with a W/L ratio ranged from 3 to 10. The reproducibility is represented by the standard deviation of the mobility as listed in Table 1. To improve the reproducibility and the uniformity, an ordered dot-like structure is required. Nanoimprinting may be utilized to produce an ordered nanoscale dot-like structure in future works. The improvement of mobility by NDD is observed for devices with various channel widths and lengths. Also, changing the W/L ratio does not significantly influence the mobility. The reported mobility overestimation due to the current spreading is not observed.[13] In our work, the channel width is defined by the IGZO pattern, not by the source/drain electrodes. A well-confined active region avoids current spreading outside the channel region. When most reported field-effect mobilities of a-IGZO TFTs are lower than 35 cm^2 V^{-1} s^{-1},[4–6] three previous studies have reported high mobility a-IGZO TFTs. The typical parameters of the high mobility a-IGZO TFTs in these previous reports are also listed in Table 1. Kim et al. proposed that the metal-oxide TFT with ITO/IGZO double active layer exhibits a high mobility of 104 cm^2 V^{-1} s^{-1}.[14] Lee et al. utilized a multilayer gate insulator to realize an effective field-effect mobility of 100 cm^2 V^{-1} s^{-1}.[3] In these reports, the photolithography process is required to realize a channel length smaller than 20 μm. Chiu et al. proposed a lithography-free long-channel a-IGZO TFT with a high-k (where k is the dielectric constant) gate dielectric to realize a high mobility of 62 cm^2 V^{-1} s^{-1}.[15] In our work, an effective mobility of 79 cm^2 V^{-1} s^{-1} can be achieved using nanodot doping with a 1000 μm channel length and a conventional silicon nitride gate dielectric. It is expected that the effective field-effect mobility could be further increased if a high-k dielectric is used with the NDD structure.

The drastically enhanced mobility in NDD structures may be for two reasons. First, the effective channel length is reduced due to the conductive dot regions inside the channel. The effective channel length for TG-NDD devices can be estimated by calculating the dot concentration. For TG-NDD devices with high-density dots (with 0.8 wt% PS spheres), the effective channel length is reduced from 1000 μm to 500 μm.

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Table 1. Comparisons of typical parameters in TG-STD and TG-NDD a-IGZO TFTs.

	W/L [μm/μm]	*W/L* ratio	V_{th} [V]	μ_{max}[a] (μ_{avg}[b]) [$cm^2 V^{-1} s^{-1}$]	σ[c] [$cm^2 V^{-1} s^{-1}$]	*S.S.* (V dec^{-1})	On/Off
TG-STD	1000/100	10	−3.1	5.53 (4.87)	0.304	0.97	1.7×10^5
	1000/300	3.33	−3.1	5.54 (5.3)	0.13	0.39	2.8×10^6
	3000/1000	3	0.5	4 (3.38)	0.24	0.67	1.6×10^6
TG-NDD (0.8 wt%)	1000/100	10	−2.29	87.4 (N/A)	N/A	0.49	1.06×10^6
	1000/300	3.33	−2.47	71.7 (N/A)	N/A	0.34	1.81×10^5
	3000/1000	3	−2.94	79.2 (67.5)	6.1	0.92	9.42×10^6
TG-NDD (0.2 wt%)	1000/100	10	5.91	45.6 (N/A)	N/A	0.29	3.5×10^6
	1000/300	3.33	4.5	47.5 (43.7)	4.16	0.72	5.6×10^6

[a] μ_{max} is the maximum effective field-effect mobility; [b] μ_{avg} and; [c] σ are average effective mobility and standard deviation calculated from five independent devices.

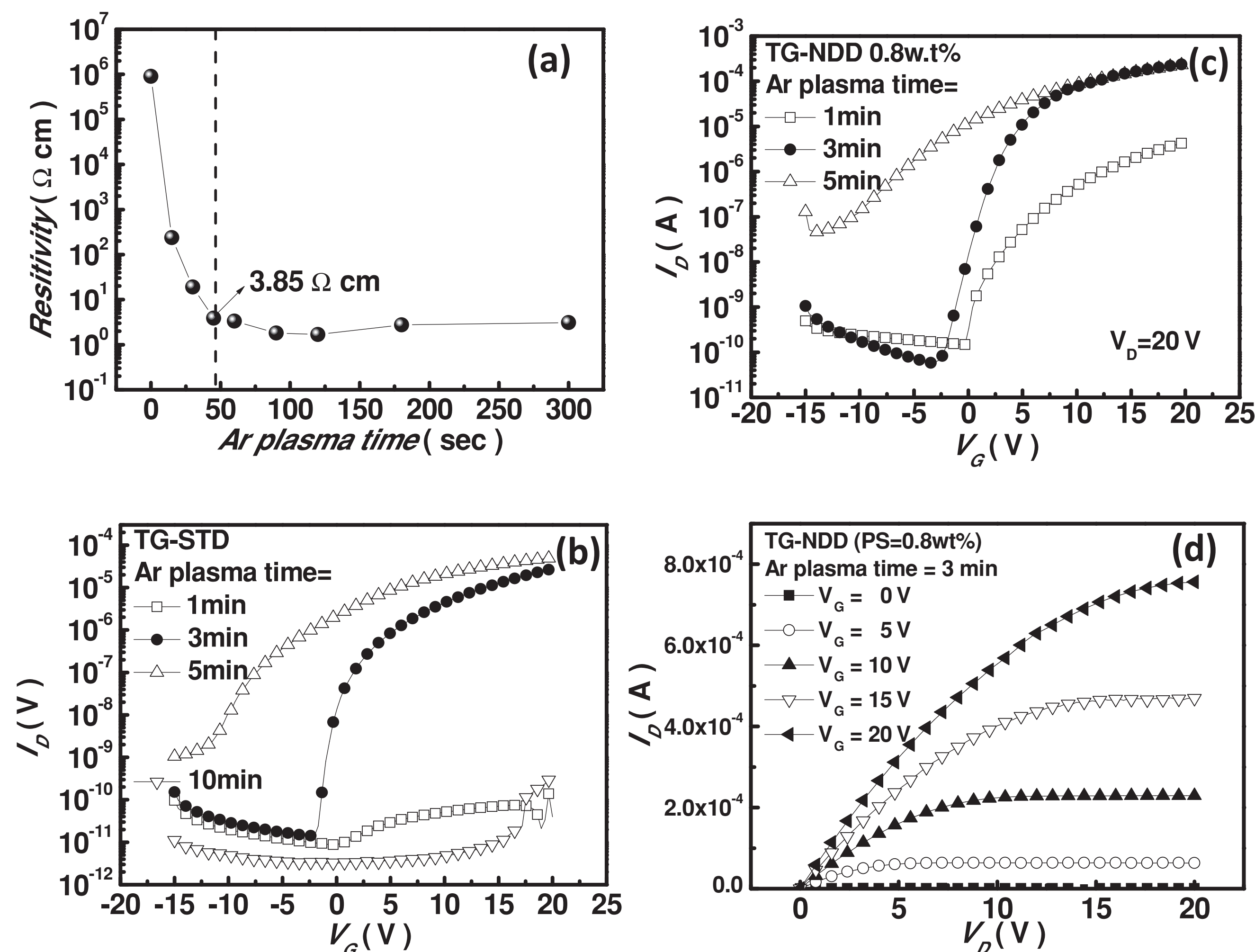

Figure 3. a) Resistivity of the a-IGZO thin film as a function of the Ar plasma exposure time. b) The transfer characteristics of TG-STD devices with different Ar plasma treatment times on source/drain electrodes. c) The transfer characteristics of TG-NDD devices with high density dots (0.8 wt% PS spheres) with different Ar plasma treatment time. d) The output characteristics of TG-NDD devices (PS spheres: 0.8 wt%) with the optimal Ar plasma treatment time (3 mins). In Figure 3b–d, the device channel width was 3000 μm and the channel length was 1000 μm.

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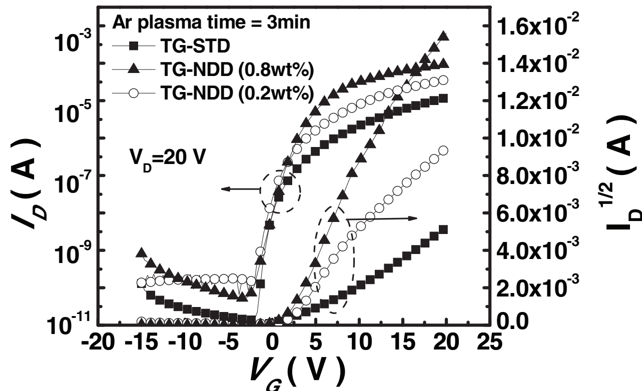

Figure 4. The transfer characteristics and the root square of the drain current plotted as a function of gate bias for three devices: TG-STD, TG-NDD (PS 0.2 wt%), and TG-NDD (PS 0.8 wt%). The device channel width is 3000 μm and the channel length is 1000 μm.

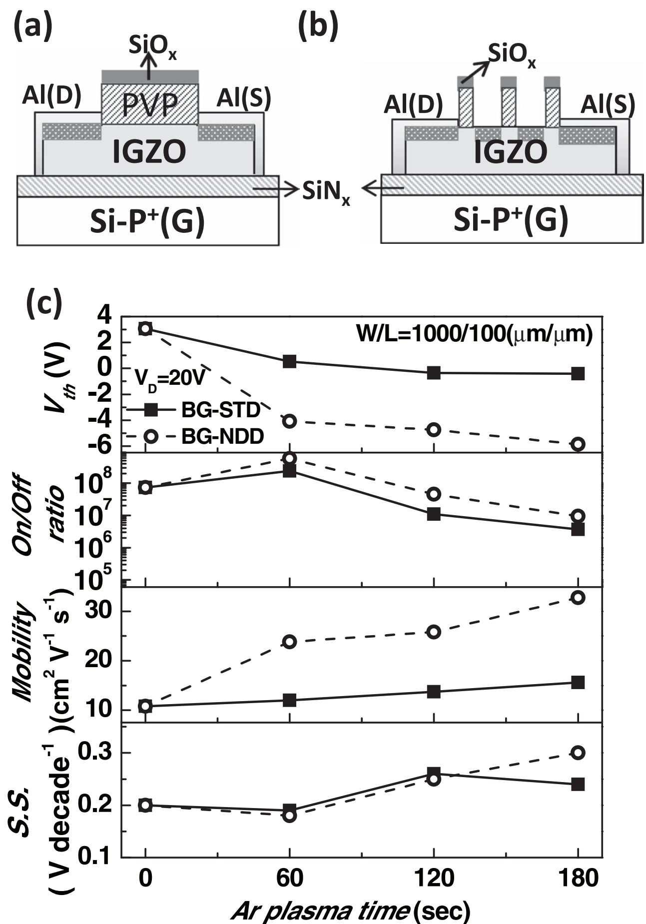

Figure 5. The schematic device structures of a) STD and b) NDD-BG a-IGZO TFTs. c) Four typical parameters (threshold voltage, on/off ratio, mobility, and subthreshold swing) of BG-STD and BG-NDD devices are extracted and plotted as a function of Ar plasma treatment time. Each data point was extracted from the transfer characteristics measured at V_D = 20 V. The device channel width is 1000 μm and the channel length is 100 μm.

For TG-NDD devices with low-density dots (with 0.2 wt% PS spheres), the effective channel length is reduced from 1000 μm to 684 μm. If the effective intrinsic channel length is used to estimate the mobility inside the intrinsic a-IGZO region, the intrinsic mobility is 39.6 cm^2 V^{-1} s^{-1} for TG-NDD devices with high-density dots and is 32.5 cm^2 V^{-1} s^{-1} for TG-NDD devices with low-density dots. The mobility for TG-STD devices is only around 3.8 cm^2 V^{-1} s^{-1}, which is 8–10 times smaller than the mobility in the intrinsic channel region for TG-NDD devices. The reduction of the effective channel length is not sufficient to explain the enhanced mobility in TG-NDD devices.

The second reason to explain the enhanced mobility in the intrinsic channel region for TG-NDD devices is the field-induced barrier lowering effect. It is known that the electron transport in a-IGZO is governed by the percolation transport.[16,17] The random distribution of Ga^{3+} and Zn^{2+} ions in the network structure forms potential barriers around the conduction band and then reduces electron mobility.[18] The potential barrier can be significantly reduced when carrier concentration is increased.[16–18] When high-density conductive dot-like regions are introduced into the intrinsic a-IGZO film, the potential barrier in the intrinsic a-IGZO is lowered by the neighboring high conductive regions. Increasing the dot concentration leads to a more pronounced barrier lowering effect. As a result, when dot density increases from 4.8×10^6 mm^{-2} to 6.8×10^6 mm^{-2}, the mobility in the intrinsic channel increases from 32.5 cm^2 V^{-1} s^{-1} to 39.6 cm^2 V^{-1} s^{-1}.

The barrier lowering effect is well observed in many semiconductor devices. For example, the Schottky barrier at the metal–organic interface exhibits a Schottky barrier lowering effect when increasing the doping level of the organic semiconductor.[19] For short-channel MOSFETs, the built-in potential barrier between the heavily doped source and the bulk suffers from the drain-induced barrier-lowering effect.[20–22] For poly-Si TFTs, the grain boundary barrier is also lowered by the drain-to-source electric field.[23] Drain-induced barrier lowering effect is also observed in short channel ZnO TFT.[24] The high density dot-like doping in channel region of field-effect transistors was not reported in previous studies. However, in our work, it is believed that the effective potential barrier in the intrinsic a-IGZO surrounded by heavily-doped dots is lowered when the dot density is increased and when the doping level is increased. Since the electron mobility in a-IGZO is exponentially dependent on the negative of the potential barrier height,[16,17] the reduction of potential barrier leads to a significant improvement of the electron mobility.

Finally, the NDD process is utilized on the back interface of conventional bottom-gate (BG) a-IGZO TFTs. The bottom-gate (BG) a-IGZO TFTs with and without NDD are denoted as BG-NDD and BG-STD, respectively. The schematic diagrams of BG-STD and BG-NDD a-IGZO TFTs are shown in **Figure 5**a,b, respectively. For bottom-gate devices, process flow is similar to that shown in Figure 2a, with two exceptions. The first difference is that the glass substrate is replaced by a heavily doped silicon substrate capped with a 100 nm silicon nitride. The second is that the top aluminum electrode above the PVP layer is replaced by a thermally evaporated SiO_x (silicon oxide) with a thickness of 40 nm. The SiO_x is served as a mask and the

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PVP without the SiO_x coverage is etched by oxygen plasma. The channel width and length of the bottom gate devices are 1000 μm and 100 μm, respectively. The channel width is defined by the edge of the a-IGZO pattern. For bottom-gate devices (BG-STD and BG-NDD), the channel length is defined by the edge of the source/drain electrodes. Four typical parameters, including threshold voltage (V_{th}), on/off ratio, field-effect mobility (μ), and subthreshold swing (*S.S.*), are extracted and plotted as a function of Ar plasma treatment time, as shown in Figure 5c.

For BG-STD devices, when the Ar plasma time increases from 0 s to 180 s, the field-effect mobility slightly increases from 10.76 to 15.6 $cm^2 V^{-1} s^{-1}$ and the threshold voltage decreases from 3.7 to –0.42 V. The subthreshold swing and the on/off current ratio are almost unchanged. The decrease in the threshold voltage and the increase of the field-effect mobility after Ar plasma treatment was also reported by Park et al. and was explained by the improvement of the contact resistance between the source/drain electrodes and a-IGZO semiconductor.[11]

For BG-NDD devices, when the Ar plasma time increases from 0 s to 180 s, the field-effect mobility significantly increases from 10.8 to 32.7 $cm^2 V^{-1} s^{-1}$. The threshold voltage decreases from 3.1 to –5.9 V. The NDD structure influences the electric field distribution in the front channel because the a-IGZO film is only 30 nm thick. As a result, the field-effect mobility is enlarged by NDD treatment due to the reduced effective channel length together with the barrier-lowering effect. The shift of the threshold voltage is not clearly understood. In our previous report, the removal or the injection of electrons into body region causes a positively shifted or a negatively shifted threshold voltage, respectively.[25] When electron concentration in body region is increased, a more negative gate bias is required to deplete the channel. In this work, the dot doping creates localized high electron concentration regions. The 3D potential distribution in channel region is still not clearly investigated. However, the negatively shift of threshold voltage is consistent with the phenomenon reported in our previous work when electrons are injected into back channel by capping calcium/aluminum layer onto the back interface of a bottom-gate a-IGZO TFT.[25]

To summarize, this study proposes a top-gate self-aligned a-IGZO TFT with nanometer-scale dotted channel doping. With a simple, low-cost, and lithography-free process, the effective mobility level of TG a-IGZO TFT becomes 19 times higher than that of the control sample and the maximum effective mobility reaches 79 $cm^2 V^{-1} s^{-1}$. If an effective intrinsic channel length is used to estimate the mobility inside the intrinsic a-IGZO region, the maximum intrinsic mobility of TG-NDD a-IGZO TFT reaches 39.6 $cm^2 V^{-1} s^{-1}$ and is 10 times larger than that of the control (STD). The nanodot doping (NDD) structure reduces the effective channel length and lowers the potential barrier in the intrinsic a-IGZO by the neighboring high conductive regions. Increasing the dot concentration leads to a more pronounced barrier lowering effect. According to the percolation conduction model, the decrease of the potential barrier leads to a significant increase of the field-effect mobility in a-IGZO semiconductor. The high mobility and the self-aligned structure of the proposed a-IGZO TFTs with NDD are promising for the development of low cost circuit-like RFID tags, smart cards, and transparent circuits on windows.

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