Transient Improvement by Window Transient Enhancement and Overshoot Suppression Techniques in Current Mode Boost Converter

Yean-Kuo Luo, Chao-Chang Chiou, Chun-Hsien Wu, Ke-Horng Chen, *Senior Member, IEEE*, and Wei-Chou Hsu

***Abstract*—In this paper, a current mode boost converter using window transient enhancement (WTE) and overshoot suppression (OSS) technique is presented for digital still camera (DSC) applications. The peak-to-peak transient overshoot voltage demand of a DSC motor driver is generally within 4%–5% of the regulated value. However, conventional boost converters usually fail to pass this criterion during large load transient. The OSS technique reduces the overshoot voltage when load current changes from heavy to very light. Experimental results show that compared with the use of a conventional current mode boost converter, the use of the technique reduces drop voltage about 62% and overshoot voltage about 51% when the load current has a load step of 400 mA. Moreover, the settling time improves to 43%, which is better than in the conventional case of a 400 mA load current step. The overhead of the silicon area is about 4.5% to achieve the overshoot reduction. The estimated high performance demonstrates that it is suitable for DSC applications.**

***Index Terms*—Boost converter, constant frequency regulation, dc-dc power converter, free-wheeling switching, on-chip compensation, OSS technique, overshoot suppression.**

I. Introduction

OVER the past few years, portable electronic devices, such as digital still cameras (DSC), have become very popular. Today, cameras come in smaller sizes but boast of more powerful features that require highly integrated power solutions. Generally, the power supply of a DSC is divided into several parts, which include the motor driver, system logic and input/output (I/O), double-data-rate-two synchronous dynamic random access memory (DDR2 SDRAM), central processing unit, charge-coupled device, CMOS sensor, and backlight unit [1]. Each part has its own specifications under specified application conditions. Here, a boost converter is designed to supply an output of 4.5–5 V to a motor driver, with a loading range between 0 and 300 mA, or 400 mA. Aside from the static specification demands, dynamic transient performance, such as peak-to-peak overshoot is also important. The reason is that a motor driver is commonly used to drive the zoom lens or audio frequency shutter. The supply voltage of the motor driver can affect the driving speed of the zoom lens. Therefore, an overshoot in the supply voltage may lead to inaccurate lens movement or focus error.

Generally, a peak-to-peak overshoot at a specified loading transient should be within 4%–5% in order to not affect system performance. The right half-plane zero decrease the system bandwidth when approaching low frequencies; it even causes instability issues at heavy loads and low-battery conditions [2]. Thus, a conventional boost converter with a limited bandwidth limited by the RHP zero usually suffers from a large transient overshoot. Many control techniques have been presented to improve transient performance in the design of buck converters [3]–[16]. External components or slave transient enhancement systems are used to improve transient performance. However, these require more off-chip components or printed-circuit board space and are more costly [5]–[7]. Some methods require special conditions to maintain effective operation. For example, the V^2 control is used for fast transient but needs a large time constant composed of a large output capacitor and equivalent series resistance (ESR). As a result, it suffers from a larger output voltage ripple, deteriorating the system performance [8]–[10]. A low-ESR ceramic capacitor is commonly used because of its low cost. However, it is not suitable for such design.

Other control methods used to improve transient performance may not be suitable to reduce overshoot in the design of boost converters [11]–[13]. For example, some control methods discharge redundant energy by turning ON the low-side power MOSFET. The control mechanisms used in boost converters may also lead to a bad overshoot, when load current changes from heavy to light [13]. The dynamic frequency control or slew rate enhancement in error amplifiers may solve the drop during current change from light load to heavy load. Unfortunately, these methods are not very effective in overshoot reduction when the load current changes from heavy to light load or very light load [11], [12]. In this paper, the proposed converter with the window transient enhancement (WTE) and overshoot suppression (OSS) techniques can efficiently reduce the overshoot problem at the cost of about 4.5% extra increase of silicon area.

Section II describes the WTE and the OSS techniques to improve transient response and reduce the overshoot problem.

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Y.-K. Luo and W.-C. Hsu are with the Institute of Microelectronics, National Cheng Kung University, Tainan 701, Taiwan.

C.-C. Chiou, C.-H. Wu, and K.-H. Chen are with the Institute of Electrical Control Engineering, National Chiao Tung University, Hsinchu 300, Taiwan (e-mail: khchen@cn.nctu.edu.tw).

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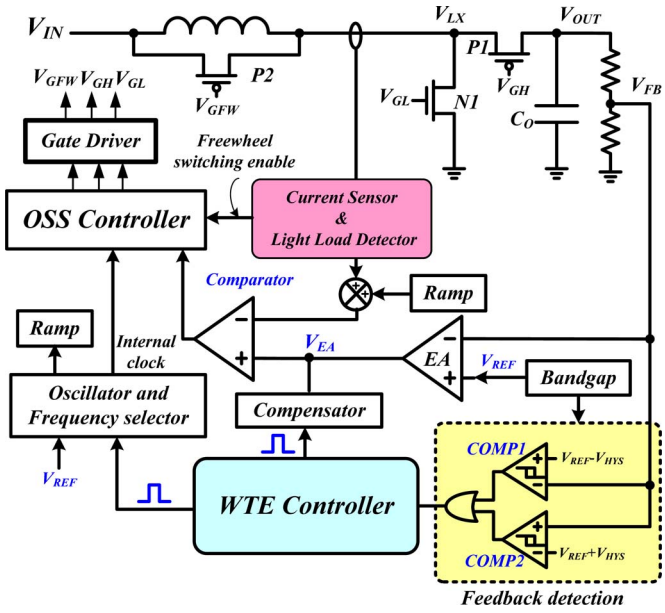


Fig. 1. Proposed current mode boost converter.

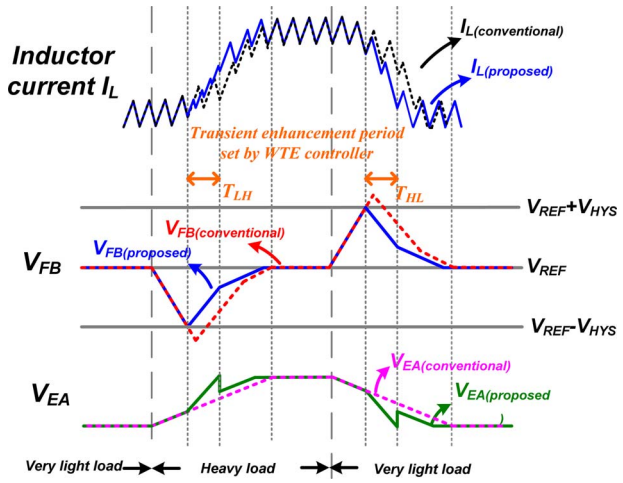


Fig. 2. Waveforms with and without the WTE technique.

The description of the WTE technique is illustrated in Section III. The proposed OSS technique is illustrated in Section IV. The experimental results are presented in Section V. Finally, conclusions are given in Section VI.

II. Proposed WTE and OSS Control Techniques

A conventional boost converter usually operates in discontinuous conduction mode (DCM) at light loads. In case of a sudden large load current, a large dip in output voltage appears due to the limited bandwidth and poor recovery ability of the DCM operation. However, the extra energy induces a large overshoot voltage at the output once the load current changes from heavy to light. Unfortunately, large transient voltage variations will cause a malfunction in the next stage. The suppression of the transient output variation becomes more important.

To improve transient response in conventional boost converters, this paper introduces the OSS technique and the WTE technique, which is depicted in Fig. 1 [14]. The function schematic includes three main parts, namely, the original pulsewidth modulation controller with a feedback network, the WTE controller, Oscillator and frequency selector, and the light-load detection used to start the OSS control mechanism.

A large variation in the output voltage caused by light-to-heavy or heavy-to-light load current transient can be detected by the feedback detection circuit. The hysteretic comparator *COMP1* with a positive input reference of ($V_{\rm REF}$-$V_{\rm HYS}$) for detecting sudden heavy load conditions, sets its output to high to turn ON the WTE controller. The controller then temporarily changes the compensator at the output, $V_{\rm EA}$, of the error amplifier to speed up the charge accumulation so that the inductor current increases rapidly to supply the heavy load. Moreover, the switching frequency is increased during the period $T_{\rm LH}$ when a drop condition is detected by the comparator, *COMP1,* at the feedback node. The increase of switching frequency avoids system instability when the compensator is changed and the new cross-over frequency comes too close to one-tenth of the original switching frequency. The WTE controller is turned OFF beyond the period $T_{\rm LH}$. Besides, the temporarily higher switching frequency is stopped and the compensator returns back to its original value for stable operation. Similarly, the heavy-to-light load current transient induces an overshoot voltage, which is detected by the hysteretic comparator *COMP2*, to turn ON the WTE controller. The controller then temporarily changes the equivalent compensator network to speed up the decrease in the ramp process of the EA output $V_{\rm EA}$. As a result, it decreases the inductor current faster or even stops the switching. The value of $V_{\rm HYS}$ is set to 2% of the $V_{\rm REF}$, and thus, the feedback detection voltage is in the range of $0.98 * V_{\rm REF}$–$1.02 * V_{\rm REF}$. The $V_{\rm HYS}$ voltage is set to 1% or less to obtain a better transient performance. However, a very small $V_{\rm HYS}$ value, when it is smaller than the output ripple or the switching noise observed at the output, leads to malfunction.

The operation of the WTE technique is presented in Fig. 2. The red dotted line denotes the feedback voltage, $V_{\rm FB}$, in a conventional boost converter. The correspondent $V_{\rm EA}$, represented by the pink dotted line, illustrates the slow transient response due to a limited system bandwidth. The blue solid line represents the behavior of the proposed WTE technique. Fast transient response is achieved because of the fast response of the correspondent $V_{\rm EA}$, which is represented by the green solid line. The inductor current waveform with and without WTE technique is represented in solid and dotted line, respectively. During the periods $T_{\rm LH}$ and $T_{\rm LH}$, the compensator is changed by the WTE technique in the proposed converter to achieve fast transient response.

Although the WTE technique is applied to improve transient performance, overshoot problems are not solved completely using only this technique. The reason is that the WTE technique is triggered when the feedback voltage exceeds $V_{\rm REF} + V_{\rm HYS}$, where an overshoot condition has already occurred. Thus, although the WTE technique prevents the inductor current from rising too quickly, it cannot discharge the excess voltage that

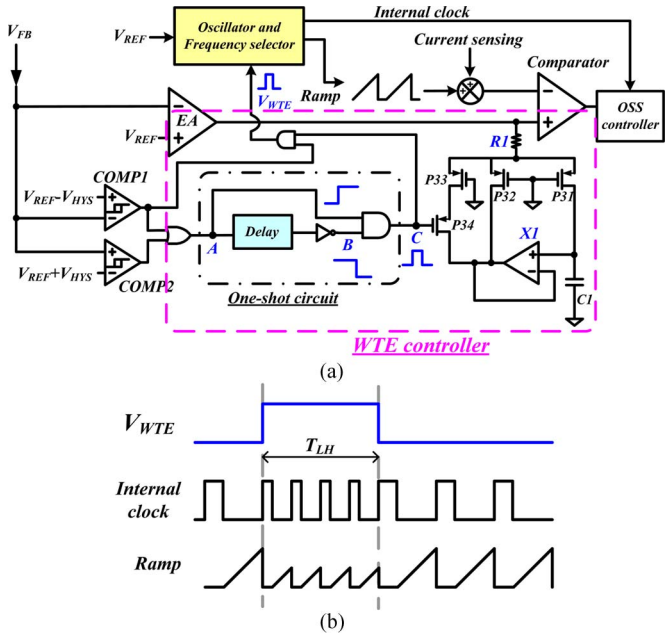


Fig. 3. (a) Proposed current mode boost converter with WTE technique. (b) Operation of Oscillator and frequency selector during light-to-heavy load transient period T_{LH}.

has already appeared at the output. Thus, a long recovery time is needed for the output to return to its steady state. Usually, a dummy load is used to reduce the settling time. Although a dummy load is applied to discharge energy, it inevitably causes loss in efficiency when an inappropriate dummy load is selected. Hence, the OSS technique is applied to replace the dummy load mechanism.

III. Implementation of the Proposed WTE Technique

The operation of the WTE technique is shown in Fig. 3(a). Generally, the transistor *P34* is turned ON in a steady state unless a large load transient is detected by the feedback detection circuit. When this scenario occurs, an off-time pulse, which is generated by logic operation, turns OFF the transistor *P34* for a few microseconds. Off-time pulse at the *C* node is the output of the one-shot circuit. This off-time pulse temporarily modifies the capacitance multiplication ratio to two times smaller than the original six times the value of the on-chip capacitance *C1* [3], [4], [15], [16]. In other words, the effective small capacitance results in a faster slew rate. The system bandwidth is also extended temporarily. Thus, transient performance is improved by the proposed mechanism. Fig. 3(b) shows that the oscillator speeds up the switching frequency clock only during the light-to-heavy load transient period T_{LH}.

The proposed circuit of the WTE technique is shown in Fig. 4(a). The off-time pulse generation circuit is not shown for simplification. The *EA* implemented by a simple structure is composed of transistors *P21–P25* and *N21–N24*. As previously mentioned, transistors, *P11–P17* and *N11–N17*, function as a rail-to-rail unity gain buffer *X1*. The rail-to-rail unity gain buffer responds from the ground to a maximum positive voltage without problems in dc-biasing operation. Transistors *P31–P34*

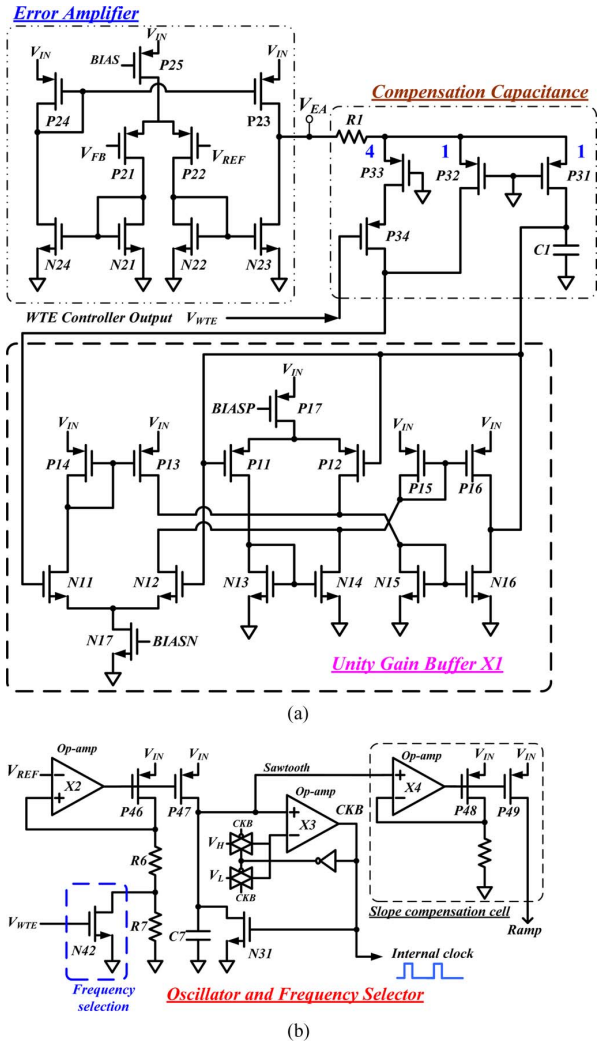


Fig. 4. (a) Transistor level of the WTE technique. (b) Oscillator and frequency selector for improving transient response in the WTE controller.

and the unity gain buffer *X1* function as capacitance multiplication. The capacitance multiplication ratio is decided by the ratio of the transistor size of *P31* to the summation size of transistors *P32* and *P33*. In this work, the size ratio of transistors *P31-P33* is 1:1:4. According to the theory published in [3], [4], [16], effective capacitance can be boosted to six times the *C1* capacitance. The gates of transistors *P31–P33* are connected to the ground, and the drain-source voltages are tracked by the unity gain buffer *X1*. Transistors *P31–P33* have the same dimensions and a well-matching layout to ensure their equivalent threshold voltages.

Fig. 4(b) illustrates the internal oscillator and the frequency selector. When the WTE controller output, V_{WTE}, is pulled high temporarily, the internal clock is increased to a higher value to cause a larger charge/discharge current on capacitance *C7* when the transistor *N42* is turned ON. The signals V_H and V_L define the boundary voltage of the sawtooth, which is generated from the reference voltage V_{REF}. The operational amplifiers *X2–X4* can be implemented by the single-stage architecture.

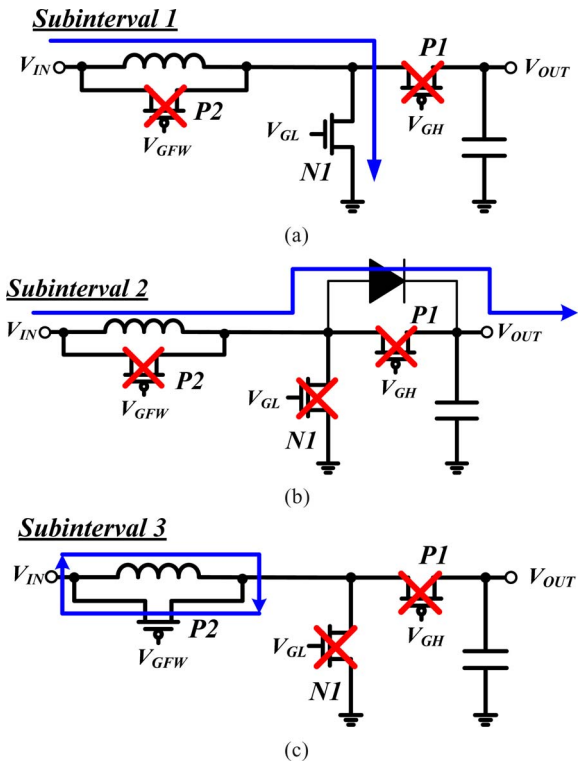


Fig. 5. Operation of the proposed OSS technique of a boost converter.

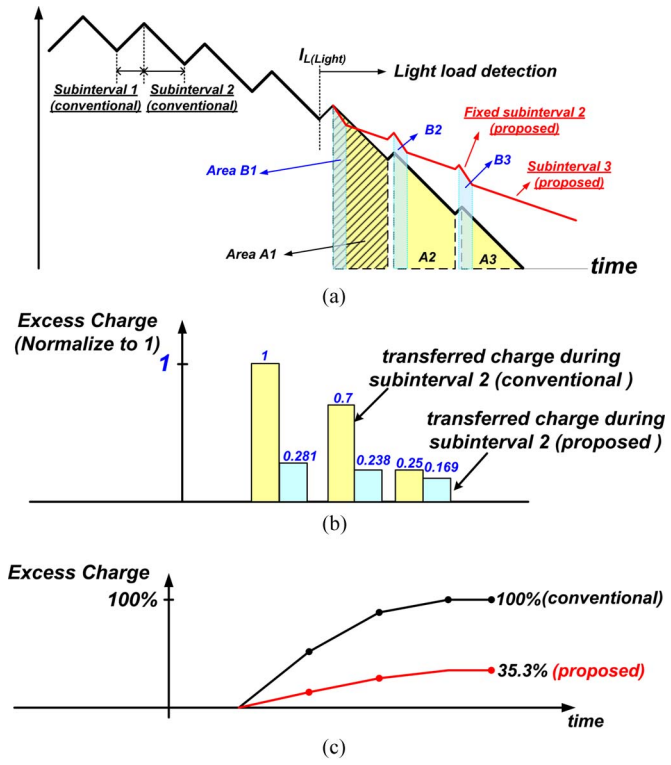


Fig. 6. (a) Waveforms with and without OSS technique. (b) Normalization of excess charge with and without OSS technique.(c) Chart of total excess charge.

IV. Operation of the Proposed OSS Technique

The OSS technique is turned ON when the inductor current is lower than the $I_{L\,(\mathrm{Light})}$. The cost is lower efficiency performance when converter operates at the light condition. At heavy load condition, the inductor is higher than $I_{L\,(\mathrm{Light})}$ and the converter operates in the continuous conduction mode (CCM) mode, as same as the conventional boost converter. When converter operates in CCM mode, the transistor *P2* is always turned OFF and transistor *P1* is turned ON after transistor *N1* is turned OFF every cycle.

Once the OSS technique is turned ON and the operation of OSS technique is shown in Fig. 5. During *subinterval 1*, The term "subinterval" has been left italicized at the first instance, and changed to Roman at other instances in the text per style guide. Kindly check if it is OK. as shown in Fig. 5(a), the power NMOSFET *N1* is on and ramps up the inductor current, whereas transistors *P1* and *P2* are OFF. This operation of subinterval 1 is the same as that of a conventional boost converter.

In subinterval 2, as shown in Fig. 5(b), all the power transistors are turned OFF, whereas transistor *P1* is turned OFF, and the inductor current passes through the body diode of transistor *P1* to charge the output capacitor. The period of subinterval 2 is fixed, which is different in comparison with that of the pseudocontinuous conduction mode control [15]. The maximum period of subinterval 2 is 20%–25% of the duty cycle in this work.

As shown in Fig. 5(c), the free-wheel transistor *P2* turns ON and shorts the inductor to dissipate the extra energy in subinterval 3. When transistor *P2* is turned ON, the inductor current

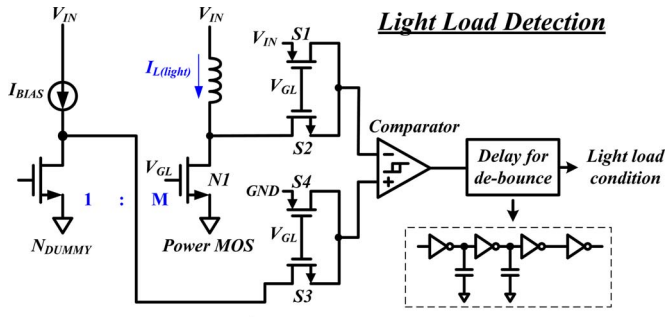


Fig. 7. Light load detection.

flows through transistor *P2* and returns to the inductor circular. Through this method, the redundant energy is consumed by the finite resistance of transistor *P2*. The inductor avoids the energy to be transmitted to the output at the same time.

The concept of OSS technique is explained in two parts. First, it blocks the inductor current from transferring to the converter output. This is achieved using the free-wheel switching control. The free-wheel period becomes subinterval 3 in the proposed operation as illustrated in Fig. 6(a). Free-wheel switching traps the inductor current in a closed loop with a finite resistance. During the free-wheel period, redundant current is consumed by the finite resistance. Power dissipation is proportional to the inductor current. There is a tradeoff between power conversion efficiency and transient recovery time. Second, it restrains energy from transferring to the output by fixing the operation period of subinterval 2, as shown in Fig. 6(a). As a conventional

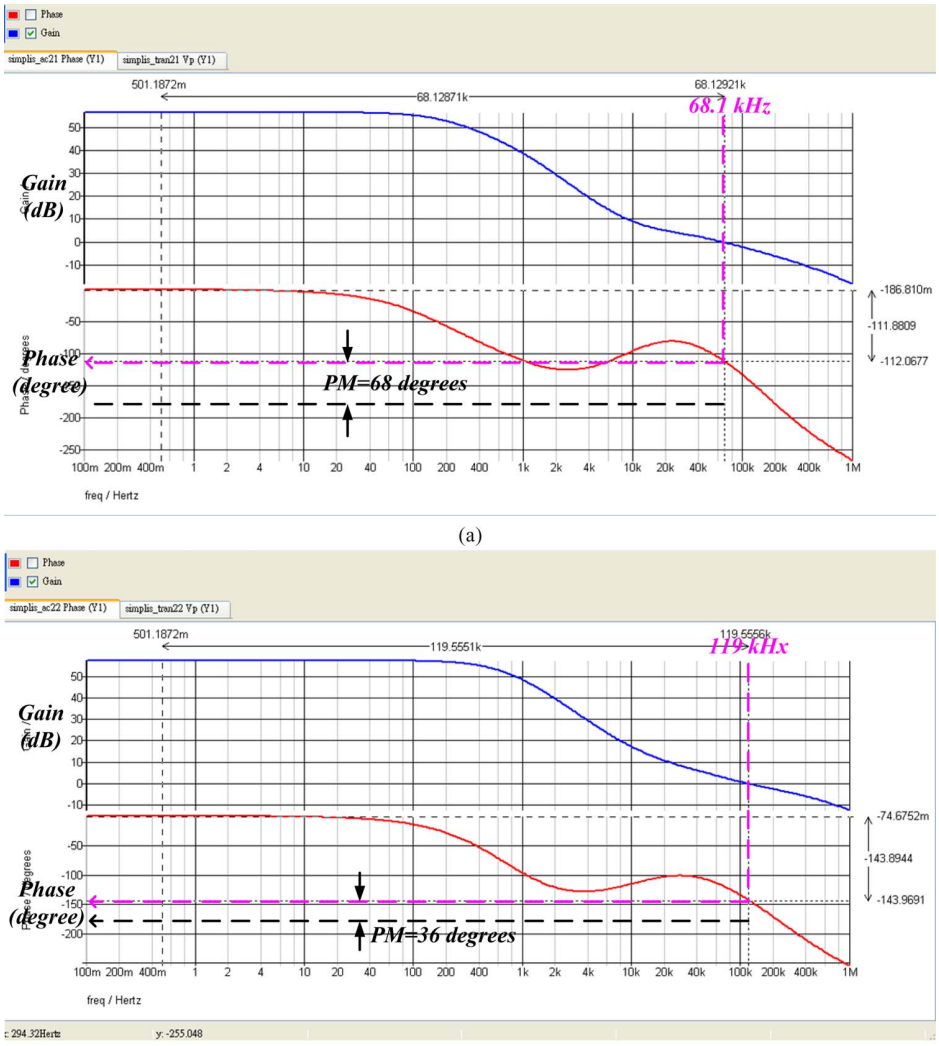


Fig. 8. (a) AC analysis of conventional boost converter at heavy load of 250 mA. (b) AC analysis of the proposed converter at heavy load with the activated WTE technique.

boost converter still transfers stored energy in the inductor to the output under an overshoot condition, a fixed period of subinterval 2 is a good choice to restrain the energy and avoid system instability due to a very small value of subinterval 2.

Fig. 6(a) shows the inductor current waveforms of a converter with or without the OSS technique. The current waveform of a conventional boost converter is represented by the black solid line, and that of a boost converter with the OSS technique is represented by the red solid line. When the inductor current is lower than $I_{L\,(\mathrm{light})}$ and the light-load detection is triggered, the OSS technique is enabled. The main difference between the proposed converter with OSS technique and conventional boost converter is the charge transferred to the converter output. In Fig. 6(a), the yellow areas, *A1–A3*, represent the transferred charge of a conventional boost, and the blue areas, *B1–B3*, indicate that of the proposed converter. Referring to *A1*, the *A1–A3* and *B1–B3* areas after normalization are shown in Fig. 6(b). In comparison, the total excess charge is shown in Fig. 6(c). These results show that the excess charge sent by the proposed OSS technique to the output is less than half of a conventional boost converter. They demonstrate that the overshoot voltage of the OSS technique is smaller than that of a conventional design.

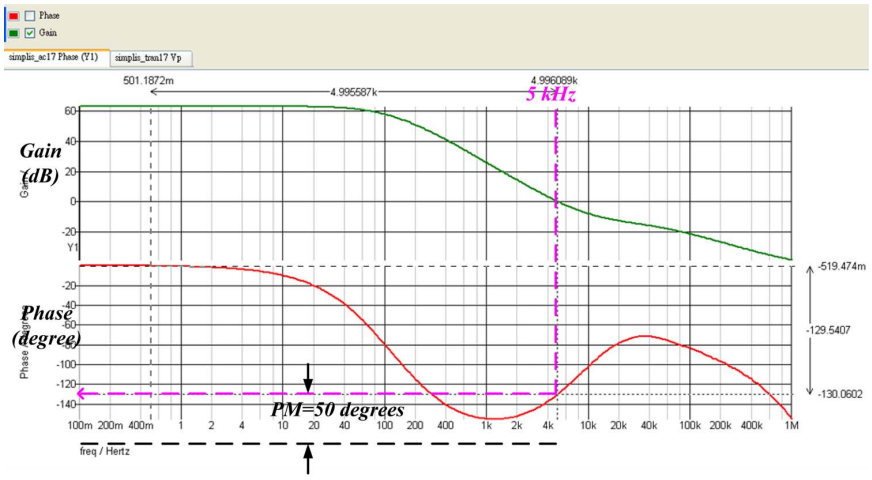
Moreover, the period of subinterval 2 is decided by the equation, as shown in (1)

$$T_{\mathrm{subinterval\,1}} + T_{\mathrm{subinterval\,2}} + T_{\mathrm{subinterval\,3}} = T_{\mathrm{period}}. \quad (1)$$

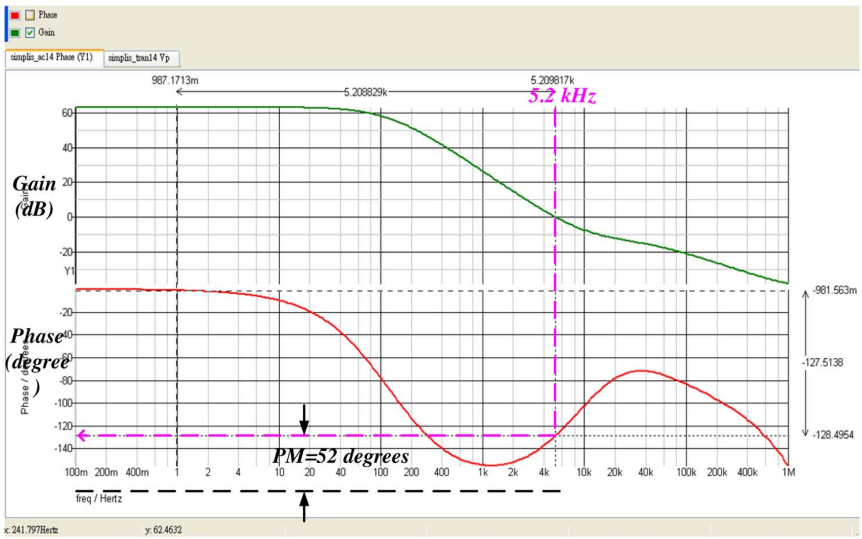
$T_{\mathrm{subinterval1}}$, $T_{\mathrm{subinterval2}}$, and $T_{\mathrm{subinterval3}}$ indicate the time periods of subinterval 1, subinterval 2, and subinterval 3, respectively. When a converter operates in a steady state, the relation of subinterval *1* and subinterval 2 is expressed in (2)

$$(T_{\mathrm{subinterval\,1}} + T_{\mathrm{subinterval\,2}}) = (V_{\mathrm{OUT}}/V_{\mathrm{IN}}) * T_{\mathrm{subinterval\,2}}. \quad (2)$$

Usually, in DSC applications, the minimum input voltage, V_{IN}, is 1.8 V, and the maximum output voltage, V_{OUT}, is 5 V. According to (2), the value of $(T_{\mathrm{subinterval1}} + T_{\mathrm{subinterval2}})$ is approximately equal to 2.78 times the value of $T_{\mathrm{subinterval2}}$. If $T_{\mathrm{subinterval2}}$ is chosen as 30% of the entire switching period, then the value of $(T_{\mathrm{subinterval1}} + T_{\mathrm{subinterval2}})$ is 83% of the



(a)



(b)

Fig. 9. (a) AC analysis of conventional boost converter at light load current of 20 mA. (b) AC analysis of the proposed converter at light load of 20 mA with the activated OSS technique.

entire switching period. The remaining period of $T_{\mathrm{subinterval3}}$ is only 17%. In other words, a very large value of $T_{\mathrm{subinterval2}}$ results in a small value of the free-wheel period $T_{\mathrm{subinterval3}}$. For example, according to I/O voltage setting above, the maximum value of $T_{\mathrm{subinterval2}}$ is 36%, while $T_{\mathrm{subinterval3}}$ is 0% of the entire switching period.

A simple method to detect light load conditions is proposed (Fig. 7). The transistor N_{DUMMY} is biased by a constant current source I_{BIAS}, and the size ratio between transistors N_{DUMMY} and *N1* is 1/M. Switches *S1* and *S2* are controlled by the signal V_{GL}, which is the gate driver of the power MOSFET *N1*. When the power MOSFET *N1* is turned ON, switches *S2* and *S1* turn ON and OFF, respectively, to sense the drain-source voltage of transistor *N1*.

Ignoring the parasitic series resistance of the inductor and the transistors, the detected light load current $I_{L\,(\mathrm{light})}$ is expressed as (3)

$$I_{L\,(\mathrm{light})} = M \times I_{\mathrm{BIAS}}. \tag{3}$$

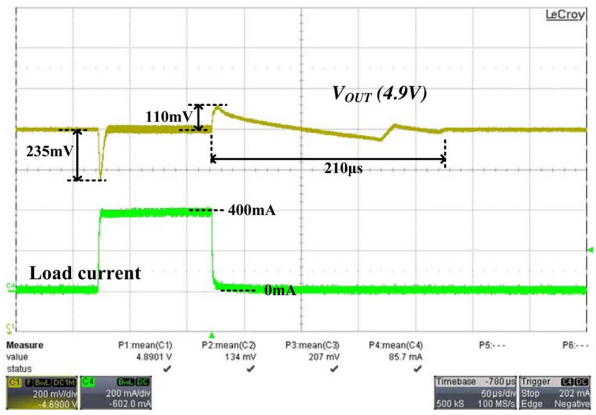


Fig. 10. Measurement results of load transient response of a conventional boost converter.

For example, $I_{L\,(\mathrm{light})}$ is 100 mA if $M = 50000$ and I_{BIAS} is 2 μA. To operate the OSS technique earlier than the DCM operation at light loads, the value of $I_{L\,(\mathrm{light})}$ should be larger

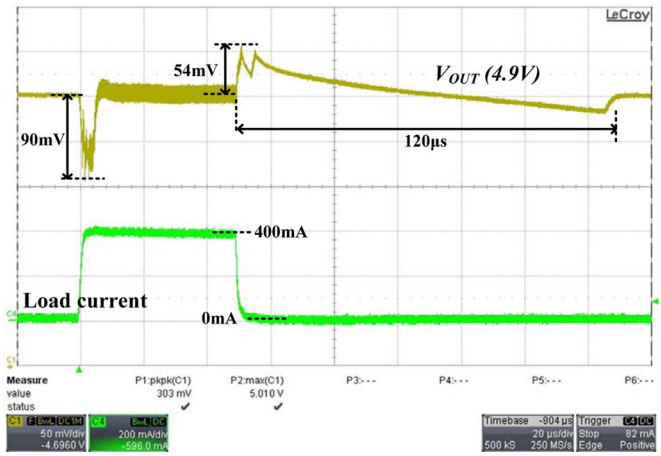


Fig. 11. Measurement results of load transient response of the proposed boost converter.

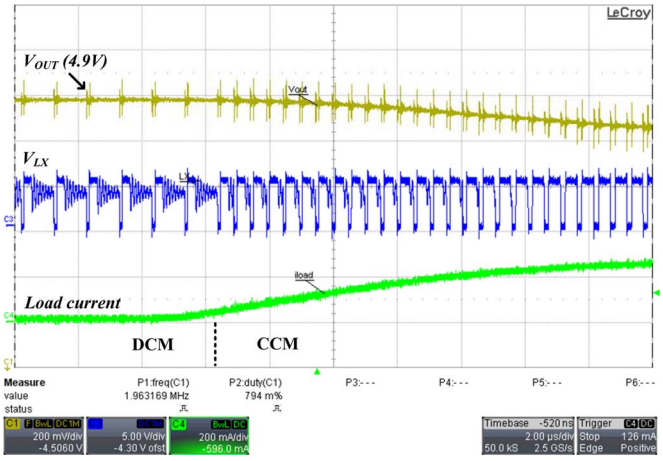


Fig. 12. Measurement waveform of a conventional boost converter from light load to heavy load.

than that of the inductor current at CCM/DCM boundary condition $I_{L\,(\mathrm{boundary})}$. Equation (4) denotes the boundary condition between the CCM and DCM operations, where L is the inductor value, D is the duty cycle in steady state, and T_s is the period

$$I_{L(\mathrm{boundary})} = \frac{V_{\mathrm{IN}} \times DT_S}{2L}. \tag{4}$$

Although a large value of $I_{L\,(\mathrm{light})}$ can be set to make the OSS operate much earlier, it results in more power loss and lower power conversion efficiency than the CCM mode operation at the same load current condition.

V. Experimental Results

The proposed boost converter with OSS technique is fabricated in a 0.4 μm CMOS technology. The converter output voltage is about 4.9 V, and the input voltage is 3 V. The total feedback resistance is 564 kΩ, with the built-in reference set to 0.8 V.

Fig. 8 is the AC analysis of conventional and the proposed boost converters in the CCM and proposed converter with the activated WTE technique at heavy-load condition of 250 mA. The proposed converter with the activated WTE technique has higher cross-over frequency than that of conventional boost converter at the cost of degraded phase margin. Fig. 9 is the ac analysis of conventional and the proposed boost converters in the DCM at light-load condition of 20 mA. The proposed converter with the activated OSS technique has similar cross-over frequency as that of conventional boost converter.

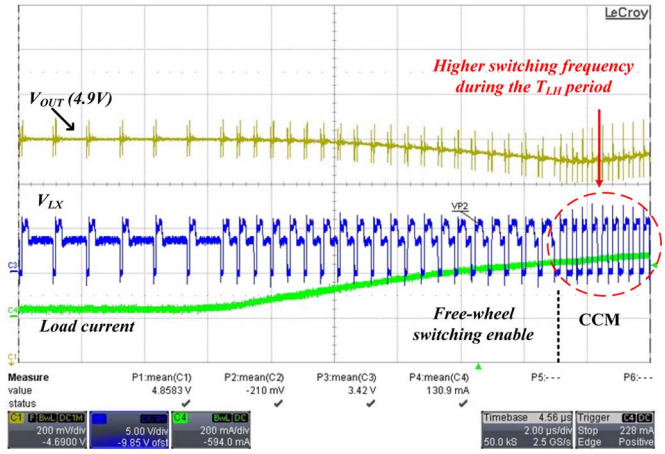


Fig. 13. Measurement waveform of the proposed boost converter from light load to heavy load.

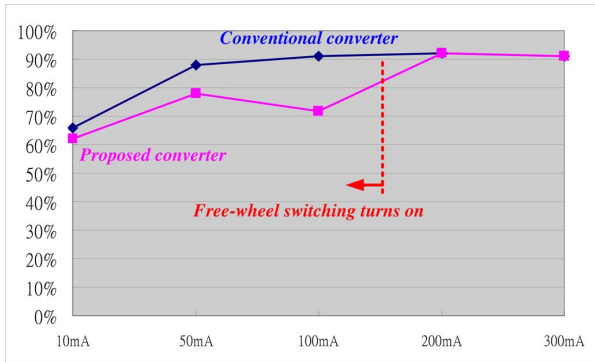


Fig. 14. Efficiency comparison of boost converter with and without OSS technique.

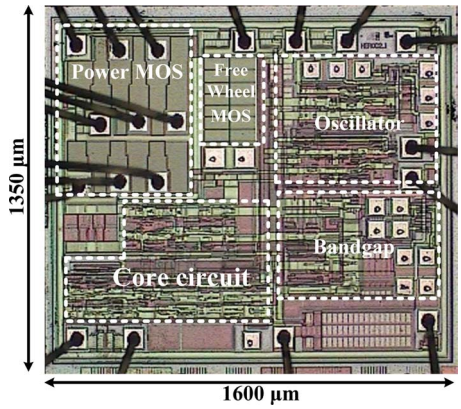


Fig. 15. Chip micrograph.

TABLE I
DESIGN SPECIFICATIONS

Technology	*0.4 μm CMOS process*
Inductor (off-chip)	*2.2 μH*
Capacitor (off-chip)	*20 μF*
Input voltage	*2.7 V ~ 4.3 V*
Output voltage	*2.7 V ~ 5 V (Typical application)*
Switching frequency	*2 MHz*
Load transient range	*0 mA-400 mA*

TABLE II
PERFORMANCE SUMMARY

	Proposed converter	*Conventional converter*
Load transient from 0 mA to 400 mA	*90 mV*	*235 mV*
Load transient from 400 mA to 0 mA	*54 mV*	*110 mV*
Settling time (load current changes from 400 mA to 0 mA	*120 μs*	*210 μs*

Fig. 10 shows the measured waveform of a conventional boost converter when the load current changes from 400 mA to 0 mA load. The drop voltage and overshoot voltage during load transient are about 235 mV and 110 mV, respectively. The settling time is 210 μs at no-load condition. A longer settling time is observed because there is no load, and the feedback resistance at the output is high.

The same transient condition and external component are used for comparison between a conventional design and the proposed method, as shown in Fig. 11. The output drop voltage is reduced from 235 to 90 mV and the overshoot voltage is effectively reduced from 110 to 54 mV. Furthermore, the settling time is decreased to 120 μs, which is 43% better than that of a conventional boost converter.

Fig. 12 shows the transient waveform of a conventional boost converter with a gradual increase in load current. According to the load current, the converter is in the DCM and CCM modes. Fig. 13 shows the mode transient waveform with an increase in load current. At light loads, free-wheel switching is turned ON in the beginning. The CCM operation replaces the operation of the free-wheel switching when the inductor current increases high enough to push the converter into heavy load operation. Higher switching frequency waveform can be observed when the WTE technique is activated during the T_{LH} period and shown at the right-hand-side of Fig. 13. This mechanism is turned OFF when the converter reaches its steady state.

Fig. 14 is the efficiency comparison between the conventional and the proposed converters. The proposed converter has lower efficiency performance due to the free-wheel switching operation. After the free-wheel switching is turned OFF at heavy load, the efficiency comes back to the value similar to that of the conventional boost converter. The chip micrograph of the proposed converter is shown in Fig. 15. The die size is 2.16 mm^2. The operation frequency is 2 MHz. Table I shows the specifications of the proposed converter and Table II summarizes the performance of the proposed converter.

VI. CONCLUSION

In this paper, a boost converter with the WTE and the OSS techniques is presented. This work provides a simple method of reducing overshoot during load transient from heavy load to very light load. The design and simulation are based on 0.4 μm CMOS technology and show a reduced overshoot voltage that ensures the performance of DSC systems. Simulation and measurement results demonstrate how overshoot and settling time are effectively reduced using a combination of the WTE and the OSS techniques at light loads. The improved drop reduction and overshoot reduction are about 62% and 51%, respectively.

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Yean-Kuo Luo was born in Tainan, Taiwan. He received the B.S. and M.S. degrees from the Institute of Microelectronics, Nation Cheng Kung University, Tainan, Taiwan, in 2001 and 2003, respectively, where he is currently working toward the Ph.D. degree.

He is a Faculty Member at the Mixed-Signal and Power Management Integrated Circuit Laboratory, Institute of Electrical Control Engineering, National Chiao Tung University, Hsinchu, Taiwan.

Chao-Chang Chiou was born in Taoyuan, Taiwan. He received the B.S. degree from Fu Jen Catholic University, Taipei, Taiwan, in 2008, and the M.S. degree from National Central University, Taoyuan, Taiwan, in 2010, at the Department of Electrical Engineering, where he is currently working toward the Ph.D. degree from the Institute of Electrical Control Engineering, National Chiao Tung University, Hsinchu, Taiwan.

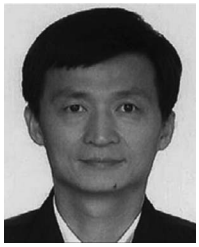
He is a Faculty Member at the Mixed-Signal and Power Management Integrated Circuit Laboratory, Institute of Electrical Control Engineering, National Chiao Tung University. His current research interests include the power management integrated circuit design and analog integrated circuit designs.

Chun-Hsien Wu was born in New Taipei City, Taiwan. He received the B.S. degree from the National Taiwan University of Science and Technology, Taipei, Taiwan, in 2007, and the M.S. degree from the National Tsing Hua University, Hsinchu, Taiwan, in 2010, both in electrical engineering, where he is currently working toward the Ph.D. degree in electrical and control engineering from the National Chiao Tung University, Hsinchu, Taiwan.

The main research area during his M. S. career was microelectronic and mechanical systems (MEMS), which include bio-MEMS and microsensor design. His current research includes the power management integrated circuit design and mixed-signal integrated circuits design.

Ke-Horng Chen (M'04–SM'09) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 1994, 1996, and 2003, respectively.

From 1996 to 1998, he was a part-time Integrated Circuit Designer at Philips, Taipei. From 1998 to 2000, he was an Application Engineer at Avanti, Ltd., Taiwan, and from 2000 to 2003, he was a Project Manager at ACARD, Ltd., where he was engaged in designing power management ICs. He is currently an Associate Professor in the Department of Electrical Engineering, National Chiao Tung University, Hsinchu, Taiwan, where he organized a Mixed-Signal and Power Management IC Laboratory. He is the author or coauthor of more than 80 papers published in journals and conferences, and also holds several patents. His current research interests include power management ICs, mixed-signal circuit designs, display algorithm and driver designs of liquid crystal display TV, red, green, and blue color sequential backlight designs for optically compensated bend panels, and low-voltage circuit designs.



Wei-Chou Hsu (M'87) was born in Taichung, Taiwan, on May 28, 1957. He received the B.S., M.S., and Ph.D. degrees from the National Cheng Kung University (NCKU), Tainan, Taiwan, all in electrical engineering, in 1979, 1981, and 1984, respectively. In 1979, he passed the National Higher Civil Service Examination and received the Technical Expert License of the Republic of China in electrical engineering.

In 1983, he was with Four Dimensions Company, California, as an Engineer. From 1982 to 1985, he was an Instructor with the Department of Electrical Engineering, NCKU, and since 1985, he has been an Associate Professor. From 1991 to 1992, he was a Postdoctoral Researcher with the Department of Electrical Engineering, University of Florida, Gainesville. Since 1993, he has been a Professor with the Department of Electrical Engineering, NCKU. During 2000–2005, he was an Associate Chair with the Department of Electrical Engineering, NCKU, and the Chair of the Institute of Microelectronics, NCKU. Between 2005 –and 2008, he was the Chair of the Department of Electrical Engineering, NCKU. Since 2008, he has been the Chair of the Advanced Optoelectronic Technology Center, NCKU. His research interests include metal–organic chemicalvapordeposition and molecular-beam-epitaxy-grown pseudomorphic heterostructure field-effect transistors, d-doped FETs, high-power FETs, heterojunction bipolar transistors, organic light-emitting diodes, and organic photovoltaic devices.