A Robust Frequency Tracking Loop for Energy-Efficient Crystalless WBAN Systems

Wei-Hao Sung, Jui-Yuan Yu, and Chen-Yi Lee

***Abstract*—This brief presents a frequency tracking loop (FTL) to realize a crystalless wireless sensor node (WSN) for wireless body area network (WBAN). By tracking a remote wireless RF reference for system clock calibration, the proposed FTL allows WSNs to tolerate a large-frequency error from on-chip CMOS oscillators. Moreover, to achieve energy-efficient transmissions in crystalless, a sufficiently accurate convergence clock is required to enable burst overmegabits-per-second system throughput with minimized operation duty cycle. For the dedicated purpose, a comparison-based binary-search tracking scheme, which ensures accurate and robust convergence against noisy wireless channel, is further developed to manage the operation of FTL. The intermediate frequency back-end part of FTL is implemented in 90-nm CMOS process. Measurement results show that the FTL extends an initial tolerance of system clock error to $\pm 3\%$ and achieves a final quartz-crystal comparable ± 50-ppm accuracy. This enables 4.85-Mb/s wireless links and improves 79% energy efficiency by RF operation-time reduction, giving a power-saved and miniaturized WSN device for WBAN applications.**

***Index Terms*—Crystalless, frequency calibration, on-chip oscillator, process, voltage and temperature (PVT) variation, wireless body area network (WBAN).**

I. Introduction

CURRENTLY, an emerging standard for wireless body area network (WBAN) applications is under development by IEEE 802.15 Task Group 6 [1]. Different from Bluetooth and ZigBee, it is specifically designed for medical or multimedia communication in, on, or around human bodies. A typical WBAN system contains several wireless sensor nodes (WSNs) for data sensing, storing, and processing, whereas a central processing node (CPN) is in charge for collecting WSNs data through a short-range channel for back-end services [2].

WSN design has various severe restrictions. First of all, it is essential to use small battery or energy harvesting techniques, whose available output power is often less than 500 μW [3], to avoid expensive and impractical battery replacement. Hence, under the supply power limitation while maintaining several years' lifetime, WSN power must be extremely low. On the other hand, minimized production cost and tiny size integration for comfortable wearing are also crucial considerations. Unfortunately, the quartz crystal, as a conventional reference frequency generator, remains a bottleneck to meet these requirements. Its heterogeneous integration with a CMOS process occupies bulky on-board passive components, which increase power, area, and manufacture cost at the same time. Consequently, it is desirable to replace the quartz crystal with an on-chip CMOS oscillator in WSN [4]–[6].

The major design challenge to realize an all-CMOS crystalless WSN is the limited system throughput caused by degraded oscillator frequency accuracy. Due to process, voltage and temperature (PVT) variations, the achievable accuracy in standalone CMOS oscillators based on analog or digital compensation circuits is between $\pm 0.5\%$ to $\pm 3\%$ [7], [8]. However, the conventional timing and frequency synchronization techniques in wireless systems could only tolerate few hundreds parts per million of carrier frequency offset and sampling clock offset. In order to compromise such incompatible provided accuracy, existing crystalless systems usually operate at submegabits-per-second data rate under specific modulation scheme and protocol [4] or merely rely on constant voltage and temperature environments [5], which certainly constrains WBAN operation scenarios. Inevitably, the limited throughput results in longer system duty cycle (wakeup duration) and inefficient energy dissipations from power-hungry RF front-end static bias currents. For an optimized energy-efficient link, a sufficiently accurate system clock is required to enable burst overmegabits-per-second data transmissions [9], [10] and thus minimize the system operation duty cycle.

Accordingly, to achieve all-CMOS crystalless integration, a frequency tracking loop (FTL) [12], which calibrates the WSN clock frequency by tracking a sinusoidal RF reference broadcasted from CPN wirelessly, is proposed to extend the system clock error tolerance compatible with on-chip oscillators [7], [8]. Moreover, to enhance the throughput of crystalless systems for energy saving, a comparison-based binary-search tracking (CBST) scheme, which ensures robust and accurate convergence performance against noisy wireless channel, is further developed to manage the operation of FTL.

In this brief, the FTL design [12] is presented in detail. The rest of the parts are organized as follows. Section II discusses the FTL architecture and highlights major design considerations of system stability. Section III introduces the CBST scheme for robust FTL control and analyzes its convergence performance. Section IV reports the experimental results of the proposed FTL. Finally, this work is concluded in Section V.

II. System Descriptions

A. FTL Architecture

Fig. 1 shows a crystalless WSN receiver architecture with the proposed FTL, where notation f on data paths indicates the signal frequency. In CPN, target clock frequency f_O is

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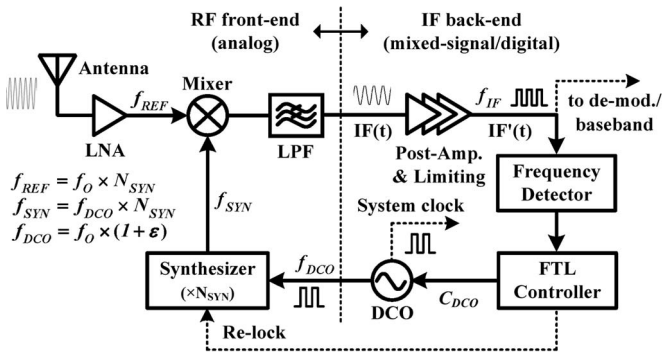

Fig. 1. Crystalless WSN receiver architecture with the proposed FTL.

multiplied $N_{\rm SYN}$ times by the synthesizer as single-carrier RF reference $f_{\rm REF}$ transmitted to WSN. In WSN, for the simple property of frequency tuning, a digitally controlled oscillator (DCO) is utilized to generate system clock $(f_{\rm DCO})$, whose frequency error is defined as $\varepsilon = |(f_{\rm DCO} - f_O)/f_O|$. By down-converting RF reference, IF signal reflects the degree of DCO frequency error, i.e., $f_{\rm IF} = N_{\rm SYN} \cdot f_O \cdot \varepsilon$. To identify ε, a frequency detector (FD) is applied to quantize $f_{\rm IF}$. According to FD outputs, FTL controller generates digital codeword $(C_{\rm DCO})$ to adjust $f_{\rm DCO}$ toward f_O iteratively.

Similarly, [6] and [13] perform wireless reference tracking for on-chip synthesizer voltage-controlled oscillator calibration. As a contrast, in the proposed FTL, decision blocks and related signal processing are entirely designed in mixed-signal and digital domains at low-IF band, whereas RF front-end structures remain unchanged. Instead of $N_{\rm SYN}$ adjustment (RF-band $f_{\rm SYN}$ calibration), the architecture of direct $f_{\rm DCO}$ control prevents using power-hungry fractional-N synthesizer and extra frequency dividing for system clock usage. Additionally, since the FTL is a frequency lock loop using noisy wireless reference, this digital implementation is necessary and much easier to ensure tracking accuracy and stability at the same time, which have not been considered and solved in [6] and [13].

B. System Stability Considerations

FTL is designed to detect a frequency error up to $\varepsilon_{\max}$ and calibrates $f_{\rm DCO}$ to an error less than ε_O for overmegabits-per-second links. To cover large $\varepsilon_{\max}$ from CMOS oscillators, the LPF bandwidth must extend to at least ${\rm BW_{IF}} = f_{\rm REF} \cdot \varepsilon_{\max}$. Thus, IF signal, represented as ${\rm IF}(t)$, not only contains the interested sinusoidal signal $f_{\rm IF}$ but also carries a noise term with bandwidth ${\rm BW_{IF}}$. Inevitably, the convergence accuracy becomes quite sensitive to SNR condition. The choice of FD and corresponding FTL ε cancellation scheme are critical design issues of stability.

The FD design in FTL negative feedback loop can be realized by two approaches. One intuitive approach is applying a frequency estimator (FE) to determine exact $f_{\rm IF}$ values. The optimal maximum-likelihood FE for sinusoidal signals is discrete Fourier transform (DFT), but it requires high sample rate $(2{\rm BW_{IF}})$ analog-to-digital converter for large $\varepsilon_{\max}$ and high-point DFT for accurate ε_O. A low-complexity alternative is to use a frequency counter (FC) shown in Fig. 2(a) according to

$$|\hat{\varepsilon}| = N_{\rm IF}/(N_{\rm DCO} \cdot N_{\rm SYN} - N_{\rm IF}) \triangleq \varepsilon_{\rm FE} \qquad (1)$$

where $f_{\rm DCO}$ and $f_{\rm IF}$ are quantized to $N_{\rm DCO}$ and $N_{\rm IF}$ by two edge counters. Target $C_{\rm DCO}$ is calculated by multiplying $1 \pm$

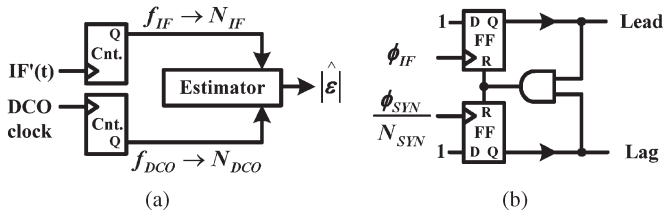

Fig. 2. FD design based on (a) frequency counter estimation and (b) PFD.

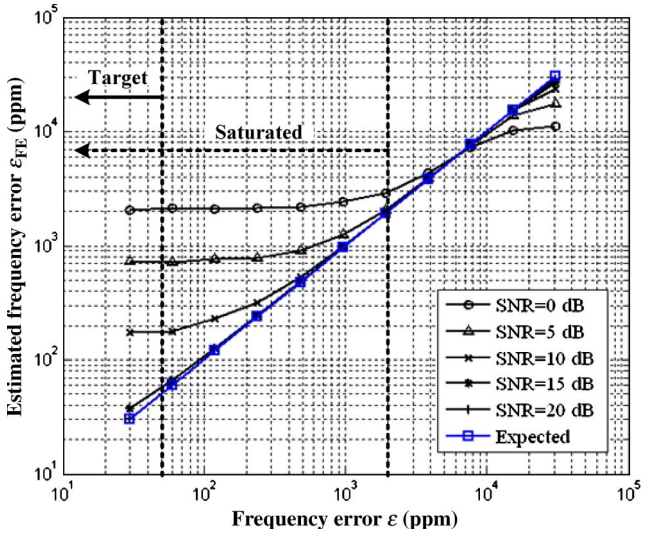

Fig. 3. Estimation performance of FC-FE approach under different SNR.

$\varepsilon_{\rm FE}$. Another approach is to utilize a phase-frequency detector (PFD) to detect the lead and lag information in phase domain, as shown in Fig. 2(b), where $\phi_{\rm SYN}$ and $\phi_{\rm IF}$ are the phases of synthesizer output and ${\rm IF}(t)$. Based on [6], $f_{\rm DCO}$ can be calibrated to f_O by modifying the reference signal to $f'_{\rm REF} = f_{\rm REF} \cdot (N_{\rm SYN} - 1)/N_{\rm SYN}$. However, for a received noisy wireless reference, conventional FDs and control schemes cannot ensure robust convergence as in normal phase/frequency-locked loop (PLL/FLL) circuits. The relatively wideband noise certainly influences FDs to extract real $f_{\rm IF}$ from ${\rm IF}(t)$, particularly when ε is approaching to ε_O. FD's trigger clock, i.e., ${\rm IF}'(t)$ or $\phi_{\rm IF}$ in Fig. 2, contains induced glitches that disturb actual clock positions or edge counting values. As a result, minimal detectable ε is limited. For instance, Fig. 3 shows the estimation performance of FC-FE approach in (1). The final accuracy saturates early at thousands part per million before FTL achieves target region in a low-SNR case.

Although a Schmitt trigger circuit can be applied in FDs to suppress external noise, its comparison threshold is not suitable to rise too much in our case. This is because the gain stages in FTL signal path are not specifically designed for ${\rm IF}(t)$ whose bandwidth is much wider than original baseband signal. Without modifying the gain control specification, the FTL only applies the Schmitt trigger to filter few noise transitions around zero crossing. For entirely stable convergence, a CBST scheme with modified FD is then proposed to manage FTL operations.

III. Proposed CBST Control Scheme

A. CBST Control Operation

Fig. 4 shows the simplified block diagram of the proposed CBST controller in FTL and its related signal path. One counter

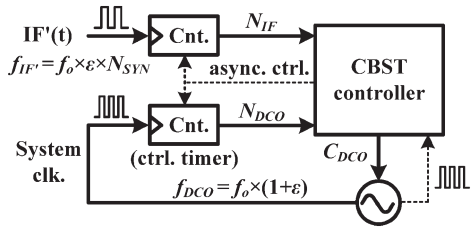

Fig. 4. Simplified block diagram of CBST controller and related signal path.

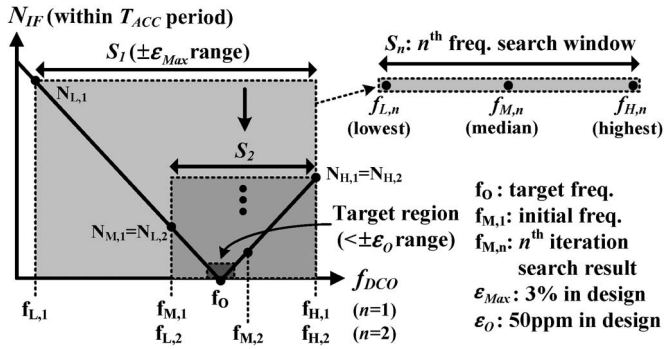

Fig. 5. Search procedure of the proposed CBST controller.

is triggered by DCO clock, and the other is triggered by $\mathrm{IF}'(t)$. The FE-like counting structure provides wide detectable range for large $\varepsilon_{\max}$. To prevent unstable loop behavior, the decisions of CBST scheme do not rely on either exact edge trigger counts or positions that may have external noise included. Instead, the N_{IF} values corresponding to different f_{DCO} are compared. Then, target C_{DCO} is determined by searching the frequency with relatively lower N_{IF}, which represents that the selected frequency is closely adjacent to f_O. For this purpose, the counter in Fig. 4 is in charge to set up constant time duration T_{ACC} according to appropriate N_{DCO} control for N_{IF} accumulation.

Fig. 5 illustrates the search procedure of the CBST controller. Assume that the channel noise is temporarily ignored. The V-shape characteristic curve indicates the relation of f_{DCO} and N_{IF} values within T_{ACC} duration. Since accumulated N_{IF} is directly proportional to ε, it is straightforward to adjust f_{DCO} toward our target region within $(1 \pm \varepsilon_O) \cdot f_O$ by searching the valley in the characteristic curve. To speed up FTL tracking time, the proposed search procedure operates based on a binary-search manner modified from fast locking PLL controllers [11]. For the ease of explanation, frequency search window S_n for nth binary-search iteration is defined by its lowest, highest, and median frequencies, denoted by $f_{L,n}$, $f_{H,n}$, and $f_{M,n}$, respectively. Note that $f_{M,n}$ represents the FTL search result in nth iteration. Initially, $f_{M,1}$ is set to the DCO free-running frequency whose error is less than tolerable value $\varepsilon_{\max}$, whereas $f_{H,1}$ and $f_{L,1}$ are set to $(1 + / - \varepsilon_{\max}) \cdot f_{M,1}$, respectively, to construct S_1. Starting from S_1, which determines the maximum search boundary, the CBST search procedure is performed by continuously comparing N_{IF} values corresponding to $f_{L,n}$ and $f_{H,n}$, denoted by $N_{L,n}$ and $N_{H,n}$. The frequency with less N_{IF} value in $f_{L,n}$ and $f_{H,n}$, together with $f_{M,n}$, is chosen to set up next window S_{n+1}. For example, S_2 is set up by $f_{H,1}$ and $f_{M,1}$ from S_1 since $N_{H,1}$ is less than $N_{L,1}$. This procedure always chooses the frequency region corresponding to the half-side characteristic curve with lower ε. Search window S_n is iteratively reduced by half from initial $\pm\varepsilon_{\max}$ to convergence

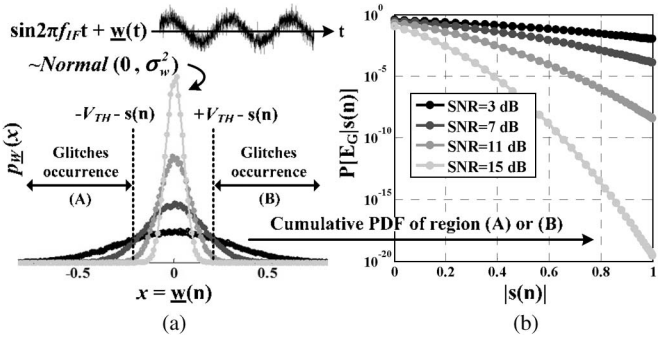

Fig. 6. (a) PDF of $\underline{w}(n)$. (b) Probability of E_G for a given $s(n)$.

$\pm\varepsilon_O$, and median frequency $f_{M,n}$ finally locates in target region after $\lceil \log_2(\varepsilon_{\max}/\varepsilon_O) \rceil$ iterations.

The CBST controller generates control code C_{DCO} for f_{DCO} adjustment according to relation $f_{\mathrm{DCO}} = (f_O \cdot \varepsilon_O)/C_{\mathrm{DCO}}$, which is a reciprocal ratio transform. Thus, binary search median $f_{M,n}$ can be controlled by $C_{M,n} = 2 \cdot (C_{L,n} \cdot C_{H,n})/(C_{L,n} + C_{H,n})$, where $C_{L,n}$ and $C_{H,n}$ are C_{DCO} for $f_{L,n}$ and $f_{H,n}$, respectively. In addition, the relation also implies that the frequency scalar operation, such as $(1 \pm \varepsilon_{\max}) \cdot f_{M,1}$ for S_1 setup or N_{DCO} control for constant T_{ACC} setup, can be performed by direct scalar division of C_{DCO}.

B. Convergence Analysis

In the following, the channel noise is considered for FTL convergence stability analysis. $\mathrm{IF}(t)$ consists of sinusoidal signal $s(t) = \sin(2\pi \cdot f_{\mathrm{IF}} \cdot \mathrm{t})$ and carried noise $\underline{w}(t)$. The $\underline{N}_{\mathrm{IF}}$ value, triggered by $\mathrm{IF}'(t)$, is written as $\underline{N}_{\mathrm{IF}} = T_{\mathrm{ACC}}/T_{\mathrm{IF}} + \underline{N}_G$, where $\underline{N}_G$ is unwanted glitch counting from $\underline{w}(t)$ and $T_{\mathrm{IF}} = 1/f_{\mathrm{IF}}$. Note that the notation underlined represents a random variable. The distribution of $\underline{N}_G$ can be modeled as a binomial (Bernoulli) experiment of glitch occurrence, which is called event E_G, under $N_{\mathrm{Trail}} = T_{\mathrm{ACC}}/T_D$ times of trails, where T_D is the minimum glitch transition width that can be captured by the counter as one success trigger count. The condition for event E_G to happen is

$$E_G : \underline{\mathrm{IF}}(n) = s(t) + \underline{w}(t)|_{t=\frac{n}{T_D}} \begin{cases} \geq +V_{\mathrm{TH}}, & \text{for } s(n) < 0 \\ \leq -V_{\mathrm{TH}}, & \text{for } s(n) > 0 \end{cases} \quad (2)$$

where V_{TH} is the decision threshold of limiting comparator (or Schmitt trigger circuit). Assume that the probability density function (PDF) of $\underline{w}(n)$, denoted by $p_{\underline{w}}(x) = P[\underline{w}(n) = x]$, is white Gaussian distribution $\sim$ Normal$(0, \sigma_w^2)$. The probability of E_G under deterministic $s(n)$, denoted by $P[E_G|s(n)]$ shown in Fig. 6(b), can be calculated by integrating $p_{\underline{w}}(x)$ values for x satisfying (2), as the tail regions indicated in Fig. 6(a). Hence, the expected $P[E_G|s(n)]$ in one T_{IF} duration, that is, $P(E_G) = E[P[E_G|s(n)]]$, is derived from

$$P\left[E_G|s(n)\right] = \int_{\frac{(V_{\mathrm{TH}}+|s(n)|)}{\sigma_w}}^{\infty} \frac{e^{-x^2/2}}{\sqrt{2\pi}} dx \triangleq Q\left(\frac{V_{\mathrm{TH}} + |s(n)|}{\sigma_w}\right)$$

$$\text{Then, } P(E_G) = \frac{1}{T_{\mathrm{IF}}/T_D} \cdot \sum_{n=0}^{T_{\mathrm{IF}}/T_D - 1} \left[Q\left(\frac{V_{\mathrm{TH}} + |s(n)|}{\sigma_w} \right) \right] \quad (3)$$

where $Q(\cdot)$ is the right-side tail probability of standard normal distribution. For large N_{Trail}, binomial $\underline{N}_G$ can

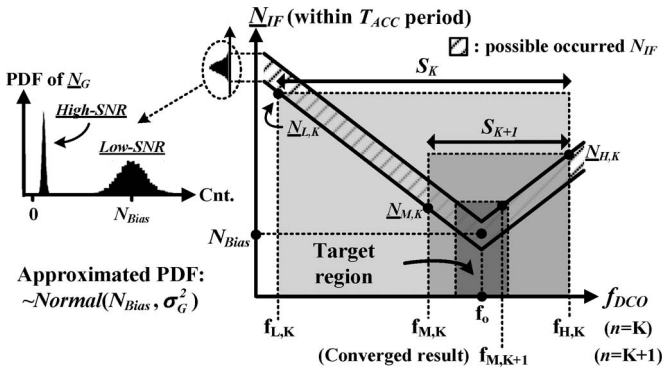

Fig. 7. CBST search procedure considering channel noise influence.

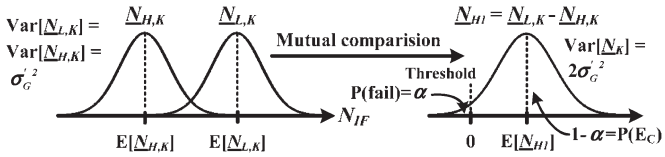

Fig. 8. Simplified PDF model for CBST convergence ability analysis.

be approximated to Gaussian distribution with $E[\underline{N}_G] = N_{\text{Trail}} \cdot P(E_G) \triangleq N_{\text{Bias}}$ and $\text{Var}[\underline{N}_G] = N_{\text{Trail}} \cdot P(E_G) \cdot [1 - P(E_G)] \triangleq \sigma_G^2$. Obviously, N_{Bias} and σ_G^2 are mainly determined by N_{Trail} and σ_w but remain nearly constant for different ε after averaging. Considering the effect of $\underline{N}_G$, the CBST operation in Fig. 5 is redrawn as Fig. 7, where original $\underline{N}_{\text{IF}}$ is shifted upward by N_{Bias} and appears within the region of variance σ_G^2 in statistics.

It is hard to estimate $\underline{N}_G$ from $\underline{N}_{\text{IF}}$ since either IF(t) under large ε or low-SNR condition eventually increases $\underline{N}_{\text{IF}}$ at the same time. Instead of general $\underline{N}_G$ extractions, the proposed CBST search scheme mutually compares $\underline{N}_{\text{IF}}$ between $f_{L,n}$ and $f_{H,n}$ to cancel the nonzero biased N_{Bias} automatically. Thus, the FTL convergence is only affected by σ_G^2. If we further enlarge T_{ACC} period to $T'_{\text{ACC}} = T_{\text{ACC}} \cdot \text{L}$ for time average, σ_G^2 can be reduced to $\sigma_G'^2 = \sigma_G^2/\text{L}$ based on the central limit theorem. Then, the boundary condition at final iteration $n = K$ in Fig. 7 can be analyzed to investigate whether the decision of $\underline{N}_{L,K} > \underline{N}_{H,K}$ is correct. As the simplified PDF model shown in Fig. 8, the comparison between $\underline{N}_{L,K}$ and $\underline{N}_{H,K}$ is equivalent to detection hypothesis $H_1 : \underline{N}_{H1} = \underline{N}_{L,K} - \underline{N}_{H,K} > 0$, where $\underline{N}_{H1}$ is Gaussian with $E[\underline{N}_{H1}] = T'_{\text{ACC}} \cdot f_{\text{REF}} \cdot \varepsilon_O$ and $\text{Var}[\underline{N}_{H1}] = 2\sigma_G'^2$. In other words, the detection rate of H_1 is written as $P(E_C)$, where E_C represents the event of successful convergence. For required convergence rate $P(E_C) \geq 1 - \alpha$, an appropriate T'_{ACC} targeted at final accuracy ε_O is determined by

$$Q\left(\frac{0 - E[\underline{N}_{H1,K}]}{\sqrt{Var[\underline{N}_{H1,K}]}}\right) = Q\left(\frac{-T'_{\text{ACC}} \cdot f_{\text{REF}} \cdot \varepsilon_O}{\sqrt{2\sigma_G'^2}}\right) \geq P(E_C) = 1 - \alpha. \quad (4)$$

As the equality in (4) holds, the corresponding period, denoted by $T'_{\text{ACC},K}$, is sufficient to discriminate minimal search window S_{K+1} from S_K. In fact, T'_{ACC} for iteration $n < K$ need not to be the same as $T'_{\text{ACC},K}$. It is because, for S_n with search region $\pm\varepsilon_n$ larger than final $\pm\varepsilon_O$, the corresponding $E[\underline{N}_{H1}]$ is much far away from zero and less L increment is enough.

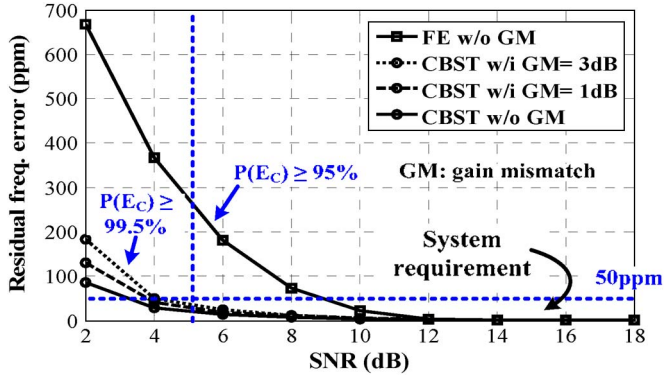

Fig. 9. FTL convergence under AWGN channel and circuit distortions.

Therefore, the optimal T'_{ACC} for nth iteration is obtained by replacing ε_O in (4) with ε_n.

IV. Experimental Results

To verify our proposal, the IF back-end part of FTL is fabricated in 90-nm standard CMOS process. All related RF front-end circuits are set up by the commercial frequency-shift keying (FSK) chip targeted at 433/915-MHz ISM-band. In our demonstration, $\varepsilon_{\max}$ is set to $\pm 3\%$ compatible with [7] and [8], and ε_O requires to be less than ± 50 ppm to enable overmegabits-per-second WBAN systems [9], [10].

In IF-FTL, a DCO is embedded to generate target $f_O =$ 5-MHz system clock with 50-ppm tuning ability. By applying power-of-two (P2) delay structure based on hysteresis delay cells, it covers wide tuning range (200 ns–10 ps) and achieves optimal power and area efficiency for low-power crystalless integrations. Initially, the free-running DCO is self-calibrated by a PVT detector [12] to maintain $\pm 3\%$ clock accuracy for basic WSN operations. As the reference is downconverted, IF(t) is converted to IF$'(t)$ by a Schmitt trigger for coarse noise filtering and square limiting. Then, IF-FTL iteratively performs the CBST calibration.

Fig. 9 shows the simulation results of FTL convergence in AWGN channel. Nonideal circuit distortions in signal path are also considered, including -110 dBc/Hz synthesizer phase noise at 1-MHz offset [6] and IF(t) gain mismatch from amplification stages. For satisfying $P(E_C) \geq 99.5\%$, the proposed FTL ensures the residual frequency error less than ± 50 ppm as SNR ≥ 5 dB. To tolerate possible gain mismatch, comparison threshold V_{TH} is chosen at the level no more than 30% full swing voltage. The results show the FTL is able to tolerate 3-dB gain mismatch (29.2% voltage distortion) under our requirement. The proposed scheme is more accurate and reliable than conventional FE/PFD approach against noise.

Fig. 10 shows the measured FTL convergence accuracy and the required operation time at SNR $= 7$ dB. From initial 3% frequency error, the FTL tracks a $f_{\text{REF}} = 435$ MHz$(N_{\text{SYN}} = 87)$ reference signal transmitted from CPN. By CBST search, DCO accuracy is converged toward ± 50 ppm as the curve indicated from the right side to the left side. To achieve final 23.5-ppm accuracy, the required CBST tracking time in IF-FTL is $T_{\text{IF-FTL}} = 1.06$ ms. Considering the settling time of testing FSK-IC, the total operation time is $T_{\text{FTL}} = 3.06$ ms, which can be minimized if the FSK synthesizer is controllable by our IF-FTL chip. Note that the exact resolution of each DCO

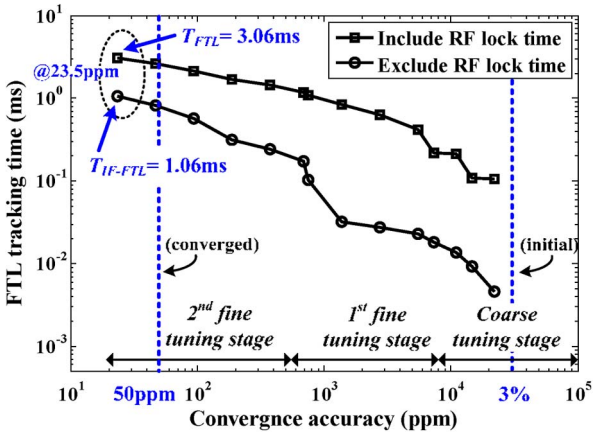

Fig. 10. Measured FTL convergence accuracy and its required operation time.

TABLE I
COMPARISONS WITH RELATED FTL DESIGNS

	This Work	[6]	[13]*
Applications	WBAN	Senor Network	ZigBee
Technology	90nm CMOS	0.18μm CMOS	0.18μm CMOS
Active Area	0.27mm^2	1.11mm^{2****}	N/A
Conv. Scheme	CBST	IF Cancellation	IF Cancellation
FD Type	Modified FC	PFD	TDC-PFD
Err. Tolerance (ε_{Max})	3%	1.15%****	83ppm*
Conv. Accuracy (ε_O)	23.5ppm**	287ppm****	5ppm*
Conv. Time	3.06ms**	N/A	30μs*
Noise Resistibility	Yes	No	No
Sys. Throughput	4.85Mbps	1Mbps	250kbps

*: Simulation results and ignores channel noise (ideal channel). **:SNR=7dB. ***: Front-ends and VCO excluded. ****: Estimation by assuming $N_{SYN}=87$.

control bit ε_n is uncertain due to PVT variations. Therefore, the CBST scheme is applied to three DCO tuning stages (coarse, first, and second fine-tuning) sequentially and separately. Optimal T'_{ACC} for three tuning stages is obtained from (4) with $\varepsilon_{\mathrm{Stage}} = f_O \cdot$ tuning stage least significant bit delay.

Moreover, the convergence clock is applied to an orthogonal frequency-division multiplexing baseband chipset in [10] to confirm overmegabits-per-second transmissions in crystalless. For continuous 9.6 kb/s electrocardiogram signal monitoring, the system requires ±100-ppm accuracy to maintain 4.85 Mb/s data link during a burst 3.45-ms active period in every 0.84-s cycle. By measuring the slope of f_{DCO} curve related to variant voltage and temperature conditions, the slope shows the variant rate of f_{DCO} around 5 MHz is 1.16%/0.1 V and 0.07%/°C. The test chip enables our demo case under the variation rate slower than 0.25 V/s and 41.8 °C/s. Eventually, at least 79% RF front-end operation time and power is reduced [4]–[6] to improve system energy efficiency.

Table I lists the comparisons with related FTL designs. In addition, with ultralow integrated power and area, the IF-FTL, which occupied 0.5×0.55 mm^2, consumes 11.3 μW in tracking mode, and the always-on P2-DCO consumes 7.6 μW in 5 MHz. Fig. 11 shows the chip microphotograph and layout view.

V. CONCLUSION

This brief has presented an FTL to realize energy-efficient crystalless WSN integrations. By tracking a wireless reference for system clock calibration, the FTL allows WSNs to tolerate a large-frequency error from on-chip oscillators. In addition, to reduce system duty cycle in crystalless for energy saving, an accurate clock frequency is certainly required for enabling overmegabits-per-second throughput. Thus, a CBST scheme is further proposed to control FTL operations for accurate and robust convergence. As a result, a miniature WSN solution with low-power and low-cost features becomes available for WBAN applications.

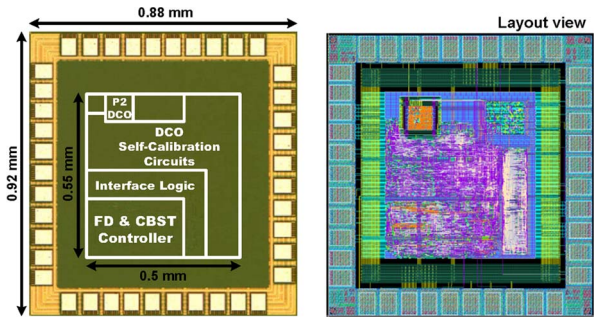

Fig. 11. Microphotograph of the test IF-FTL chip and layout view.

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