Numerical Analysis of Frequency Dispersion of Transconductance in GaAs MESFET's

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Abstract— A fully two-dimensional numerical model for the transconductance dispersion in GaAs MESFET's is presented. According to simulated results, the dominating surface traps belong to the hole trap type in order to obtain consistent results with reported measurements. The AC frequency-dependent modulation of negative surface charge can explain this anomalous phenomenon. The holes injecting from and emitting out of the gate metal electrode interact with the surface hole traps, and result in the change of the gate-to-source and the gate-to-drain resistances, which in turn cause the change in transconductance. The gate voltage and the gate length effects on the dispersion are also considered. Good agreement with reported results is obtained.

I. INTRODUCTION

IT is often observed that the small-signal extrinsic transconductance, g_m, and its phase angle in GaAs MESFET's and JFET's exhibits significant low-frequency dispersion [1]–[7]. The transconductance measured at very low frequencies (usually ≤ 10 Hz) is larger than at high frequencies (≥ 1 kHz). The phase angle also has a dip appearing around the transition frequency. The transition frequencies typically range from few 10's Hz to few 10's kHz. Moreover, different surface treatment, gate voltage, temperature, and device structures (such as gate length) also have a strong influence on this transconductance dispersion. The low frequency dispersion of g_m has a profound effect on the microwave behavior of FET-based MMIC's [8]. To understand and to control this effect is essential in obtaining reliable and controllable device performance.

It has been shown in the past, the charge exchange via surface states existing at the ungated surface region is responsible for the observed dispersion. This was first shown by Ozeki *et al.* [1] and later verified by Wallis *et al.* [4] and Blight *et al.* [5]. Up to now, there have been many reports concerned with the analytical modeling of the transconductance dispersion. Ladbrooks *et al.* [6] proposed a model based on uniform depletion at the ungated surface region due to surface states. Kachwalla [9] applied this model to study surface state energy levels. Kawasaki *et al.* [7] extended the uniform depletion assumption and used two types of fitting parameters to model the dispersion in an ion-implanted GaAs FET's. Zhao *et*

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al. [10] assumed the surface states at the ungated surface region capture electrons injected from the gate metal and presented a model which correlates the peak frequency in the transconductance dispersion spectrum and the characteristic frequency of the surface states.

There are still remaining questions not well understood. In many conductance-mode DLTS (*Deep-Level-Transient-Spectroscopy*) experiments on short-gate devices [5], DLTS spectra with signals corresponds to hole traps were observed. But the trap type, i.e., hole trap or electron trap, cannot be directly given from these measured results. Most people thought this anomalous "hole trap signal" is caused by the re-injection of electrons into surface states, since the generation of holes is not normally expected in an n-channel FET [5], [10]. So, the relationship between transconductance dispersion and hole-trap DLTS signal is not yet clarified. In this paper, we present a fully two-dimensional numerical model for the transconductance dispersion. Both the surface and the bulk traps are taken into account. The type of the surface traps and the mechanisms for the low frequency-dispersive transconductance are studied. The effect of gate voltage and gate length on transconductance dispersion are also considered.

II. PHYSICAL MODELS AND NUMERICAL METHODS

A. Device Structures

The GaAs MESFET structure used in the simulation is shown in Fig. 1. the n-type channel beneath the gate is 0.16 μm thick and is uniformly doped with a concentration of 1×10^{17} cm^{-3}. Both the source-gate and the gate-drain spacing are 1.0 μm. The gate length chosen in this calculation are 0.5, 1, 2, 3, 4 μm. The threshold voltage is about -1.0 V.

The bulk EL2 concentration $N_{TB,D}$ and the shallow-acceptor concentration N_A in the semi-insulating substrate beneath the channel layer are chosen to be 1×10^{16} and 1×10^{15} cm^{-3}, respectively. Both $N_{TB,D}$ and N_A assumed in this study are typical values found in normal undoped LEC substrates [11], [12]. The total depth simulated is 3.16 μm which is deep enough to encompass all physical phenomena. The work function difference of the gate metal-semiconductor contact is assumed to be 0.8 eV. Current transport across the Schottky-barrier junction is described by the thermionic emission-diffusion theory.

B. Surface and Bulk Trap Models

The emission and the capture of free carriers for donor-type bulk traps (EL2) in the substrate follow the Shockley-Read-
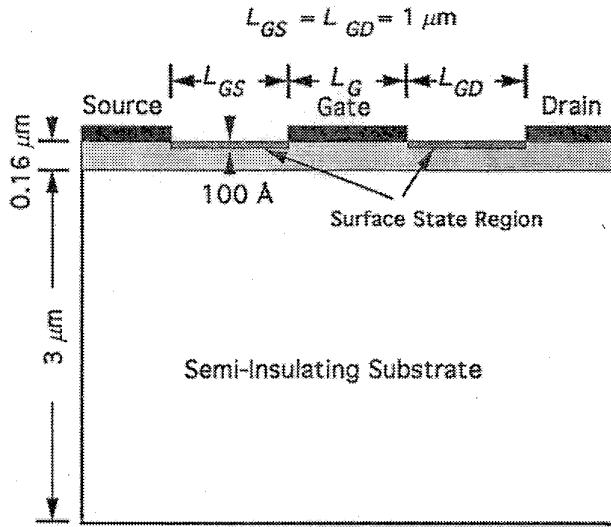
Fig. 1. A device structure used in the simulation. The surface states are uniformly distributed to a depth of 100 Å.

Hall model. The energy difference between the conduction band edge and the EL2 level, $E_{CT,B}$, is assumed to be 0.69 eV at room temperature [13]. The electron and the hole capture cross sections, $\sigma_{nB,D}$ and $\sigma_{pB,D}$, are 3.5683×10^{-15} and 1×10^{-18} cm^2, respectively [14]. The rate equation for the ionized EL2 traps can be described as

$$-\frac{\partial N_{TB,D}^+}{\partial t} = [c_{nB,D} N_{TB,D}^+ n - e_{nB,D}(N_{TB,D} - N_{TB,D}^+)]$$
$$- [c_{pB,D}(N_{TB,D} - N_{TB,D}^+)p - e_{pB,D} N_{TB,D}^+] \quad (1)$$

where $c_{nB,D}$ and $e_{nB,D}$ are the capture and the emission rates for electrons, and $c_{pB,D}$ and $e_{pB,D}$ are the capture and the emission rates for holes. The relationships between $c_{pB,D}$ and $e_{pB,D}$ and between $c_{nB,D}$ and $e_{nB,D}$ can be expressed as

$$c_{nB,D} = \sigma_{nB,D} v_{n,th}$$
$$c_{pB,D} = \sigma_{pB,D} v_{p,th}$$
$$e_{nB,D} = c_{nB,D} N_C e^{-E_{CT,B}/kT} \quad (2)$$
$$e_{pB,D} = c_{pB,D} N_V e^{-(E_G - E_{CT,B})/kT}$$

where $v_{n,th}$ and $v_{p,th}$ are the thermal velocities of electrons and holes, respectively.

The surface model used in this study was based on Spicer's unified defect model [15]. Two surface deep states were assumed in Spicer's model, i.e., a single donor-type trap, $E_{CT,S,D} = 0.925$ eV, below the conduction band edge and a single acceptor-type trap, $E_{TV,S,A} = 0.8$ eV, above the valence band edge. The energy level of donor-type surface traps is 0.301 eV below that of acceptor type surface traps. At steady state, the ionized donor-type surface charge density is less than one-tenth of occupied acceptor-type surface trap density [16]. It can be expected that the contribution of donor-type surface traps to the electrical characteristics can be negligible, so the donor-type surface traps are neglected in our calculation. For an n-type semiconductor with a doping

concentration of 1×10^{17} cm^{-3}, a surface state density of greater than 2×10^{12} cm^{-2} is required to pin the surface Fermi level at the position of the defect states [17]. Experimentally, it has been shown that the traps at and beneath the metal-semiconductor interface have little contribution to the dispersion of transconductance [4], [5]. Therefore, they are not considered in the simulation. In this study, the surface states are uniformly distributed to a depth of 100 Å from the ungated surface as shown in Fig. 1. The surface state density is 5×10^{13} cm^{-2} in the study and the calculated volume density of the surface traps is 5×10^{19} cm^{-3}. In our 2-D numerical analysis, a very small vertical grid spacing of 20 Å is used near the surface region. At thermal equilibrium, the surface Fermi level at the ungated region is calculated to be pinned by the surface states at 0.7 eV below the conduction band edge, which agrees with the measured result. The electron and the hole emission rates for surface traps, $e_{nS,A}$ and $e_{pS,A}$, are two important physical parameters determining the charge trapping and emitting rates for surface traps. From the conductance DLTS experiments on MESFET's performed by Zylbersztejn et al. [2] and Blight et al. [5], a large hole trap peak with an emission rate of several 100's s^{-1} appears around room temperature. From another conductance DLTS experiments by Harrang et al. [18], with the rate window varied from 8.656 ms to 0.4431 s, a large peak corresponding in sign to "hole-trap-like" also appears at around room temperature. Therefore, it is reasonable to assume the carrier emission rate for the dominating surface traps is 100 s^{-1}. Only by the conductance DLTS, we cannot directly judge if the dominating acceptor-type surface traps are hole traps ($e_{pS,A} > e_{nS,A}$) or electron traps ($e_{pS,A} < e_{nS,A}$). Since the type of the dominating surface traps is unknown, we consider three cases: (1) for hole trap, $e_{pS,A} = 100$ s^{-1} and $e_{nS,A} = 0.01 e_{pS,A}$, (2) for electron trap, $e_{nS,A} = 100$ s^{-1} and $e_{pS,A} = 0.01 e_{nS,A}$, and (3) no surface trap, i.e., $N_{TS} = 0$.

According to the Shockley-Read-Hall model, the rate equation for surface acceptor traps can be expressed as

$$\frac{\partial N_{TS,A}^-}{\partial t} = [c_{nS,A}(N_{TS,A} - N_{TS,A}^-)n - e_{nS,A} N_{TS,A}^-]$$
$$- [c_{pS,A} N_{TS,A}^- p - e_{pS,A}(N_{TS,A} - N_{TS,A}^-)] \quad (3)$$

where $N_{TS,A}$ and $N_{TS,A}^-$ denotes the total and the occupied acceptor-type surface state densities, respectively. The $c_{pS,A}$ and the $c_{nS,A}$, respectively, are the hole and the electron capture rates for the acceptor-type surface traps. The relationships between $c_{pS,A}$ and $e_{pS,A}$ and between $c_{nS,A}$ and $e_{nS,A}$ can be expressed as

$$c_{nS,A} = \sigma_{nS,A} v_{n,th}$$
$$c_{pS,A} = \sigma_{pS,A} v_{p,th}$$
$$e_{nS,A} = c_{nS,A} N_C e^{-(E_G - E_{TV,s,A})/kT} \quad (4)$$
$$e_{pS,A} = c_{pS,A} N_V e^{-E_{TV,s,A}/kT}.$$

For case (1), $\sigma_{pS,A} = 3.9 \times 10^{-11}$ cm^2 and $\sigma_{nS,A} = 6.4 \times 10^{-15}$ cm^2, and for case (2), $\sigma_{pS,A} = 3.9 \times 10^{-13}$ cm^2 and $\sigma_{nS,A} = 6.4 \times 10^{-13}$ cm^2.

The Poission equation is described as

$$\nabla^2\psi + \frac{q}{\varepsilon}(-n + p + N_D - N_A + N_{TB,D}^+ - N_{TS,A}^-) = 0 \quad (5)$$

where ψ, q and ε are the electrostatic potential, the electron charge and the permittivity of GaAs, respectively. The current continuity equations for electrons and holes are given by

$$\frac{1}{q}\nabla \cdot \vec{J}_n - [c_{nB,D}N_{TB,D}^+ n - e_{nB,D}(N_{TB,D} - N_{TB,D}^+)]$$

$$- [c_{nS,A}(N_{TS,A} - N_{TS,A}^-)n - e_{nS,A}N_{TS,A}^-] = \frac{\partial n}{\partial t} \quad (6)$$

$$- \frac{1}{q}\nabla \cdot \vec{J}_p - [c_{pB,D}(N_{TB,D} - N_{TB,D}^+)p - e_{pB,D}N_{TB,D}^+]$$

$$- [c_{pS,A}N_{TS,A}^- p - e_{pS,A}(N_{TS,A} - N_{TS,A}^-)] = \frac{\partial p}{\partial t} \quad (7)$$

where the low field mobility's for electrons and holes are assumed to be 5 000 and 800 cm^2/V·s, respectively.

C. Numerical Methods

For small signal simulation, a two-dimensional, two-carrier device simulation program based on the drift-diffusion formulation was developed. Before the small signal analysis, a DC solution for the coupled equations, (1)–(7), needs to be first obtained. The Newton's method is used in our calculation. Then a small-signal analysis described by S. E. Laux [19] is used to calculate the small-signal transconductance value. The AC input gate voltage and the AC solutions are expressed as $v_G e^{j\omega t}$ and $\tilde{\psi}e^{j\omega t}$, $\tilde{n}e^{j\omega t}$, $\tilde{p}e^{j\omega t}$, $\tilde{N}_{TB,D}^+ e^{j\omega t}$ and $\tilde{N}_{TS,A}^- e^{j\omega t}$, where variables with $\sim$ above are the complex AC solutions.

The small-signal extrinsic transconductance is defined as

$$\tilde{g}_m = g_m \angle\theta = \frac{\tilde{i}_D(= i_D\angle\theta)}{v_G} \quad (8)$$

where g_m and θ are the magnitude and the phase angle of the small-signal transconductance, respectively, and i_D is the AC drain current. The AC gate voltage v_G is 0.05 V in our calculation.

### III. EXPLANATION OF FREQUENCY DISPERSION

A. Trap Type Effect

For the three cases defined in Section II, the calculated small-signal transconductance and the phase angle versus frequency are shown in Fig. 2(a)–(c). The FET's gate length is 1 μm, the surface state density is 5×10^{13} cm^{-2} and the DC drain and the DC gate voltages are 0.1 V and 0 V, respectively. For the hole trap case, as shown in Fig. 2(a), the transconductance at low frequencies is larger than at high frequencies. The transition frequency is around 10 Hz. The percentage shift of g_m, which is defined as $(g_m(0) - g_m(f))/g_m(0)$, is about 15.6%. A maximum dip of phase angle θ, which is about $-4.2°$, is found also at about 10 Hz. This result agrees with all the reported experimental results. But for the electron trap case, as shown in Fig. 2(b), the simulated frequency dispersions are just opposite to the reported experimental results: the transconductance is larger

rather than smaller at high frequencies and a maximum positive θ rather than negative θ appears at the transition frequency. For the case without surface trap, as shown in Fig. 2(c), no transconductance dispersion and phase angle dip are found. Since the bulk EL2 traps are included in all our calculations, this result indicates that the bulk traps beneath the channel region are not responsible for the transconductance dispersion.

Because the simulated results for the case with surface electron traps are opposite to the measured results, our simulation excludes any close relationship between the surface electron traps and the common observed transconductance dispersion. If the dominating surface traps are hole traps, consistent results with experiments are obtained. Therefore, Our simulation supports that the type of the dominating surface traps are hole trap, i.e., $e_{pS}, A > e_{nS}, A$. Because the holes in an n-channel MESFET are minority carriers, the origin of these holes which interact with surface hole traps still remains to be a question and we discuss it later.

After identifying the trap type of dominating surface states, the following studies are concentrated on the hole trap case. To see the frequency response of surface traps to the AC gate voltage, the AC negative surface trap density and the AC surface potential along the ungated surface region are plotted in Fig. 3(a) and (b), respectively. The calculated frequencies are 0.1 Hz, 10 Hz and 10 kHz. As shown in Fig. 3(a), the AC modulation of $N_{TS,A}^-$ appears in the region near the gate edge and gradually decays toward the source edge. The AC magnitude of negative surface trap densities decreases with increasing frequency. The real part of AC negative surface charge density, $\text{Re}(\tilde{N}_{TS,A}^-)$, is negative, which means the negative surface trap density decreases at positive cycle of AC gate voltage. As shown in Fig. 3(b), the real part of AC surface potential, $\text{Re}(\tilde{\psi})$, is positive and the modulation of surface potential increases with decreasing frequency due to the decrease of $N_{TS,A}^-$ at low frequencies (shown in Fig. 3(a)). It is noted that the imaginary parts of $\tilde{N}_{TS,A}^-$ and $\tilde{\psi}$ are near zero at 0.1 Hz and 10 kHz but significant at 10 Hz, which corresponds to the dip in phase angle at $f = 10$ Hz (see Fig. 2(a)). From Fig. 3(a) and (b), both the profiles of $\tilde{N}_{TS,A}^-$ and $\tilde{\psi}$ are functions of the distance from the gate edge indicating the surface depletion is not uniform, which is different from the assumption of uniform depletion used by other authors.

It can be expected that the channel depletion due to the modulation of surface negative potential will be quite different. Fig. 4(a) and (b) show the three dimensional plots for the real part of AC free electron concentration at $f = 0.1$ Hz and $f = 10$ kHz, respectively. At both frequencies, the imaginary part of the AC free electron concentration, $\text{Im}(\tilde{n})$, is less than one-tenth of the real part, $\text{Re}(\tilde{n})$, so $\text{Im}(\tilde{n})$ is negligible. As shown in Fig. 4(a) and (b), $\text{Re}(\tilde{n})$ under the gate electrode and at the ungated region is positive, which means the electron concentration increases during the positive cycle of AC gate voltage. Comparing Fig. 4(a) with (b), we can find that the modulated length of ungated surface region due to AC gate voltage is longer at low frequency. It implies that the gate-to-source resistance is frequency-dependent and smaller at lower frequencies. That can be explained by the
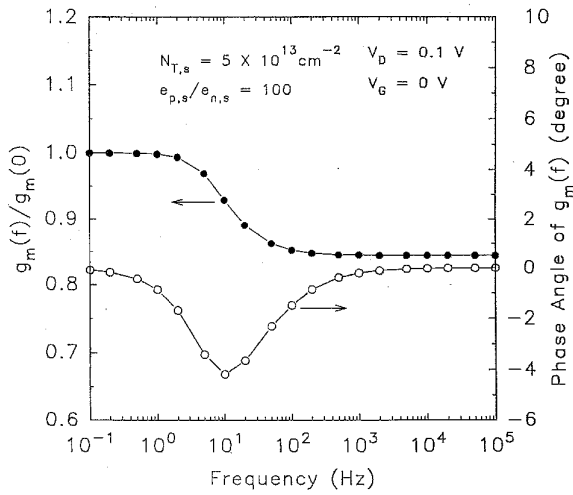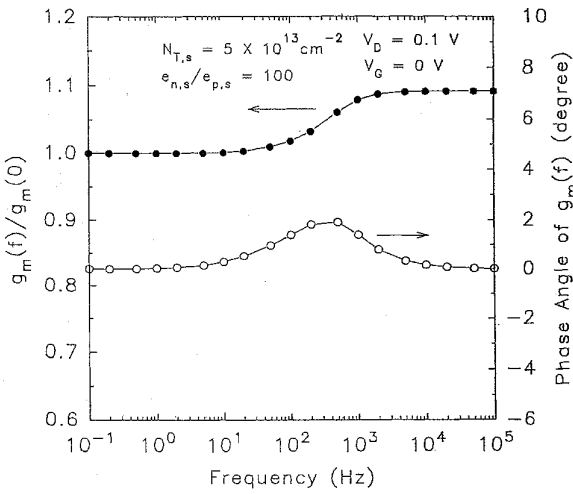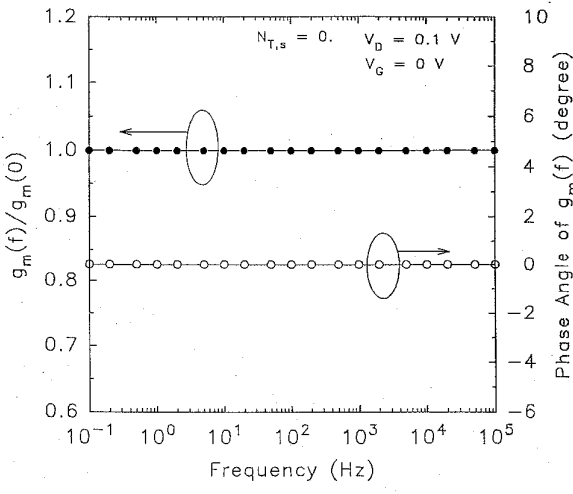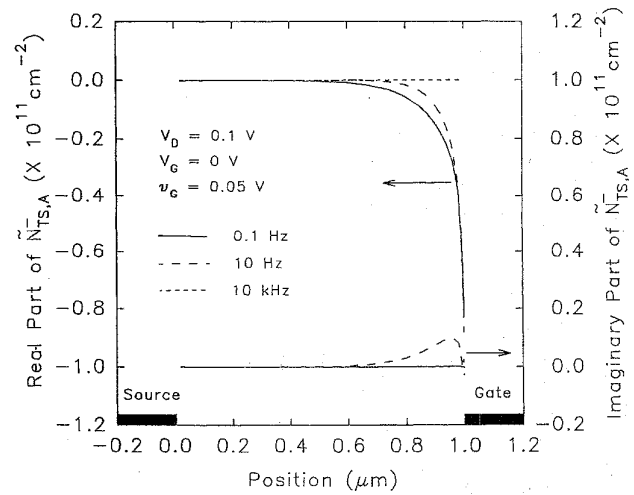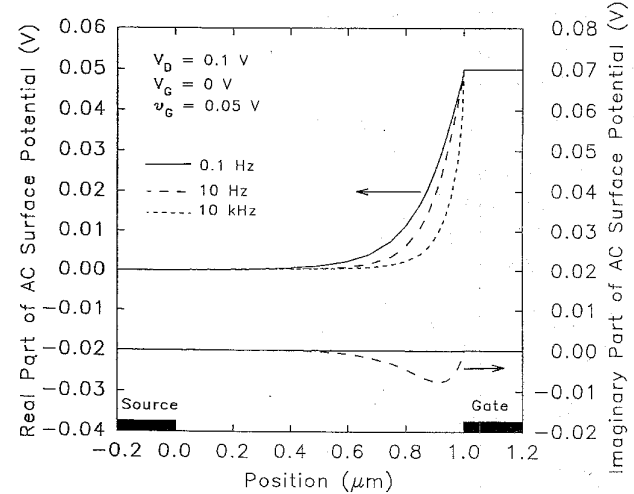
Fig. 2.   Calculated transconductance dispersion versus frequency for (a) the hole trap case, $e_{pS}/e_{nS} = 100$, (b) the electron trapcase, $e_{nS}/e_{pS} = 100$ and (c) no surface trap.

Fig. 3.   Profiles for (a) the AC negative surface trap density, and (b) the AC surface potential along the ungated surface region. The frequencies are 0.1 Hz, 10 Hz and 10 kHz.

frequency-dependent surface potential near the gate edge. At low frequencies, the length of modulated surface region is longer and during the positive cycle of AC gate voltage, the AC positive potential become larger (see Fig. 3(a) and (b)). Therefore, the channel depletion width due to negative surface potential is smaller, i.e., the parasitic source-to-gate resistance is smaller. Moreover, it is expected the gate-to-drain resistance is also smaller at low frequencies as the gate-to-source resistance. So, the extrinsic transconductance is larger at low frequencies due to the two smaller parasitic resistance's.

B. Origin of Carriers Interacting with Surface States

To clarify the origin of the carriers interacting with the surface hole traps, the AC amplitudes and the phase angles of the electron and hole currents flowing into gate electrode are shown in Fig. 5. The AC electron gate current, $\tilde{I}_{Gn}$, is negligible compared to that of AC hole current and its phase
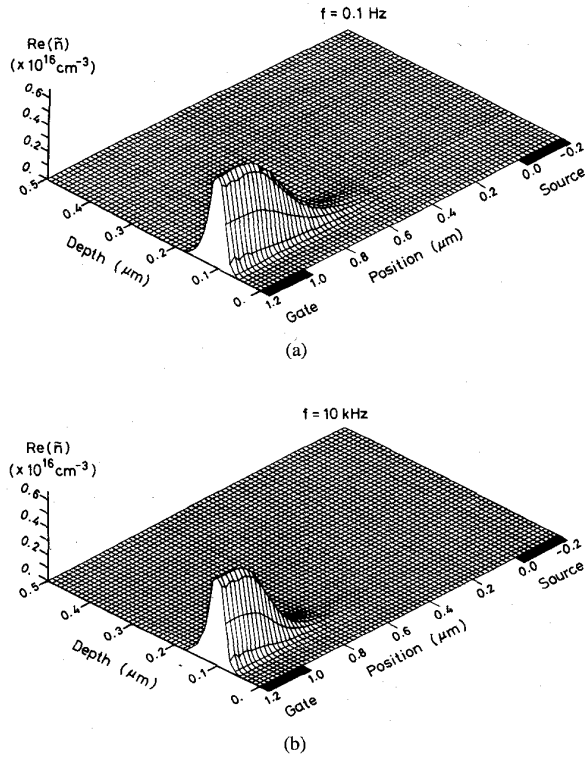
Fig. 4. Three dimensional plots for the real part of AC free electron concentration at (a) $f = 0.1$ Hz, and (b) $f = 10$ kHz.

Fig. 5. Calculated AC amplitudes and phase angles of hole and electron gate currents flowing into the gate electrode.

angle is near zero from $f = 0.1$ Hz to $f = 100$ kHz. For the AC hole gate current, $\tilde{I}_{Gp}$, its magnitude increases very slightly before 5 Hz but undergoes a drastic increase between 5 Hz and 1 kHz. After that it saturates at its maximum value at 1 kHz. A dip of phase angle also appears at about 10 Hz. Compared to the other components of the gate conductance, the real part of the AC hole gate current dominates for the frequency range of 0.1 Hz to 100 kHz. In other words, the gate conductance also increases with frequency, which agrees with the measured results of Ozeki et al. [1] and Zylbersztejn [20]. This anomalous frequency dispersion of $\tilde{I}_{Gp}$ just corresponds to the transconductance dispersion shown in Fig. 2(a). Because of the large recombination rate through the high-density surface states at the ungated surface region, a lot of holes can flow into the surface region by thermionic-emssion-diffussion transport and be captured there, causing the large AC hole gate current. The AC hole gate current increases about one order when the frequency increases from 0.1 Hz to 0.1 MHz.

The frequency dependence of the AC surface charge density and surface potential near the gate edge can be well explained by the slow trapping behavior of the surface states and the hole leakage current through the gate electrode. The physical mechanisms during the positive and the negative cycles of AC gate voltage swing, such as the sign of AC hole current and the interaction processes between holes and traps, are opposite to each other. Here only the positive cycle is discussed. The holes are injected from the gate electrode by thermionic-emssion-diffusion transport. The source and the drain hole currents
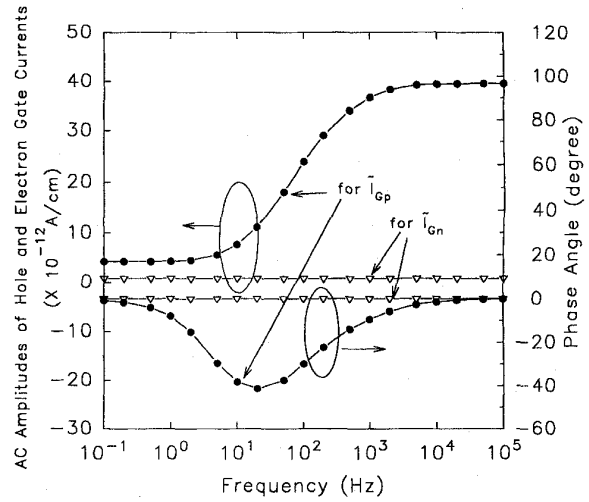
from $f = 0.1$ Hz to $f = 100$ kHz have been calculated, and found to be negligible compared to the gate hole current. Therefore, the injected holes are unable to reach the source contact. They are captured by the surface traps at the ungated region near the gate edge. At low frequencies, the trapping behavior of the surface states can follow the slow AC voltage swing. Consequently the negative surface charge densities are effectively reduced (see Fig. 3(a) for $f = 0.1$ Hz), causing the AC surface potential to be higher and the AC electric field parallel to the ungated surface to be lower (see Fig. 3(b) for $f = 0.1$ Hz). At high frequencies, the trapping behavior of the surface states cannot follow the fast AC voltage swing and consequently the negative surface charge densities are less modulated. Therefore, the AC surface potential at the ungated surface is lower and the AC parallel electrical field is larger (see Fig. 3(b) for $f = 100$ kHz). The increase of the AC electrical field near the gate edge at high frequencies explains why the AC gate hole current increases with the frequencies (see Fig. 5). The number of injected holes through the gate is approximately proportional to the product of the AC hole gate current and the period time of the AC gate voltage swing, i.e., $\tilde{I}_{Gp} \times 1/f$. Because $\tilde{I}_{Gp}$ increases slowly with the frequency (see Fig. 5, for six orders of magnitude increase in frequency there is only 10 times increase in $\tilde{I}_{Gp}$), the number of injected holes through the gate is approximately inversely proportional to the frequency. At high frequencies, less holes are injected and captured by the surface traps at the ungated surface near the gate edge. Therefore, the modulation of the surface potential is negligibly affected by the injected holes.

IV. GATE BIAS AND GATE LENGTH EFFECTS

Experimentally, the magnitude of the transconductance dispersion in MESFET's and JFET's strongly depends on DC gate bias and gate length [4], [5], [7]. To confirm the validity of our numerical model, we also apply our model to study the transconductance dispersion with different DC gate biases and gate length. The transconductance versus the DC gate
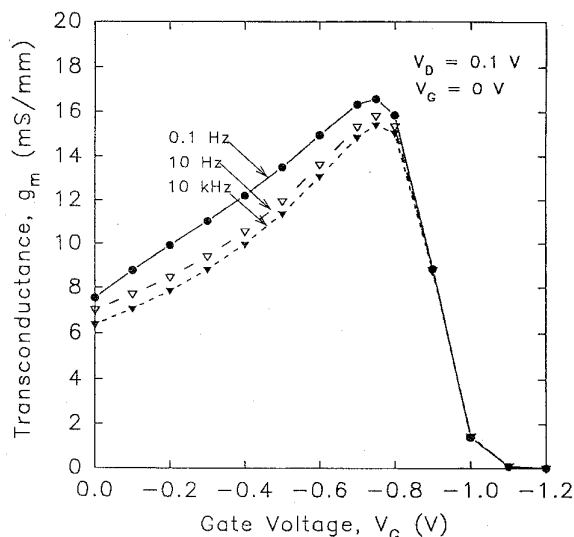
Fig. 6. Calculated normalized shift of transconductance versus gate voltage as a function of frequency. The frequencies are 0.1 Hz, 10 Hz and 10 kHz.

Fig. 7. Calculated normalized shift of transconductance versus gate length. Both the gate-to-source and the gate-to-drain distances are 1 μm.

voltage at $f = 0.1$ Hz, 10 Hz and 10 kHz is shown in Fig. 6. Evidently, the dispersion is noticeable near $V_{GS} = 0$ V and negligible near pinch off ($\cong -1$ V). Our results agree with Wallis's [4] and Blight's [5]. At pinch-off, the channel beneath the gate is almost depleted, so the channel width can not be effectively modulated by the AC gate voltage and the transconductance is very small. Although the two parasitic resistances at the ungated region are frequency-dependent, they cannot cause any significant transconductance dispersion.

Fig. 7 shows the g_m dispersion versus gate length. The L_{GS} and the L_{GD} are 1 μm for all calculation. The normalized shift of transconductance decreases monotonically with an increase in the gate length. Our calculated results agree with Wallis's [4] and Kawasaki's [7]. This dependence of g_m on gate length can be explained by the ratio of the modulated length of surface region (see Fig. 3(a) and (b)) to the gate length. As the gate length increases, the ratio becomes smaller, so the modulation of surface charge has less influence on the transconductance.

V. CONCLUSION

The frequency dispersion of the small-signal transconductance for GaAs MESFET's is analyzed using 2-D numerical simulation. It is confirmed that the bulk traps beneath the n channel are not responsible for the dispersion. The surface traps at the ungated surface are the cause of this phenomenon. We have also found that the dominating surface traps are hole traps. The calculated results agree with experimental findings which show higher transconductances at lower frequencies and a dip in the phase angle at the transition frequency. This result can be explained by the frequency-dependent modulation of the gate-to-source and the gate-to-drain resistances caused by the slow behavior of the charge exchange via the surface states at the ungated surface region near the gate edge. At positive cycle of AC gate voltage, holes can inject into the
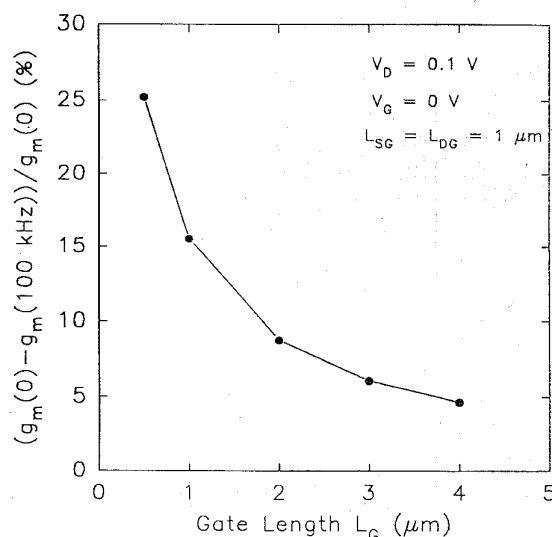
surface region from the gate electrode by thermionic-diffusion-emission transport. Due to frequency-dependent potential at the ungated region near the gate edge, the AC hole gate current also exhibits frequency dispersion behavior corresponding to the transconductance dispersion. Gate bias and gate length effects on the transconductance dispersion are also considered. Agreement with reported measurements is obtained.

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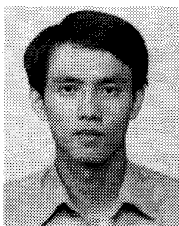
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