# A New Quantitative Model for Weak Inversion Charge Injection in MOSFET Analog Switches

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*Abstract*— **This paper proposes a new model concerning the channel charges in weak inversion injected from a turn-off MOSFET into a holding capacitor. This portion of charge injection has recently been newly observed, showing a significant contribution to the switch-induced error voltage on the switched capacitor. Our model is derived at the critical point where the device is operated in the transition region between strong inversion and weak inversion. This point has been expressed explicitly as a function of the DC input voltage, the threshold voltage, and the fall time of the gate voltage. The ability of the model in accurately determining quantitatively the impact of the weak inversion charge injection on the error voltage has been extensively judged experimentally and by two-dimensional mixed-mode simulation for a wide variety of design parameters such as the channel width and length, the holding capacitance, the fall time of the gate voltage, and the DC input voltage. The assumptions utilized in the model development have also been validated.**

## I. Introduction

A typical analog MOS switch comprises an n-channel MOSFET and a holding capacitor (see Fig. 1 for the circuit configuration and the associated waveforms when operating this switch). This switch is one of the major building blocks for the switched-capacitor circuits [1]. One of the fundamental factors that limit the accuracy of the switched-capacitor circuits is the charge injection occurring when the MOSFET turns off [2]. Analysis and modeling of charge injection due to channel charges in strong inversion and feedthrough charges through the gate-to-diffusion overlap capacitance have been well established [3]–[7]. Our recent work [8], [9] has further separated the charge injection into three distinct components: (i) the channel charges in strong inversion $Q_a$; (ii) the channel charges in weak inversion $Q_b$; and (iii) the charges coupled through the gate-to-diffusion overlap capacitance $Q_c$. These charges injected into the switched capacitor $C_H$ cause a nonzero error voltage $\Delta V_{OUT}$, which can be expressed as $\Delta V_{OUT} = (Q_a + Q_b + Q_c)/C_H$. Although two-dimensional device and mixed-mode simulations have successfully reproduced both the measured error voltage and the experimental waveforms [8], [9], a model with the ability of accurately calculating the error voltage due to these charges injected is desirable. It has been proved experimentally [8], [9] that the analytical model cited in [3] can provide such ability with respect to the two components $Q_a$ and $Q_c$. However, a quantitative model for the weak inversion charge injection component $Q_b$ has not previously been published. It is noted [8], [9] that this newly observed component can contribute comparably to the switch-induced error voltage and thus neglecting this component can seriously underestimate the correct value of the error voltage.

In this paper we will propose a new model for the error voltage arising from the channel charges in weak inversion. This model can quantitatively provide information about the dependencies of the weak inversion charge injection induced error voltage on the design parameters such as the channel width and length, the holding capacitance, the fall time of the gate voltage, and the DC input voltage. The validity of both the model itself and the assumptions in the model development will be addressed in detail in a given CMOS process, by comparing both the experimental results and the two-dimensional device and mixed-mode simulations.

## II. Model Development

According to the work [8], [9], some important observations of the charge injection in a MOS switch can be drawn from the waveform of the current $I_D(t)$ through the switched capacitor as depicted in Fig. 1. In Fig. 1 the area under the curve of the current $I_D(t)$ in the turn-off transition of $t_1 < t < t_3 (= t_1 + t_f)$ can be separated into three different components $Q_a$, $Q_b$, and $Q_c$, where $Q_a$ represents part of the channel charges in strong inversion for $t_1 < t < t_2$; $Q_b$ represents the channel charges in weak inversion for $t_2 < t < t_3$; and $Q_c$ represents the charges coupled through the gate-to-diffusion overlap capacitance for $t_2 < t < t_3$ . Here $t_1$ is the time for the gate voltage $V_G(t)$ starting to drop; $t_2$ represents the time for the gate voltage reaching the sum of the input voltage $V_{in}$ and threshold voltage $V_{th}$; and $t_f$ is the fall time of the gate voltage.

Here a ramp type waveform is assumed for the gate voltage in the turn-off transition, i.e. $V_G(t) = V_H - (V_H - V_L)(t - t_1)/t_f$ for $t_1 \leq t \leq t_3$, where $V_H$ and $V_L$ are the high and low level values of the gate voltage, respectively. In this situation, Sheu and Hu [3] have published an analytical model for two components $Q_a$ and $Q_c$:

$$Q_a = \sqrt{\frac{\pi(V_H - V_L)C_H}{2t_f\beta}}(C_{GD} + \frac{1}{2}C_{ox}) \cdot \mathrm{erf}(\sqrt{\frac{t_f\beta}{2(V_H - V_L)C_H}}(V_H - V_{in} - V_{th})) \quad (1)$$

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and

$$Q_c = C_{GD}\,(V_{in} + V_{th} - V_L) \tag{2}$$

where $C_{ox}(= WL\epsilon_{ox}/t_{ox})$ is the gate capacitance excluding the overlap portion; $C_{GD}(= WL_D\epsilon_{ox}/t_{ox})$ is the gate-to-diffusion overlap capacitance; $\beta = W\mu\epsilon_{ox}/Lt_{ox}$; $t_{ox}$ is the gate oxide thickness; $\epsilon_{ox}$ is the oxide permittivity; $\mu$ is the carrier mobility; $L_D$ is the lateral diffusion distance; and W/L is the channel width to length ratio. In our work the gate width $W_G$ is equal to W and the gate length $L_G = L + 2L_D$. The threshold voltage $V_{th}$ considering the back-gate bias effect can be written as [10]

$$V_{th} = V_{FB} + \frac{2kT}{q}\ln\frac{N_A}{n_i} + \frac{t_{ox}}{\epsilon_{ox}}\sqrt{2q\epsilon_{si}N_A}\sqrt{\frac{2kT}{q}\ln\frac{N_A}{n_i} + V_{in}} \tag{3}$$

where $V_{FB}$ is the flat-band voltage; $N_A$ is the effective doping concentration in the channel; $n_i$ is the intrinsic concentration; $\epsilon_{si}$ is the silicon permittivity; and $kT/q$ is the thermal voltage. The critical point $t_2$ can be written explicitly as

$$t_2 = t_1 + t_f(V_H - V_{in} - V_{th})/(V_H - V_L) \tag{4}$$

which satisfies the condition of $V_G(t_2) = V_{in} + V_{th}$. Now we demonstrate how to develop a quantitative model for the newly observed component $Q_b$. First we assume that the amount of the channel charges responsible can be evaluated singly at the point $t_2$ where the device is operated in the transition region between strong inversion and weak inversion. After $t_2$ these charges will all flow to the drain, constituting the current $I_D$ that decays with the time as shown in Fig. 1. In addition, to ensure that (1) and (2) can be employed accordingly, our new model should maintain necessary compatibility with the mathematical process used in [3] for deriving (1) and (2), i.e. (1) was achieved by making the channel conduction current zero at $t_2$; and a zero channel conduction current at $t_2$ was used as an initial condition for (2), both indicating that at $t_2$ the electron quasi-Fermi level is a constant from source to drain. Thus we write the electron quasi-Fermi level $\phi_{fn}$ along the surface beneath the gate as

$$\phi_{fn} = \phi_{fp} + V_{in} \tag{5}$$

where $\phi_{fp}(= \frac{kT}{q}\ln\frac{N_A}{n_i})$ is the hole quasi-Fermi level in the neutral p-type substrate. Further we assume that the depletion region beneath the gate can be separated into three distinct sub-regions: the gate modulation, the drain depletion, and the source depletion, as schematically plotted in Fig. 2. It is intuitively assumed that the source and drain depletion regions are essentially symmetrical toward the mid-channel since the source and drain voltages are nearly identical to each other, indicating that the channel charges flow equally to source and drain. Thus the component $Q_b$ can be determined by integrating the channel charges from the mid-channel to the drain edge. According to the above assumptions, the component $Q_b$ can be written as

$$Q_b = W\int_0^{\frac{L}{2}} Q_I\,dx \tag{6}$$

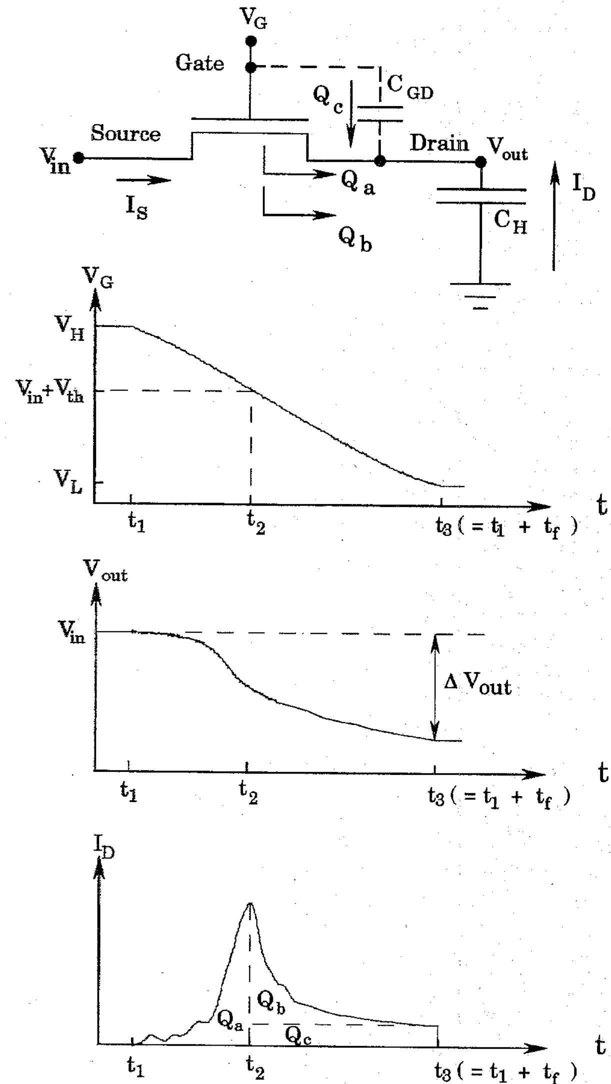



Fig. 1. The schematic MOS analog switch under study. Also shown are the waveforms of the voltages at the gate and the output as well as the current $I_D$ through the switched holding capacitor $C_H$. $C_{GD}$ is the gate-to-drain overlap capacitance. The error voltage $\Delta V_{out}$ is caused by three components $Q_a$, $Q_b$, and $Q_c$, which are defined in the text.

where the channel charge density $Q_I$ can be expressed as a function of the surface potential $\phi_s$, the hole quasi-Fermi level $\phi_{fp}$, and the electron quasi-Fermi level $\phi_{fn}$ [10]

$$\begin{aligned} Q_I &= \sqrt{2q\epsilon_{si}N_A} \cdot \left(\sqrt{\phi_s + \frac{kT}{q}exp[\frac{q(\phi_s - \phi_{fn} - \phi_{fp})}{kT}]} - \sqrt{\phi_s}\right) \\ &= \sqrt{2q\epsilon_{si}N_A} \cdot \left(\sqrt{\phi_s + \frac{kT}{q}exp[\frac{q(\phi_s - V_{in})}{kT} - 2\ln\frac{N_A}{n_i}]} - \sqrt{\phi_s}\right). \end{aligned} \tag{7}$$

As mentioned above, the depletion region of interest can be separated into two distinct ones: the gate modulation for $0 \le x \le L/2 - \Delta L$ and the drain depletion for $L/2 - \Delta L \le$

$x \leq L/2$. In the gate modulation region the surface potential is a constant $\phi_{so}$, which can be expressed as [10]

$$\begin{aligned}\phi_{so} &= V_G - V_{FB} - ((\frac{t_{ox}}{\epsilon_{ox}})\sqrt{2q\epsilon_{si}N_A}) \\ &\quad \cdot (\sqrt{\phi_{so} + \frac{kT}{q}exp[\frac{q(\phi_{so} - \phi_{fn} - \phi_{fp})}{kT}]}) \\ &= V_{in} + V_{th} - V_{FB} - ((\frac{t_{ox}}{\epsilon_{ox}})\sqrt{2q\epsilon_{si}N_A}) \\ &\quad \cdot (\sqrt{\phi_{so} + \frac{kT}{q}exp[\frac{q(\phi_{so} - V_{in})}{kT} - 2\ln\frac{N_A}{n_i}]}) \quad (8)\end{aligned}$$

for $V_G = V_{in} + V_{th}$ at $t_2$. Note that both (7) and (8) deal with the transition region between strong inversion and weak inversion. (8) can easily be solved iteratively for $\phi_{so}$ as given the values of the process parameters such as $V_{FB}$, $N_A$, and $t_{ox}$, and the circuit parameters such as $V_{in}$. In our work the abrupt junction depletion approximation is applied to the drain depletion region. Consequently, the surface potential distribution between mid-channel and drain edge can be written as

$$\phi_s = \begin{cases} \phi_{so} & , 0 \leq x \leq \frac{L}{2} - \Delta L \\ \phi_{so} + \frac{qN_A}{2\epsilon_{si}}(x - \frac{L}{2} + \Delta L)^2, & \frac{L}{2} - \Delta L \leq x \leq \frac{L}{2}. \end{cases} \quad (9)$$

Since the drain potential is the sum of the $V_{in}$ and the built-in potential $V_{bi}$ and the surface potential in the gate modulation region is a constant $\phi_{so}$, according to the abrupt depletion approximation the drain surface depletion length $\Delta L$ can be expressed as

$$\Delta L = \sqrt{\frac{2\epsilon_{si}}{qN_A}(V_{in} + V_{bi} - \phi_{so})}. \quad (10)$$

Equation (9) ensures that the potential is continuous and differentially continuous at $x = L/2 - \Delta L$. According to (9), (6) can be rewritten as

$$\begin{aligned}Q_b &= W\frac{Q_I(\phi_{so})L}{2} \\ &\quad + W(\int_{\frac{L}{2}-\Delta L}^{\frac{L}{2}} Q_I(\phi_s)dx - Q_I(\phi_{so})\Delta L). \quad (11)\end{aligned}$$

Apparently, we have achieved a new quantitative model for $Q_b$ expressed as a function of the design parameters of interest, i.e. the channel width and length and the DC input voltage in a given CMOS process. From (11) we can observe that the $Q_b$ can be separated into two distinct components: one depends on the channel length and the other is independent of the channel length. It can also been noticed that not only the fall time of the gate voltage but also the holding capacitance are not included in (11).

## III. Experiment and Mixed-Mode Simulation

Based on test chip and two-dimensional device and mixed-mode simulations, here we give evidence to support the assumptions in the above model development. The experimental MOSFET analog switch chip, fabricated by existing standard CMOS process, includes three different gate lengths of 2, 4, and 5 $\mu$m each with the same gate width of 25 $\mu$m for a holding capacitance fixed at 1.0 pF. These values are typically encountered in the present analog circuit design in order to avoid the mismatch due to process variations. The complete chip layout and on-chip measurement circuit have been described in detail in [9]. The test chip has been mounted on a plastic 24-pin package, which has been inserted into the printed-circuit board specially designed for suppression of oscillation and noise interference. The measurement conditions are: $V_H = 5$ V; $V_L = 0$ V; $t_f$ ranging from 50 ns to 5 $\mu$s; and $V_{in}$ from 1 V to 2 V. Simultaneously, the two-dimensional device and mixed-mode simulations by utilizing the program MEDICI [11] have been performed and have appropriately reproduced both the experimental waveform of the current through the switched capacitor and the measured switch-induced error voltage. Here we present the experimental and simulated waveforms of both the output voltage and the current through the switched capacitor in Fig. 3 for $L_G = 5$ $\mu$m at two different $V_{in}$ values of 1 and 2 V and two different $t_f$ values of 500 ns and 5 $\mu$s. From Fig. 3 we can observe that the simulated voltage and current waveforms match quite closely the measured ones. Note that some deviations appear near the end of the turn-off transition in Fig. 3 due to the transmission line effect in the measurement, which makes the practical waveform of the $V_G(t)$ slightly different from the ideal one (not shown here). This effect was not included in our simulation work. In Fig. 3 the current waveform at $t_f = 500$ ns seems to be different from that at $t_f = 5$ $\mu$s due to different scales for current and time; however, further observation can show that the area dominated by the $Q_b$ is almost the same for two different fall times.

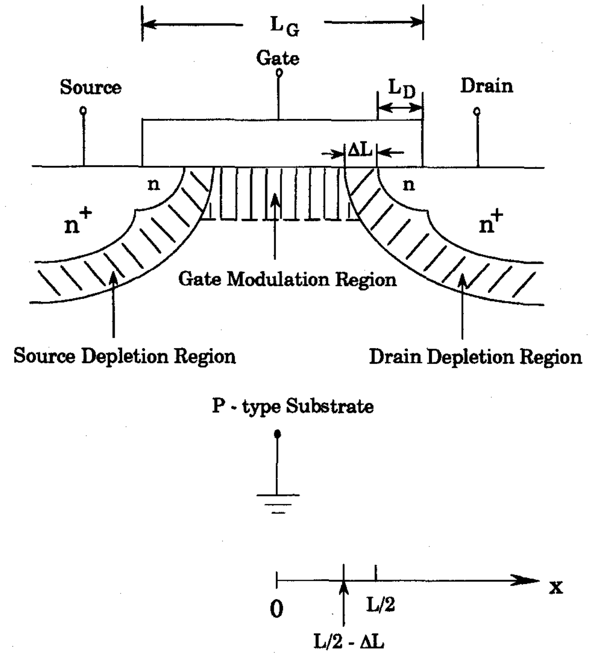



Fig. 2. The cross section of the MOSFET in weak inversion with the depletion region schematically separated into three different sub-regions.

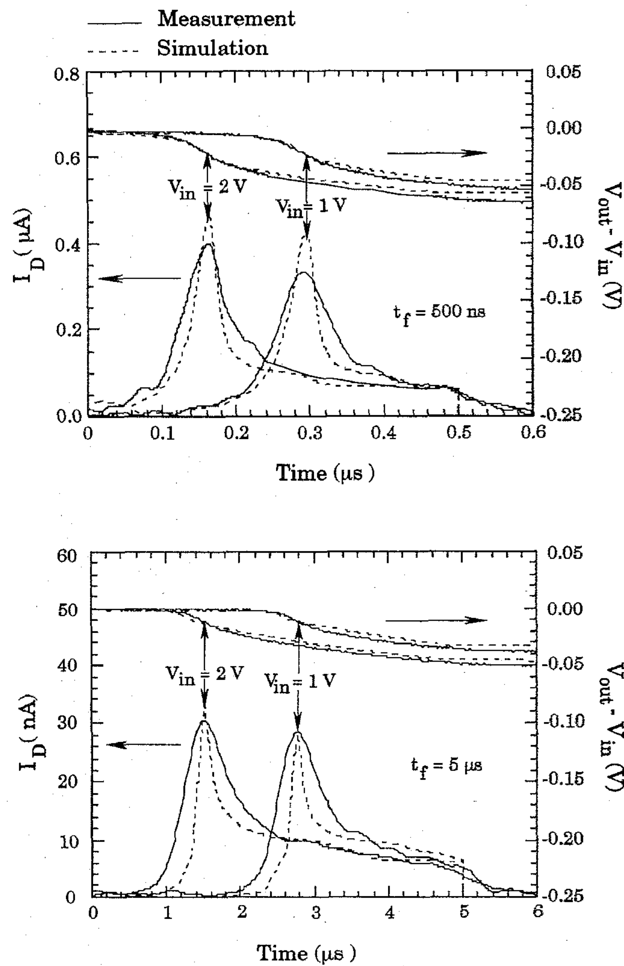
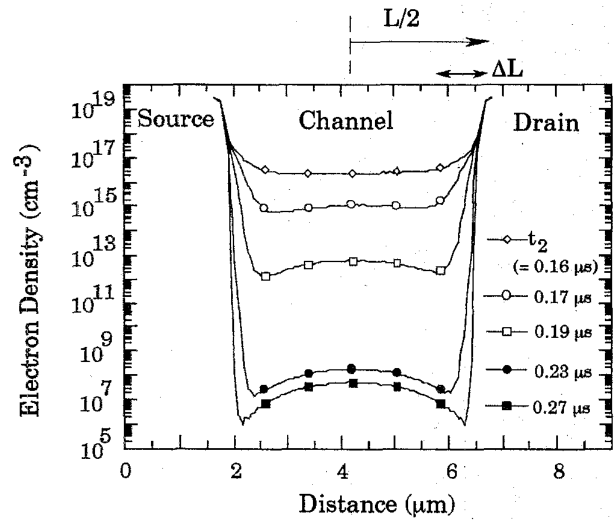
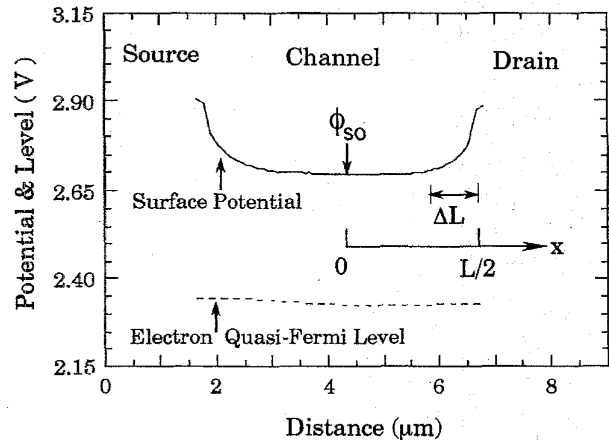



Fig. 3. The comparison of the measured and simulated waveforms at $V_{in}$ = 1 V and 2 V for two different fall times of 500 ns and 5 $\mu$s. $L_G$ = 5 $\mu$m and $t_1$ = 0.




(a)




(b)

Fig. 4. (a) The simulated surface electron density distribution as function of the time after $t_2$ and (b) the simulated surface potential and electron quasi-Fermi level distributions at $t_2$, all corresponding to the drain current waveform in Fig. 3 for $V_{in}$ = 2 V and $t_f$ = 500 ns. The drain depletion length $\Delta L$ is also shown.

From the calibrated two-dimensional device and mixed-mode simulations, the internal behavior can properly be drawn to judge the above assumptions. Fig. 4 demonstrates one example corresponding to the simulated current waveform in Fig. 3 for $V_{in}$ = 2 V and $t_f$ = 500 ns. Fig. 4(a) shows the surface electron density distribution from source to drain for 5 different time points after $t_2$; and Fig. 4(b) shows the surface potential and surface electron quasi-Fermi level distributions at $t_2$. From Fig. 4(a) we can observe that after $t_2$ the channel charges drop with the time until the channel beneath the gate is fully depleted of mobile carriers. Each of the surface electron density distributions are symmetrical toward the mid-channel, in agreement with that assumed in the model development process. The surface potential distribution at $t_2$ in Fig. 4(b) also exhibits such symmetrical property. Particularly in Fig. 4(b) it can be clearly seen that for $0 \leq x \leq L/2 - \Delta L$ the surface potential is a constant and there exists locally a small region $\Delta L$ where the dependence of the surface potential on the position follows the abrupt junction depletion approximation. Therefore, the surface potential distribution at $t_2$ can be properly modeled by (9). Moreover, from Fig. 4(b) we can observe that the electron quasi-Fermi level along the surface is nearly unchanged from source to drain, in agreement with (5).

Finally, we give additional evidence to validate the first assumption: the channel charges responsible can be evaluated singly at $t_2$. This is achieved by addressing two plausible current sources: the current directly flowing from source to drain and the current due to the channel electrons recombined with the holes from the substrate. The first source is negligible because the potential minimum is located in the channel as shown in Fig. 4(b). In fact, for t $\geq$ $t_2$ the drain current is nearly identical to the source current (with the direction defined in Fig. 1), as plotted in Fig. 5. On the other hand, the second source is about several orders of magnitude smaller than the drain current. For example, in Fig. 5 the simulated

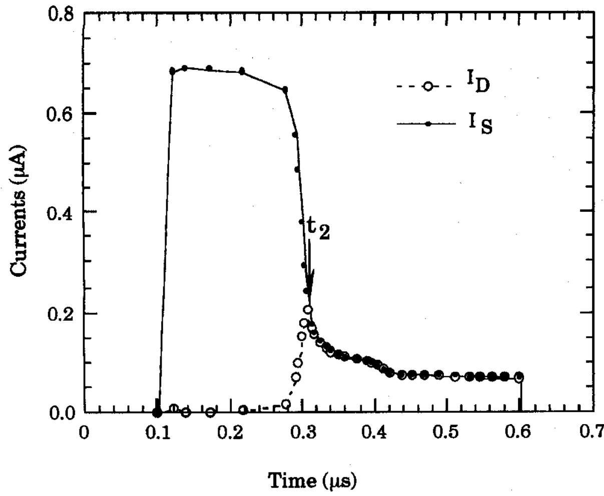



Fig. 5. The simulated waveforms of the drain and source currents in the turn-off duration. $V_{in} = 2$ V; $L_G = 2$ μm; $t_1 = 100$ ns; and $t_f = 500$ ns.

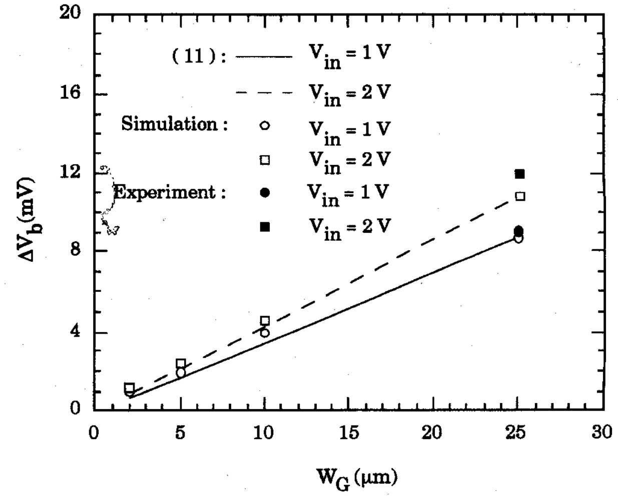



Fig. 7. The comparison of the measured, simulated, and calculated error voltage due to weak inversion charge injection versus the gate width for two different input voltage values. $L_G = 5$ μm; $C_H = 1$ pF; and $t_f = 500$ ns.

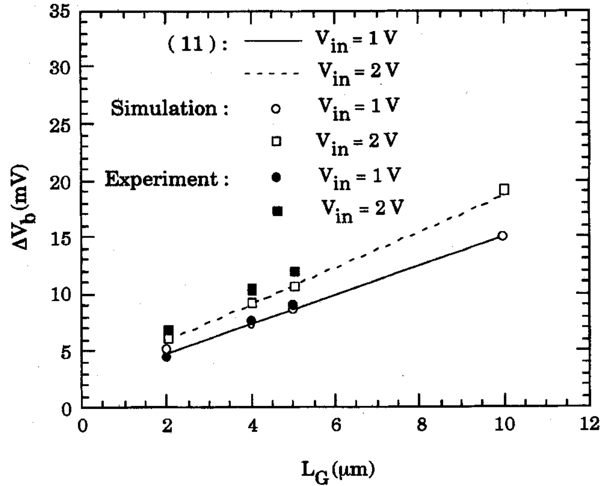



Fig. 6. The comparison of the measured, simulated, and calculated error voltage due to weak inversion charge injection versus the gate length for two different input voltage values. $W_G = 25$ μm; $C_H = 1$ pF; and $t_f = 500$ ns.

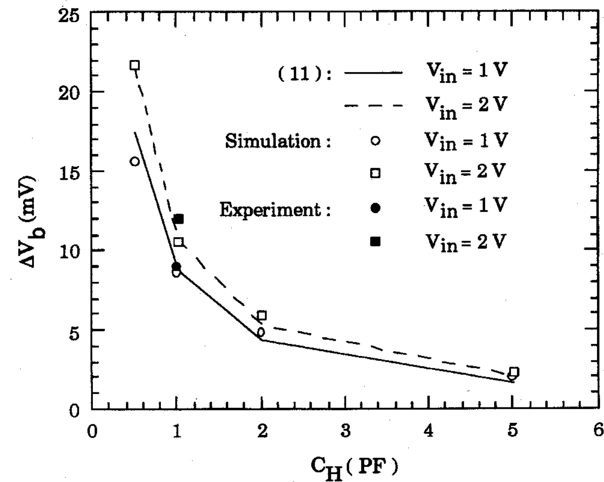



Fig. 8. The comparison of the measured, simulated, and calculated error voltage due to weak inversion charge injection versus the holding capacitance for two different input voltage values. $L_G = 5$ μm; $W_G = 25$ μm; and $t_f = 500$ ns.

recombination current has an extremely small value of about 0.1 nA.

## IV. The Impact

Here the impact of channel charges in weak inversion on the switch-induced error voltage will be addressed for a wide variety of the channel width and length, the holding capacitance, the fall time, and the input voltage. This has been achieved by employing the new model established above along with the experimental data and the two-dimensional device and mixed-mode simulations for comparison. The process parameters available from the foundry are: $t_{ox} = 250$ Å, $C_{GD} = 7.76$ fF, $N_A = 1.0 \times 10^{16} cm^{-3}$, and $V_{FB} = -0.5$ V. By substituting these values into the model, the error voltage singly due to weak inversion charge injection $\Delta V_b (= Q_b/C_H$ for $C_H = 1.0$ pF) has been calculated and has been found to be in excellent agreement with the experimental and simulated values. Figs. 6–9 show the calculated $\Delta V_b$ for two different input voltage values as function of the gate length, the gate width, the holding capacitance, and the inverse of the fall time, respectively. Also together plotted are the data extracted experimentally and from two-dimensional device and mixed-mode simulations. The procedure for extracting experimentally the $Q_b$ is: the $t_2$ is determined at the maximum peak from which a line is drawn vertically down to $I_D = 0$; and another line is drawn horizontally from the $I_D$ point determined at $t_3$. The experimental $Q_b$ represents the area surrounded by these two lines and the measured curve. From these figures we can conclude that without adjusting any parameter, the proposed model is capable of accurately calculating the error voltage arising from the channel charges in weak inversion.

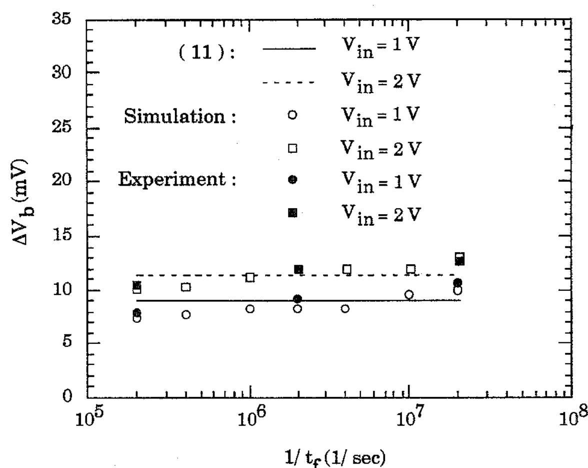
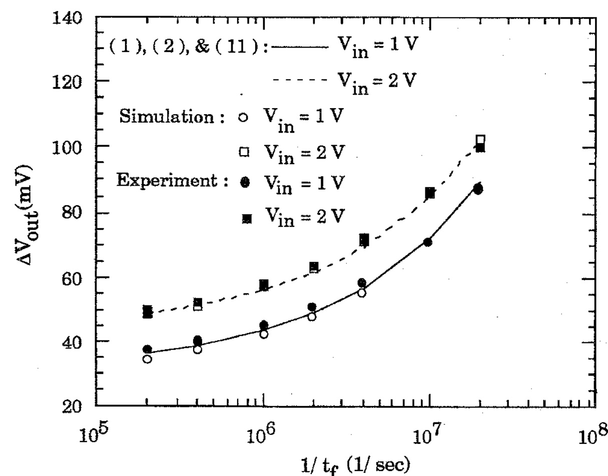
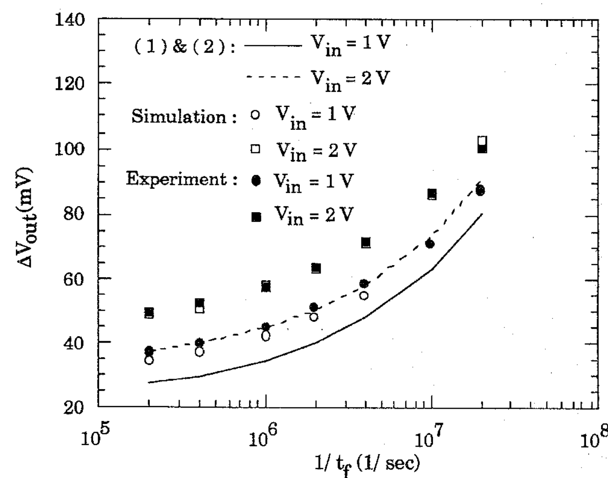



Fig. 9. The comparison of the measured, simulated, and calculated error voltage due to weak inversion charge injection versus the inverse of the fall time for two different input voltage values. $L_G = 5$ $\mu$m; $W_G = 25$ $\mu$m; and $C_H = 1$ pF.




(a)

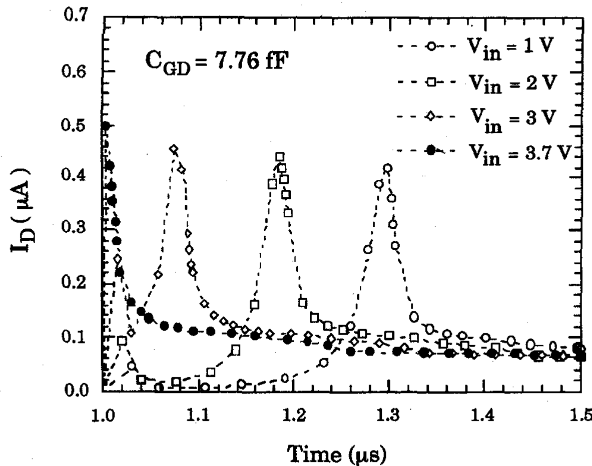



(b)

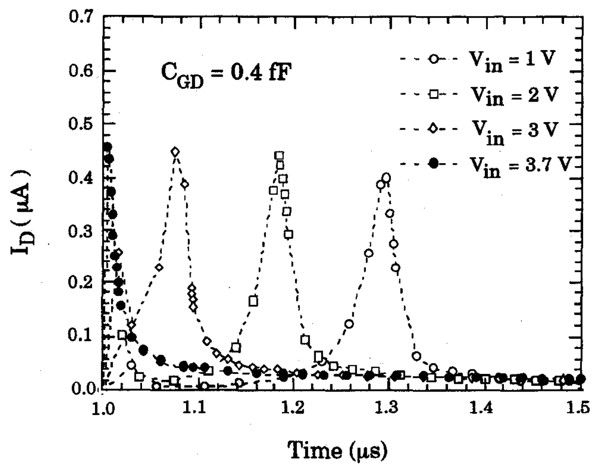
Fig. 10. The comparison of the switch-induced error voltage versus the inverse of the fall time for two different input voltage values, calculated (a) by the complete model expressions (1), (2) and (11), and (b) only by (1) and (2). Also shown are the data from experiment and simulation. $L_G = 5$ $\mu$m; $W_G = 25$ $\mu$m; and $C_H = 1$ pF.

Further observations of Fig. 6 and 7 show that the error voltage $\Delta V_b$ increases with the MOSFET size and this increase can be enhanced by increasing the input voltage. Especially in Fig. 6 if we draw the extrapolations from two lines, they will point toward the same point at $L = 0$, indicating that the $Q_b$ includes a component independent of the channel length. In Fig. 8 the error voltage $\Delta V_b$ behaves really as the inverse of the holding capacitance, indicating that the $Q_b$ is independent of the holding capacitance as demanded by the model. Fig. 9 shows that the error voltage $\Delta V_b$ is considerably independent of the fall time for a wide range, in agreement with our first assumption that the amount of the charges responsible can be evaluated singly at $t_2$. In order to understand the importance of including the new model in the analysis of charge injection in MOS analog switches, we re-plot the total error voltage $\Delta V_{out}$ versus the inverse of the fall time in Fig. 10 with the same conditions as Fig. 9. In Fig. 10(a) the calculated results by employing the complete model expressions (1), (2) and (11) are shown for comparisons with experimental and simulated values. From Fig. 10(a) we can observe that good agreement is achieved. However, neglecting the component $Q_b$ will seriously underestimate the correct value of the error voltage, as depicted in Fig. 10(b). Therefore, our model for weak inversion charge injection in combination of the analytical model for the other two components can provide the ability of accurately predicting the switch-induced error voltage on a switched capacitor.

Again we present some cases of high input voltage and low gate-to-diffusion overlap capacitance. The simulated drain current waveforms with the input voltage as parameter for two different gate-to-diffusion overlap capacitances of 7.76 and 0.4 fF are plotted in Fig. 11. From Fig. 11, we can observe that the component $Q_a$ decreases with increasing the input voltage and approaches nearly zero at a high input voltage of 3.7 V. If the overlap capacitance $C_{GD}$ is reduced to a low value of 0.4 fF, the $Q_c$ becomes less important and at a high $V_{in}$ of 3.7 V the component $Q_b$ dominates the charge injection. The simulated and calculated charge percentage of $Q_b$ versus the inverse of the fall time is plotted in Fig. 12 for two different input voltages of 1 and 3.7 V and two different overlap capacitances of 7.76 and 0.4 fF. Obviously, the calculation agrees closely with the simulated results. It is noted from Fig. 12 that neglecting the component $Q_b$ can cause a large deviation of 90%, which is the same over the illustrated falling time range, for the case of $V_{in} = 3.7$ V and $C_{GD} = 0.4$ fF. Also from Fig. 12 we can observe that: (i) the percentage of $Q_b$ increases with increasing the input voltage for $C_{GD} =$ 0.4 fF; (ii) for the case of $C_{GD} = 0.4$ fF, the influence of $Q_b$ can be reduced by decreasing the falling time for $V_{in} =$ 1 V while it is ineffective for $V_{in} = 3.7$ V; and (iii) for a large $C_{GD} = 7.76$ fF the $Q_b$ component has a considerable amount of 10 to 30%. Therefore, we can conclude that the charge injection due to channel charges in weak inversion can contribute comparably to the switch-induced error voltage and the dominant component of the charge injection at high input




(a)




(b)

Fig. 11. The simulated drain current waveform with input voltage as parameter for (a) $C_{GD} = 7.76$ fF and (b) $C_{GD} = 0.4$ fF. $L_G = 5$ μm; $W_G = 25$ μm; $t_1 = 1.0$ μs; and $t_f$ 500 ns.

voltage and low overlap capacitance arises from the channel charges in weak inversion.

## V. Conclusions

A new quantitative model for weak inversion charge injection in MOSFET analog switches has been established. The model, expressed as function of the process and circuit parameters, has been derived at the critical point where the device is operated in the transition region between strong inversion and weak inversion. Not only the experiments but also the two-dimensional device and mixed-mode simulations have ensured the validity of both the model and the assumptions in the model development. The impact of the weak inversion charge injection has also been demonstrated based on the model.

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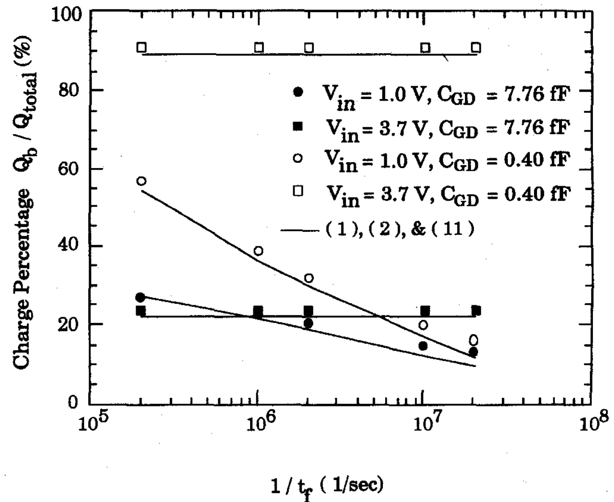


Fig. 12. The simulated and calculated charge percentage of $Q_b/Q_{total}$ versus the inverse of the fall time for four different combinations of $V_{in}$ and $C_{GD}$. $Q_{total} = Q_a + Q_b + Q_c$.$L_G = 5$ μm; $W_G = 25$ μm; and $C_H = 1$ pF.

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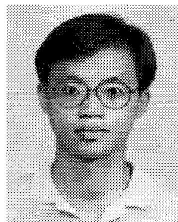

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